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A 10-kHz 12–16-bit reconfigurable zoom ADC with pole optimization technique and floating current-starved amplifier

Zhangming ZHU, Jiajun SONG & Yuhua LIANG*

Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Integrated Circuits, Xidian University, Xi'an 710071, China

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Recently, zoom analog-to-digital converters (ADCs) have been shown to be well-suited for reconfigurable ADCs. They achieve high resolution and high energy efficiency by combining the advantages of the successive approximation register (SAR) ADC and the delta-sigma modulator (DSM) [1,2]. An SAR ADC performs coarse quantization, which is used to update the reference of the DSM. Then, the DSM performs fine quantization to realize high resolution. Compared to DSM, zoom ADCs limit the loop filter swing within the range of the reference voltage determined by the SAR ADC, reducing power consumption. Furthermore, this structure improves the robustness of the loop filter, which provides a more flexible approach for coefficient reconfiguration. A theory for optimizing the noise transfer function (NTF) is proposed to accomplish high energy efficiency in each mode [3]. Nevertheless, the operational transconductance amplifier (OTA) still uses a traditional structure, resulting in high power consumption. The theoretical analysis process for the optimization is also incomplete.

This study proposes a 12–16-bit reconfigurable zoom ADC. As the oversampling ratio (OSR) is set to 100, 60, and 30, the ADC can be reconfigured to be high-resolution mode (16-bit), medium-resolution mode (14-bit), and low-resolution mode (12-bit), respectively. A pole optimization technique is used to improve the signal-to-noise and distortion ratio (SNDR) in the medium-resolution and low-resolution modes. A floating current-starved amplifier (FCA) is proposed, which can achieve less than half the power consumption of a static amplifier. Consequently, the zoom ADC can achieve high energy efficiency in each mode.

Proposed zoom ADC. Figure 1(a) shows the diagram of the reconfigurable zoom ADC. It consists of an SAR ADC and a DSM. The SAR ADC, which serves as a coarse quantization, outputs digital code to generate the reference of the DSM. If the output of the SAR ADC is D, the analog input lies between the voltages V_d and V_{d+1} corresponding to D and $D+1$. Therefore, V_d and V_{d+1} can be used as the high and low references of the DSM. The feedback signal of the fine digital-to-analog converter (DAC) is selected as V_d or V_{d+1} according to the bitstream output of the 1-bit quantizer. Considering the overloads caused by the mismatch between the quantization levels of the SAR ADC, the high and low references should be extended to V_{d+1+M} and V_{d-M}, respectively, where M represents the scaling factor. Figure 1(a) shows the signals in the case of $M=1$. The relevant theoretical derivations are provided in Appendix A.

The resolution of the SAR ADC and scaling factor collectively determine the range of the DSM's reference. Considering the trade-off between accuracy, power consumption, and circuit size, the resolution of the SAR ADC is set to be 5. The asynchronous SAR, which operates at the same f_s as the DSM, can save power because it does not require the SAR ADC to be constantly refreshed in the background. With a bandwidth of 10 kHz, M can take the minimum value of 1 and the input of DSM can still fall within the reference voltage range. The cascade of integrators with feed-forward (CIFF) structure is suitable for low-voltage, low-power applications due to the small loop filter swing. Simulation indicates that to achieve an SNDR greater than 100 dB, a second-order modulator is sufficient.

Pole optimization technique. To satisfy the demands of multimodal applications, the simplest way to achieve multimodality is to adjust the OSR because this can be easily accomplished by adjusting the sample rate.

In high-resolution mode, the OSR is not only related to quantization noise but also to sampling thermal noise, which can be expressed as $2kT/(C\times \mathrm{OSR})$. Considering the modulator shown in Figure 1(a), the coefficient is determined by traditional Butterworth filter design methods. The simulation indicates that when the sampling capacitor is set to 2.4 pF and OSR is set to 100, the quantization noise and sampling noise are at the same level.

In the medium and low accuracy modes, quantization noise is the main source of noise. A pole optimization technique is employed to enhance SNDR. As an NTF with more shaped noise has less in-band noise, the in-band noise can be reduced by increasing the gain at high frequencies while keeping the gain at $z=-1$ unchanged, which can be achieved by shifting the conjugate poles toward the imaginary axis. The change in pole positions before and after optimization is depicted in Figure 1(b). This operation increases the gain at high frequencies and forms a peak in the NTF, as shown in Figure 1(b). It is observed that the overall in-band gain has decreased by approximately 6 dB. And

* Corresponding author (email: yhliang@xidian.edu.cn)

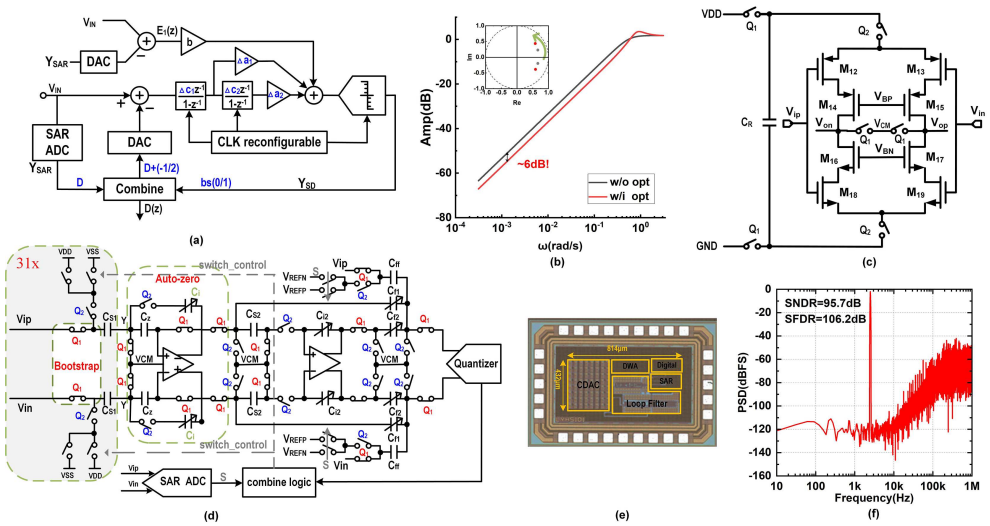

Figure 1 (Color online) (a) System diagram of the reconfigurable zoom ADC; (b) changes of the NTF and the pole positions; (c) floating current-starved OTA; (d) simplified schematic of the system; (e) die photograph; (f) measured PSD in the high-resolution mode.

the OSR is set to 60 and 30 in medium and low accuracy modes, respectively. The simulation shows that using the pole optimization technique, the SNDR is optimized by 3.2 and 4.3 dB for the medium and low accuracy modes, respectively. The pole optimization is achieved by adjusting the gain coefficients (c_1, c_2) and the feedforward coefficients (a_1, a_2) as shown in Figure 1(a).

Circuit implementation. The schematic of the zoom ADC is depicted in Figure 1(d), which includes a 5-bit asynchronous SAR, a 5-bit DAC array, a combined logic circuitry, and a second-order loop filter. The coefficient reconfiguration is achieved by adjusting capacitors. The SAR ADC and combined logic are shown in Appendix B.

The input sampling capacitor and the feedback DAC capacitor are shared. Together with the OSR, the input capacitor determines the thermal noise level, so it is 2.4 pF and consists of 31 units of 77 fF. The bootstrap switches are used to achieve high sampling accuracy.

The current-starved amplifier is often used in energy-efficient design because both N-type and P-type transistors are used as inputs to achieve a larger transconductance. To save static power consumption, this structure can be further improved to a dynamic structure [4]. The floating current-starved amplifier (FCA) is applied here by replacing the current source with a switched capacitor circuit as shown in Figure 1(c). During the sampling phase, the capacitor is charged while the FCA is in the reset state. There is no current in the FCA during this period. During the integration phase, the capacitor supplies power to the amplifier to complete the function of the integrator. The current gradually decreases during this period. The performance of the FCA is closely related to the charge stored in capacitor C_R. Therefore, the size of C_R determines the gain and bandwidth of the OTA. To prove the power efficiency advantages of the FCA, an SC amplifier is simulated with the sampling and holding capacitors set to 10 pF. Simulations indicate that to achieve a harmonic level of −110 dBc, the static current-starved OTA requires a current consumption of 80 μA. However, the FCA only needs to consume an average current of 30 μA with a C_R of 16 pF. The gain and bandwidth of the operational amplifier can be easily adjusted to accommodate different modes by changing the capacitor C_R.

In the high-resolution mode, the FCA needs high gain (> 60 dB), high gain-bandwidth product (GBW) (> $4\times f_s$), and high slew rate (SR) (> 10 V/s) to suppress the error. Consequently, the capacitor C_R is set to be 14 pF. And the capacitors of 12 and 10 pF are sufficient in the medium-resolution and low-resolution modes. The auto-zero technique is employed in the first-stage OTA to reduce the impact of $1/f$ noise and offset as shown in Figure 1(d).

Measurement results. The die photograph of the zoom ADC is shown in Figure 1(e) and is implemented in 0.18 μm technology, occupying an area of 432 μm × 814 μm. At a supply voltage of 1.8 V, the chip consumes a power of 241 μW (the analog part consumes 74 μA, the digital part consumes 38 μA, and the reference consumes 22 μA.)

The zoom ADC achieves 95.7 dB peak SNDR and 97.2 dB DR over a 10 kHz bandwidth. The measured power spectral density (PSD) at peak SNDR is shown in Figure 1(f) with a 2.533 kHz sinusoidal input with a magnitude of −1.94 dBFS. The SNDRs measured in the medium-resolution and low-resolution modes are 82.4 and 71.5 dB, respectively. The detailed results are given in Appendix C.

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Supporting information Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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