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• **Supplementary File** •

A 10-kHz 12-16 bit reconfigurable Zoom ADC with pole optimization technique and floating current-starved amplifier

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Appendix A Theoretical analysis of the Zoom ADC

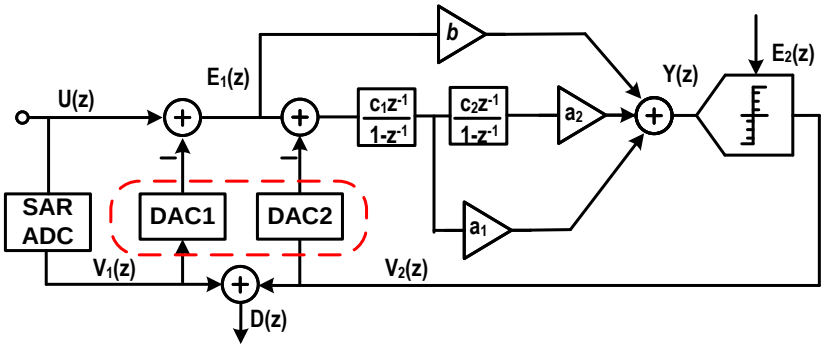

Figure A1 Simplified diagram of the Zoom ADC.

Figure A1 shows the signal flow diagram of the Zoom ADC. To simplify the mathematical derivation, the DAC is divided into two branches. A detailed derivation of the Zoom ADC's transfer function is presented here. The transfer function of the SAR ADC can be expressed as

$$E_1(z) = U(z) - V_1(z) \tag{A1}$$

The loop filter's output is Y, and the transfer function from E_1 and V_2 to Y are denoted by $L_0(z)$ and $L_1(z)$, respectively. Therefore, Y(z) can be expressed as:

$$Y(z) = E_1(z)L_0(z) + V_2(z)L_1(z) \tag{A2}$$

$L_0(z)$ and $L_1(z)$ can be expressed as:

$$L_0(z) = c_1\left[a_1 I(z) + c_2 a_2 I(z)^2\right] + b \tag{A3}$$

$$L_1(z) = -c_1 a_1 I(z) - c_1 c_2 a_2 I(z)^2 \tag{A4}$$

The relationship between Y(z) and $V_2(z)$ can be expressed as:

$$V_2(z) = Y(z) + E_2(z) \tag{A5}$$

And $V_2(z)$ can be expressed by the STF(z) and NTF(z) of the DSM.

$$V_2(z) = STF(z)E_1(z) + NTF(z)E_2(z) \tag{A6}$$

Therefore, the $STF(z)$ and $NTF(z)$ of the DSM can be expressed as:

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} = 1(b = 1) \tag{A7}$$

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$$NTF(z) = \frac{1}{1 - L_1(z)} = \frac{1}{1 + c_1 a_1 I(z) + c_1 c_2 a_2 I(z)^2} \tag{A8}$$

As a result, $V_2(z)$ can be expressed as:

$$V_2(z) = E_1(z) + NTF(z) E_1(z) \tag{A9}$$

So, the output of the system can be expressed as:

$$D(z) = V_1(z) + V_2(z) = U(z) + NTF(z) E_2(z) \tag{A10}$$

The output of the Zoom ADC contains the input signal and the shaping quantization error, which is limited to the V_{LSB} of the SAR ADC. At the circuit level, the Zoom ADC combines the DACs needed to generate V_1 and V_2 into a single DAC. Without the use of a subtractor, this operation thus improves the performance of the circuit.

Appendix B Other circuit implementation

The schematic of the SAR ADC is depicted in Figure B1, and it is composed of several parts including the sampling switch, DAC array, comparator, and SAR logic. The SAR ADC employs asynchronous timing and completes conversion during the sampling phase of the modulator. The unit capacitor is around 10 fF to achieve high accuracy more than 8-bit. During the sampling phase, the input signal is sampled and held to the capacitor array through bootstrap switches. During the conversion phase, the dynamic comparator, which is the same as the one used in the DSM, utilizes asynchronous clock feedback from the SAR logic to rapidly complete five comparisons. At the same time, the locked digital code by the SAR control logic is output to the fine DAC. The dynamic logic is used to simplify design and reduce power consumption.

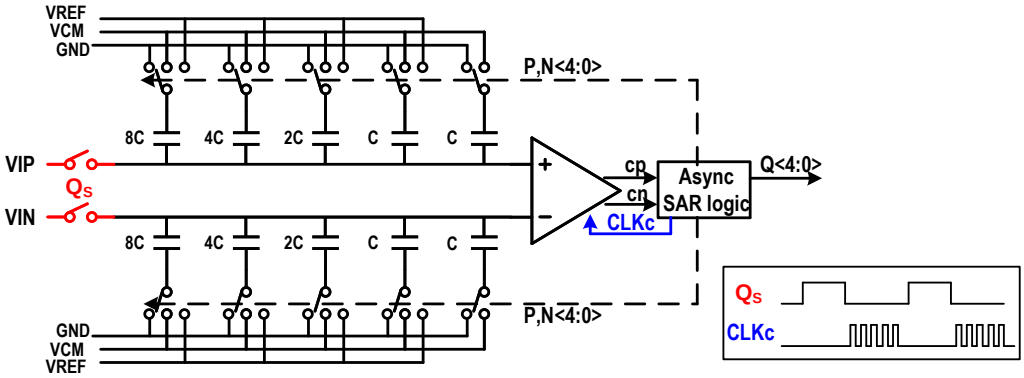

Figure B1 Simplified schematic of the SAR ADC.

The diagram of the combine logic circuit in the Zoom ADC is shown in Figure B2. The 5-bit digital output generated by the SAR ADC and the scaling factor M are simultaneously fed into a 5-bit adder and a 5-bit subtractor, and the reference D_{ref+} and D_{ref-} is obtained through digital addition and subtraction operations. These two signals are then used as input signals for a multiplexer. And the 1-bit digital code stream output by the Delta-Sigma modulator serves as the control signal for the multiplexer. According to the 1-bit digital code, the D_{ref+} or D_{ref-} is selected to control the fine DAC. Additionally, the output of the combine logic circuit serves as the final digital output of the Zoom ADC.

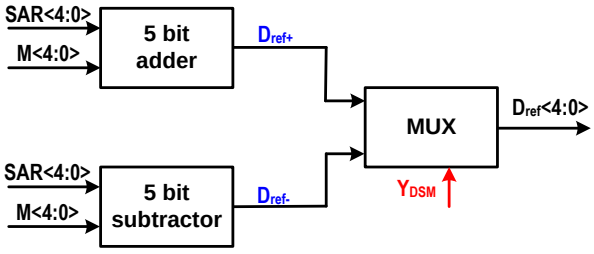

Figure B2 Diagram of the combine logic.

Appendix C All measurement results

Figure C1(a) shows the measured SNDR and SNR versus the input amplitude for a 2.533 kHz sinusoidal input in high-resolution mode. The Zoom ADC achieves 95.7 dB peak SNDR and 97.2 dB DR over a 10 kHz bandwidth. The measured PSD at peak

SNDR is shown in Figure B1(b) with a 2.533 kHz sinusoidal input with a magnitude of −1.94 dBFS. The measured results in medium-resolution and low-resolution modes are shown in Figure B1(c) and Figure B1(d). The Zoom ADC achieves an SNDR of 82.4dB and 71.5dB, respectively.

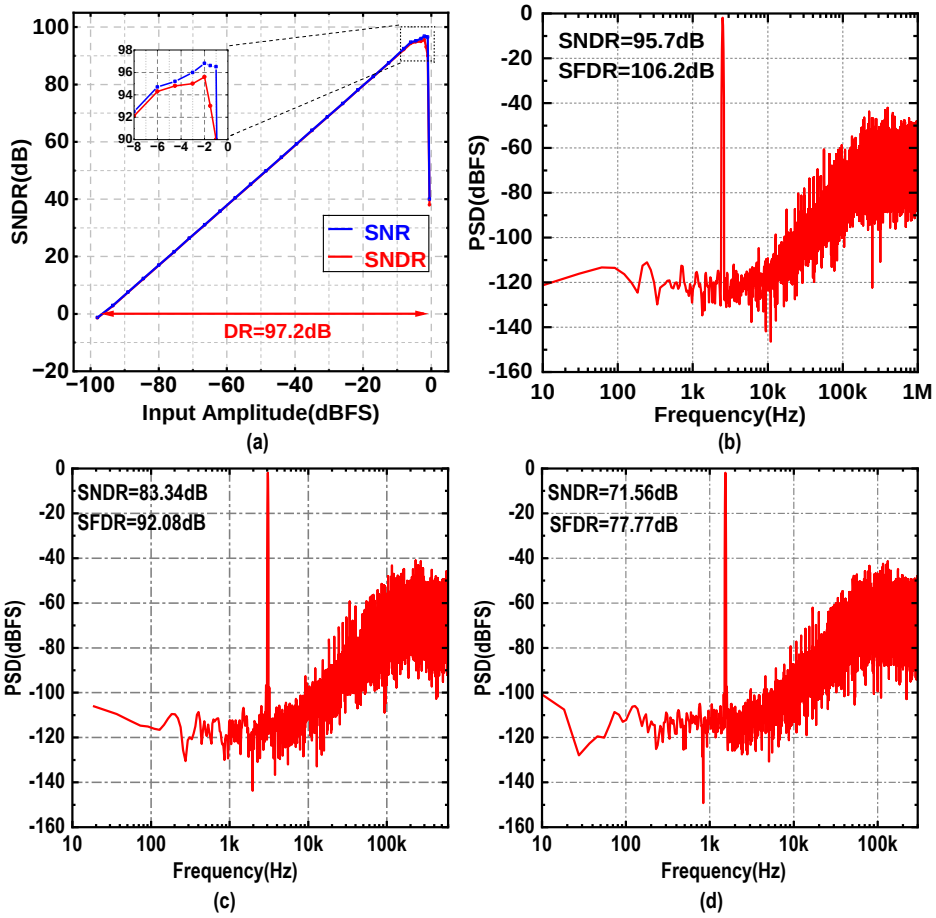

Figure C1 (a)Measured SN(D)R versus input amplitude. Measured out spectrum of the Zoom ADC (a)in the high-resolution mode. (b)In the medium-resolution mode (c) In the low-resolution mode.

Table 1 lists a comparison of this design with some recent advanced research results under similar parameters (SNDR > 90 dB) in recent years. It can be observed that this design achieves a Schreier figure of merit (FoM) of 171.8 dB, reaching an internationally advanced level.

Table C1 performance summary and comparison.

Reference	[1]	[2]	[3]	[4]	[5]	This work
Process(nm)	160	180	180	65	180	180
OSR	282	250	384	88	96	100
BW(kHz)	20	10	10	50	250	10
Fs(MHz)	11.29	10	7.68	8.8	48	2
Power(μW)	1120	1300	378	243	17700	241
SNDR(dB)	103	102.8	103.3	92	103.2	95.7
DR(dB)	109	104.2	110.3	97.4	104	97.2
FoMs(dB)	175.5	174.6	177.6	175.1	174.7	171.8

FoMs=SNDR+10*log(BW/power)

References

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