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A high consistency ramp circuit design method for negative feedback adaptive adjustment mechanism applied to large area array CMOS image sensors

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Generally speaking, the column level ADC provides ramp signals for each column in the way of global ramp [1]. At present, the scale of the high-end image sensor array has reached tens of millions, hundreds of millions or even billions [2]. With the increasing scale of the image sensor array, the parasitic metal routing on the ramp becomes larger and larger [3], and the inconsistency of the ramp becomes more and more obvious. Tens of thousands of comparators work at the same time, and the distortion of the ramp signal of the input stage of the comparator is becoming more and more serious, resulting in the failure of the global ramp. Although the use of regional multi-ramp design can reduce the above effects, there is a natural mismatch among multi-ramp circuits. Therefore, in the special application environment of super large area array CIS, there are differences between the ramp signals of each column no matter using the global ramp signal generator or the block-based multi-ramp generator.

In order to address the inconsistency problem caused by parasitic backend wiring among multiple ramp generators and among multiple columns in large-array CMOS image sensors(CIS), this study adopts a high-precision compensation technology combining average voltage technology, adaptive negative feedback dynamic adjustment technology and digital correlation double sampling technology to complete a ramp circuit design for high consistency adaptive adjustment of large area CMOS image sensor, as shown in Figure 1(a). The distributed multi-ramp circuit used in this study interconnects the ramps through metal wires, which can average the ramp voltage signals, reduce the inconsistency caused by the matching problem of the circuit itself, and greatly improve the consistency among the ramp signals.

The integrated current generation circuit is a voltage to current conversion realized by using switched capacitors to simulate accurate resistors. The principle of its current generation is the same as (1). The value of I_{REF} is determined by the control signal frequency f_0 of switches S_4 and S_5, common mode voltage V_{CM} and capacitance C_{01}.

$$I_{\mathrm{REF}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{CM}}}{1/(f_0 \cdot C_{01})} = (V_{\mathrm{DD}} - V_{\mathrm{CM}}) \cdot f_0 \cdot C_{01}. \quad (1)$$

As shown in the ramp signal generation circuit in Figure 1(a), in the case of large array CMOS image sensors, it is very difficult for some global signals to be completely consistent. The driving capacity of ramp start voltage V_H is very large, so four buffers are used to provide start voltage V_H to 8192 columns respectively. Considering that the offset voltage between buffers is different, different common mode errors will be introduced to the ramp circuit, so the common mode difference needs to be eliminated by the digital correlation double sampling technology in the design [4]. The error detection circuit only samples the ramp output signal of the last column of ramp voltage generation circuit, and feeds back the difference between the termination voltage of the actual ramp and the termination voltage V_L of the ideal ramp to the V_{FB} signal. V_{FB} is the input of the voltage controlled oscillator. The feedback V_{FB} controlled voltage controlled oscillator generates a digital signal with a frequency of f_0. The frequency f_0 completes the negative feedback mechanism of adaptive adjustment of ramp by adjusting the required integral current.

The specific working process can be generally summarized into four processes: reset, hold, slope generation and calibration. The switch state of the error detection circuit in the ramp generation stage is exactly the same as those in the hold stage, and the charges of capacitors C_2, C_3, C_4 are the same as those in the hold stage. The formula for generating ramp voltage signal at this stage is:

$$\begin{aligned} V_{\mathrm{ramp}} &= V_H - \frac{I_{\mathrm{REF}} \cdot T_{\mathrm{ramp}}}{C_1} \\ &= V_H - \frac{(V_{\mathrm{DD}} - V_{\mathrm{CM}}) \cdot f_0 \cdot C_{01} \cdot T_{\mathrm{ramp}}}{C_1}. \end{aligned} \quad (2)$$

T_{ramp} is the integration time corresponding to the ramp generation signal, and C_1 is the integration capacitance. It can be seen from (2) that within the integration time of T_{ramp}, the circuit will generate a descent ramp with an initial level of V_H as time goes by. C_{01} and C_1 in (2) are relative quantities, and this ratio relationship can be well maintained in the actual process. f_0 is the frequency of the

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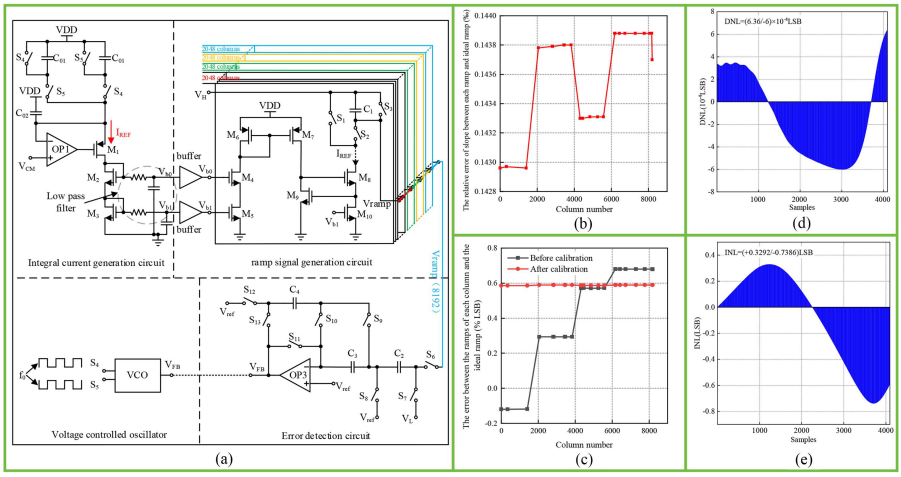

Figure 1 (Color online) (a) High consistency adaptive ramp circuit for large area CMOS image sensor; (b) relative error diagram of slope between adaptive ramp and ideal ramp; (c) error diagram among the ramp signals of each column; (d) DNL; (e) INL.

switch control signal of the integral current generation module, f_0 and T_{ramp} are both digital signals, so the impact of signal mismatch is also small.

In the calibration stage, the integration stops, and the termination voltage $V_{\text{ramp}(3)}$ of the actual ramp in the ramp generation phase is sampled on the capacitor C_2. From the ramp generation stage to the calibration stage, according to the charge conservation between the right pole plate of capacitor C_2 and the left pole plate of capacitor C_4, there are:

$$V_{\text{FB}(4)} = \frac{C_2}{C_4} \cdot [V_L - V_{\text{ramp}(3)}] + V_{\text{FB}(2)} + V_{\text{OS}}. \quad (3)$$

As can be seen from (3), the adaptive calibration circuit samples the actual termination output voltage of the ramp after the end of each ramp generation cycle, compares it with the termination voltage V_L of the ideal ramp, and sends the difference of the comparison to the input V_{FB} of the voltage controlled oscillator through the error detection circuit.

Simulation results. As shown in Figure 1(b), it can be seen that the difference between the maximum value and the minimum value of the actual ramps and the ideal slope is about 0.144‰ and 0.143‰ respectively. By making a difference between the maximum value and the minimum value, it can be concluded that the slope difference among the ramp signals of 8192 columns is only one millionth, which obviously ensures the high consistency of the ramp signal.

As shown in Figure 1(c), the point line diagram before correction is the curve diagram corresponding to the bias voltage provided by the low-voltage cascode circuit, and the maximum error among each large module is about 0.8 LSB. In order to reduce the introduction of noise here, the ordinary cascode circuit is used to generate V_{b1}. Combined with the modulated cascode current mirror, the integral current is copied to each column of ramp circuit to further improve the linearity of ramp signal, as shown in the corrected dotted line diagram in Figure 1(c). After using the above method, the inconsistency of ramp signals among each large module is reduced by 99.28%, and the maximum error generated is less than 0.4% LSB, which greatly improves the consistency of each ramp. From Figure 1(d), DNL is +0.000636 LSB/−0.0006 LSB, which meets the design requirements. From Figure 1(e), INL is +0.3292 LSB/−0.7386 LSB.

When using the traditional method, the chip area is 88 mm(H)×88.5 mm(V), and the chip length in the vertical direction is 88.5 mm. However, when the chip uses the method in this study, it will introduce an additional length of about 500 μm in the vertical direction, so it will introduce 0.6% more in the overall area. In the traditional method, each column of the circuit needs to consume about 75 μA of current. After using the method in this study, it needs to consume about 360 nA more current in each column, so the power consumption on each column is about 0.5% more.

Conclusion. In this study, a design method of high consistency adaptive ramp circuit based on distributed integration is proposed. The method is applied to a CMOS image sensor with 8192(H)×8192(V) pixel array using 55 nm 1P4M process. The pixel size is 10×10 μm^2, the chip area is 88(H)×89(V) mm^2, and the analog-to-digital converter is a 12 bit-SS ADC. The experimental results show that the column fixed pattern noise can be reduced to 0.000037% at a frame rate of 10 fps, the inconsistency error among the ramp signals of each column is less than 0.4% LSB, and the chip area and power consumption are only increased by 0.6% and 0.5%, respectively. This method provides a theoretical guidance for the development of high-performance large area array CMOS image sensor.

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