

Appendix A Processor Architecture

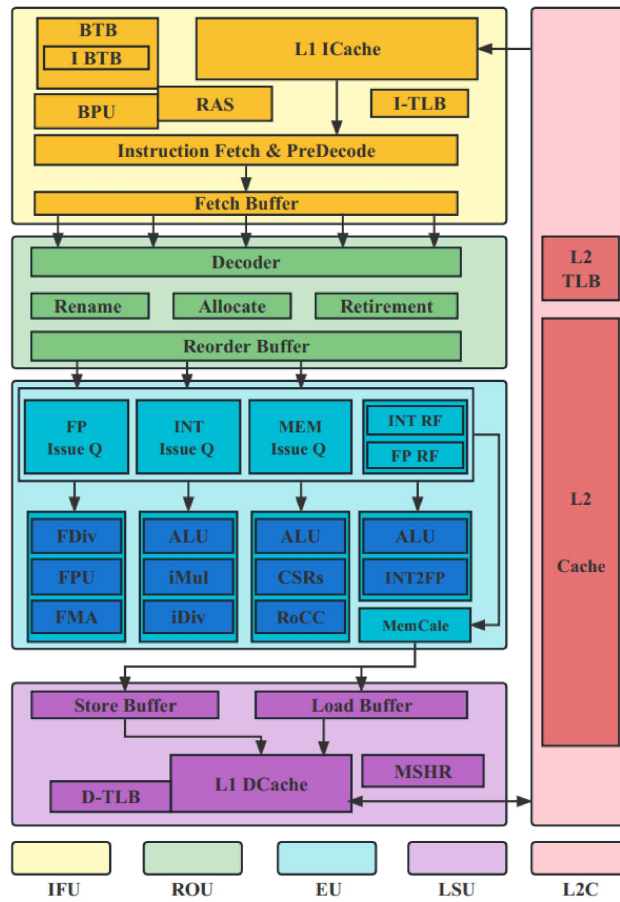


Figure A1 BOOM architecture schematic.

Appendix B Parameters and Constraints List

Table B1 Microarchitectural Parameters List

Module	Parameter	Index	Min;Interval;Max	Type
IFU	Instruction Queue Size	p_1	16;4;64	L
	Run ahead Queue Size	p_2	4;1;16	L
	Instruction BTB Set	p_3	6;1;8	E
	L1ITLB Way	p_4	8;4;64	L
	BTB Set	p_5	7;1;10	E
	BTB Way	p_6	4;4;8	L
	L1ICache Set	p_7	6;1;9	E
	L1ICache Way	p_8	4;4;8	L
ROU	Decode Width	p_9	2;1;4	L
	FP Decode Queue Credits	p_{10}	4;2;16	L
	Int Decode Queue Credits	p_{11}	4;2;16	L
	NZCV Register Map Queue	p_{12}	16;4;44	L
	Int Register Map Queue	p_{13}	40;8;136	L
	Vector Register Map Queue	p_{14}	16;4;72	L
	PC Buffer Size	p_{15}	16;4;48	L
	Reorder Buffer Size	p_{16}	32;8;128	L
	Int μ op Decode Width	p_{17}	2;1;4	L
	FP μ op Decode Width	p_{18}	2;1;3	L
	Int Rename Width	p_{19}	2;1;4	L
	FP Rename Width	p_{20}	2;1;4	L
EU	Int ALU1 Issue Queue Size	p_{21}	8;2;24	L
	Int ALU2 Issue Queue Size	p_{22}	8;2;24	L
	Int ALU3 Issue Queue Size	p_{23}	8;2;24	L
	LSU1 Issue Queue Size	p_{24}	8;2;20	L
	LSU2 Issue Queue Size	p_{25}	8;2;20	L
	LSU3 Issue Queue Size	p_{26}	8;2;20	L
	ALU Write Ports No.	p_{27}	2;1;3	L
	LSU1 Write Ports No.	p_{28}	2;1;4	L
	LSU2 Write Ports No.	p_{29}	2;1;4	L
	Int ALU Register No.	p_{30}	82;8;154	L
	FP ALU Register No.	p_{31}	56;4;100	L
	FP Issue Queue Size	p_{32}	16;4;20	L
	FP Data Issue Queue Size	p_{33}	12;4;16	L
LSU	DTLB Way	p_{34}	16;2;64	L
	L1 DCache Set	p_{35}	7;1;8	E
	L1 DCache Way	p_{36}	4;4;8	L
	Memory Data Block size	p_{37}	8;2;128	L
	Load Buffer Size	p_{38}	16;2;64	L
	Store Buffer Size	p_{39}	8;2;32	L
	Store Commit Buffer Size	p_{40}	4;1;16	L
L2C	L2 Cache Set	p_{41}	8;1;10	E
	L2 Cache Way	p_{42}	6;1;8	L
	L2 Return Store Buffer Size	p_{43}	16;1;64	L

Table B2 System & Custom Design Rules

No.	Description	Type
1	L2 Cache Set * L2 Cache Associativity ≥ 4096	Customer Constraint
2	L1ICache set ≥ 8	Customer Constraint
3	FP decode queue credits > Decode Width	System Constraint
4	Load Buffer Size > Store Buffer Size	System Constraint
5	Int Rename Width = Int μ op Decode Width	System Constraint
6	FP Rename Width = FP μ op Decode Width	System Constraint
7	Load Buffer Size \geq LSU1 Write Ports Number + LSU2 Write Ports Number	System Constraint
8	Int ALU1 Issue Queue Size = Int ALU2 Issue Queue Size	System Constraint
9	Int ALU2 Issue Queue Size = Int ALU3 Issue Queue Size	System Constraint
10	LSU1 Write Ports No. = LSU2 Write Ports No.	System Constraint

Table B3 Model Constraints. δ is an extremely small positive number to convert open constraints into closed constraints.

No.	Constraint formulation	Type
1	$-\sum_{k=1}^{m_{41}} p_{41}^{(k)} y_{41}^{(k)} * \sum_{k=1}^{m_{42}} p_{42}^{(k)} y_{42}^{(k)} \leq -4096$	Quadratic inequality
2	$2^8 - \sum_{k=1}^{m_8} p_8^{(k)} y_8^{(k)} \leq 0$	Customer Constraint
3	$\sum_{k=1}^{m_9} p_9^{(k)} y_9^{(k)} - \sum_{k=1}^{m_{10}} p_{10}^{(k)} y_{10}^{(k)} - \delta \leq 0$	Linear inequality
4	$\sum_{k=1}^{m_{39}} p_{39}^{(k)} y_{39}^{(k)} - \sum_{k=1}^{m_{38}} p_{38}^{(k)} y_{38}^{(k)} - \delta \leq 0$	Linear inequality
5	$\sum_{k=1}^{m_{17}} p_{17}^{(k)} y_{17}^{(k)} - \sum_{k=1}^{m_{19}} p_{19}^{(k)} y_{19}^{(k)} = 0$	Linear equality
6	$\sum_{k=1}^{m_{18}} p_{18}^{(k)} y_{18}^{(k)} - \sum_{k=1}^{m_{20}} p_{20}^{(k)} y_{20}^{(k)} = 0$	Linear equality
7	$\sum_{k=1}^{m_{28}} p_{28}^{(k)} y_{28}^{(k)} + \sum_{k=1}^{m_{29}} p_{29}^{(k)} y_{29}^{(k)} - \sum_{k=1}^{m_{38}} p_{38}^{(k)} y_{38}^{(k)} - \delta \leq 0$	Linear inequality
8	$\sum_{k=1}^{m_{21}} p_{21}^{(k)} y_{21}^{(k)} - \sum_{k=1}^{m_{22}} p_{22}^{(k)} y_{22}^{(k)} = 0$	Linear equality
9	$\sum_{k=1}^{m_{22}} p_{22}^{(k)} y_{22}^{(k)} - \sum_{k=1}^{m_{23}} p_{23}^{(k)} y_{23}^{(k)} = 0$	Linear equality
10	$\sum_{k=1}^{m_{28}} p_{28}^{(k)} y_{28}^{(k)} - \sum_{k=1}^{m_{29}} p_{29}^{(k)} y_{29}^{(k)} = 0$	Linear equality

Appendix C Running Time Comparison of Optimization Algorithm in Numerical Experiment

Table C1 Average iteration time of SOBPs and HEBO, ECO-HCT, SRADE.

Algorithm	ECO-HCT	SRADE	HEBO	SOBP
Running time/s	29.5	27.78	50.9	40.6