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Demonstration of normally-off p-channel GaN transistor with high threshold voltage and low subthreshold swing based on single p-GaN

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GaN outperforms silicon in applications with high power and high frequency owing to the high critical electric field and high electron mobility. However, the hole-based GaN transistors which are pivotal to the GaN-based CMOS circuits and high-side switching are still under investigation. Two-dimensional hole gas (2DHG) has been used to demonstrate the p-channel GaN field-effect-transistors (FETs) [1–5]. However, almost all of the contemporary research are based on the heterostructures (e.g., p-GaN/AlN, p-GaN/AlGaN, p-GaN/AlInGaN), as the 2DHG is likely to be generated adjacent to the interface benefiting from the polarization effect. The epitaxial design of the heterostructures is relatively complex and less cost-effective. Even more, selective regrowth is required for some of the p-FETs, which has limited reproducibility and is time-consuming and costly. In addition, a parasitic two-dimensional electron gas (2DEG) channel is always unavoidable in most of the aforementioned structures [4]. Moreover, the reproducibility of the device performance is affected by the 2DHG which is vulnerable to factors such as the Al composition, the thickness of the back barrier, the thickness of p-GaN, and the delay effect of Mg.

In this study, we fabricate the GaN p-FETs using a single p-GaN epitaxially grown on a 6-inch Si substrate, which is easier to scale up and more cost-effective. The parasitic 2DEG channel is also excluded as the p-channel locates in the single p-GaN rather than the heterointerface. A gate-recessed design is adopted to engineer E-mode (normally-off) GaN p-FETs. Several outstanding DC performances have been obtained.

Experiments. The schematic diagram of the GaN p-FET device with a gate length of 50 μm (100 μm gate width) as well as the epilayer structure is delineated in Figure 1(a). A 300 nm p-GaN is grown on a 6-inch GaN-on-Si template. Below the 300 nm p-GaN is the 1 μm-thick insulating GaN doped with carbon, which acts as the isolation layer for each device. The cross-sectional structure is shown in Figure 1(b) by transmission electron microscopy (TEM). The source (S) and drain (D) electrodes are designed by photolithography. A Ni(20 nm)/Au(40 nm) metal stack is deposited by e-beam evaporation followed by annealing in oxygen at 550°C for 10 min. Then the devices are isolated by ICP and passivated by SiO_2. A ∼280 nm-deep gate recess is determined by ICP. The gate metal composed of Ti(20 nm)/Al(500 nm)/Ni(20 nm) is on a 20 nm Al_2O_3 dielectric layer.

Results and discussion. The ohmic contact resistivity is evaluated by transfer length method (TLM) [4] with R_c of 129 Ω·mm and R_{sh} of 219 kΩ/□ (Figure 1(c)). With positive sweep (i.e., V_{GS} from −9 to 2 V) (Figure 1(d)), the GaN p-FET with a gate length of 50 μm demonstrates a V_{th} of −5.3 V by linear extrapolation [1]. While with negative sweep (i.e., V_{GS} from −9 to 2 V) (Figure 1(e)), the V_{th} shifts to −4.4 V, showing a V_{th} hysteresis of 0.9 V, which may be caused by the traps located in the interface between the p-channel and dielectric. The I_g is in the range of few nA/mm as $V_g > -8$ V, guaranteeing an ultra-low static power consumption in CMOS ICs. Figure 1(f) shows an I_{ON}/I_{OFF} ratio of 2.4×10^5 and SS values under negative and positive sweeps of 136 and 186 mV/dec, respectively. The R_{ON} is extracted at $V_{DS} = -5$ V from Figure 1(g). A maximum output current density of 9.0×10^{-5} mA/mm is obtained at $V_{DS} = -10$ V. The low output current should be partly due to the long gate length ($L_g = 50$ μm). The GaN p-FET is completely turned off at $V_{GS} = 0$ V with an I_g of $\sim 4.2 \times 10^{-7}$ mA/mm, indicating an ultra-low static power consumption which is desired in CMOS logic gates [4]. Figure 1(h) benchmarks the V_{th} and SS with other GaN p-FETs. The GaN p-FET in this study demonstrates the highest V_{th} among all the state-of-the-art ones, which all benefit from the 2DHG generated by the heterostructures. The one in this study also preserves the lowest SS among all the p-FETs with a GaN/Al(Ga)N heterostructure. By scaling down the gate length and width to 3 and 20 μm, a V_{th} of

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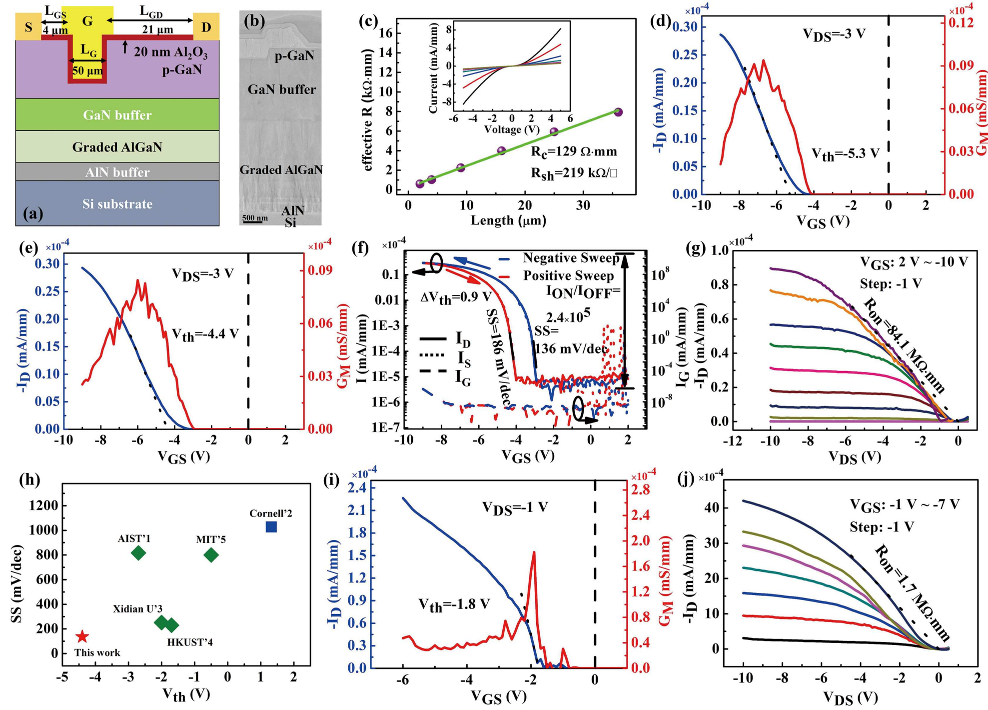

Figure 1 (Color online) (a) Schematic diagram and (b) cross-sectional TEM image of an E-mode GaN p-FET with a gate length of 50 μm. (c) TLM results of the as-fabricated Ni/Au contact pads. The transfer characteristics of the GaN p-FET with positive (d) and negative (e) sweeps. (f) Switching and (g) output characteristics. (h) Benchmark of GaN p-FETs in terms of $V_{\rm th}$ and SS. (i) Transfer and (j) output characteristics of the GaN p-FET with a gate length of 3 μm.

−1.8 V, a hole mobility of 0.002 $\rm cm^2/V{\cdot}s$, and an $I_{\rm ON}/I_{\rm OFF}$ ratio of 2.3×10^6 are extracted from Figure 1(i). An output current of 4.2 μA/mm is obtained under a gate voltage of −8 V from Figure 1(j). An $R_{\rm ON}$ of 1.7 MΩ·mm is extracted at $V_{\rm DS}=-3$ V. The output performance is limited by the deeper depth of the gate recess. Further reducing the thickness of Al_2O_3 dielectric layer or using the high-K dielectric materials to increase gate-channel capacitance may improve the device performance. Moreover, scaling down the gate length will also benefit the improvement of output current.

Conclusion. The E-mode GaN p-FETs of different gate lengths on single p-GaN are demonstrated. With a gate length of 50 μm, the p-FET exhibits a high $V_{\rm th}$ up to −4.4 V and a low SS of 136 mV/dec with an $I_{\rm ON}/I_{\rm OFF}$ ratio of 2.4×10^5 and low I_g. By scaling down the gate length to 3 μm, an output current of 4.2 μA/mm is obtained, revealing the probability of fabricating normally-off p-FET on single p-GaN, which paves a facile and cost-effective way to fabricate GaN complementary and power integrated circuits.

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