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High performance 2T0C DRAM cells based on atomic-layer-deposited InAlZnO FETs

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Recently, the oxide semiconductor-based 2T0C dynamic random-access memory (DRAM) has shown great potential in monolithic three-dimensional (M3D)-integrated memory, owing to some unique advantages of oxide semiconductors, such as high electron mobility, wide band gap, and compatibility with back-end-of-line (BEOL) processes [1, 2]. More importantly, benefiting from excellent step coverage and precise nanoscale thickness controllability, atomic layer deposition (ALD) technology holds great promise for the fabrication of ultrathin oxide semiconductor transistors, especially in high-density vertical-structure 2T0C DRAM applications [3, 4]. To date, 2T0C DRAM cells based on various ALD oxide semiconductor transistors, such as ALD IGZO and ZnO, have been reported; however, their retention ability and reliability require further improvements [2, 5]. By contrast, InAlZnO (IAZO) has a larger bandgap and higher oxygen vacancy formation energy than most oxide semiconductors, such as ZnO, In_2O_3, and IGZO [6]. Accordingly, the use of IAZO transistors is expected to improve the retention characteristics and reliability of the 2T0C DRAM cells. In this letter, a 2T0C DRAM cell consisting of two short-channel IAZO-based field-effect transistors (FETs) was fabricated using plasma-enhanced (PE) ALD, exhibiting a fast write speed of 10 ns, long retention time of >18 ks, 3-bit storage capability, and excellent endurance of $>10^{11}$. These results demonstrate the potential of ALD IAZO-based 2T0C DRAM cells in M3D integrated memory applications.

Experimental. To form a bottom gate, a 50 nm W film was deposited on the SiO_2/Si substrate by sputtering, followed by electron beam lithography (EBL) and dry etching. Then, a 7 nm Al_2O_3 film was used as the gate dielectric grown by thermal ALD at 200°C. Subsequently, a 5 nm IAZO channel film was grown by plasma-enhanced ALD (PEALD) at 200°C, where $In(CH_3)_3$, $Al(CH_3)_3$, $Zn(C_2H_5)_2$ and O_2 plasma were used as the sources of In, Al, Zn, and O, respectively. The IAZO film was deposited by alternating the growth of one Al_2O_3 cycle and two InZnO supercycles, where one InZnO supercycle contained three cycles of In_2O_3 and one ZnO cycle. The atomic percentages of In, Al, and Zn were 33.1%, 14.2% and 7.8%, respectively. The channel was defined using EBL and wet etching. Subsequently, 50 nm Ni source/drain electrodes were formed by sputtering. Finally, a 20 nm Al_2O_3 film was deposited on the back of the channel by thermal ALD at 200°C as a passivation layer using the $Al(CH_3)_3$ and H_2O precursors. The threshold voltage ($V_{\rm th}$) was defined as the gate voltage at which drain current is equal to channel width/length (W/L) $\times$ 10^{-10}. The 2T0C DRAM cell was fabricated by interconnecting two IAZO transistors. The optical image of the 2T0C DRAM cell and scanning electron microscope (SEM) images of the local channel area are shown in Figure 1(a), where the source of the write transistor ($T_{\rm Write}$) is connected to the gate of the read transistor ($T_{\rm Read}$).

Results and discussion. Figure 1(b) shows a typical hysteresis transfer curve of the IAZO transistor with a channel length of 100 nm, where almost no hysteresis window is observed, indicating a high-quality Al_2O_3 dielectric and an ideal interface. Figure 1(c) shows the $V_{\rm th}$ shift of the IAZO transistors as a function of stress time under positive and negative bias stresses. After stressing at +3 and −3 V for 60 min, the $V_{\rm th}$ shifts were 0.07 and −0.08 V, respectively. This reveals the excellent bias-stress stability of the IAZO transistor. Additionally, the memory performance of a 2T0C DRAM cell based on the aforementioned IAZO transistors was studied. Figure 1(d) shows the circuit schematic of the 2T0C DRAM cell. A timing diagram of the write and read operations is shown in Figure 1(e). During the write operation, the peak voltages applied to the write word line ($V_{\rm WWL}$) and write bit line ($V_{\rm WBL}$) were set to 4 and 3 V, respectively. The write time, defined as the overlap time between $V_{\rm WWL}$ and $V_{\rm WBL}$, was 10 ns. During the read operation, a negative hold voltage ($V_{\rm Hold}$) was applied to the write word line (WWL) to minimize the off-current of $T_{\rm Write}$. The voltages applied to the read bit line ($V_{\rm RBL}$) and read word line ($V_{\rm WBL}$) were kept at 0.1 and 0 V, respectively, to determine the memory state through the source-drain current ($I_{\rm Read}$) of $T_{\rm Read}$. Figure 1(f) shows the relationship between storage node voltage ($V_{\rm SN}$) and $I_{\rm Read}$ determined by polynomial fitting. Figure 1(g) shows $V_{\rm SN}$ as a function of time before and after the write operation. The retention time ($t_{\rm retention}$) of the 2T0C DRAM cells (defined as the time required for $V_{\rm SN}$ to drop to 0.1 V) was more than 18 ks, which is attributed to the extremely low off-current of the IAZO transistors. The storage capacitance ($C_{\rm s}$) was approximately 15 fF, which was calculated based on the gate dielectric capacitance density and capacitance area of the $T_{\rm Read}$. The actual off-state leakage current

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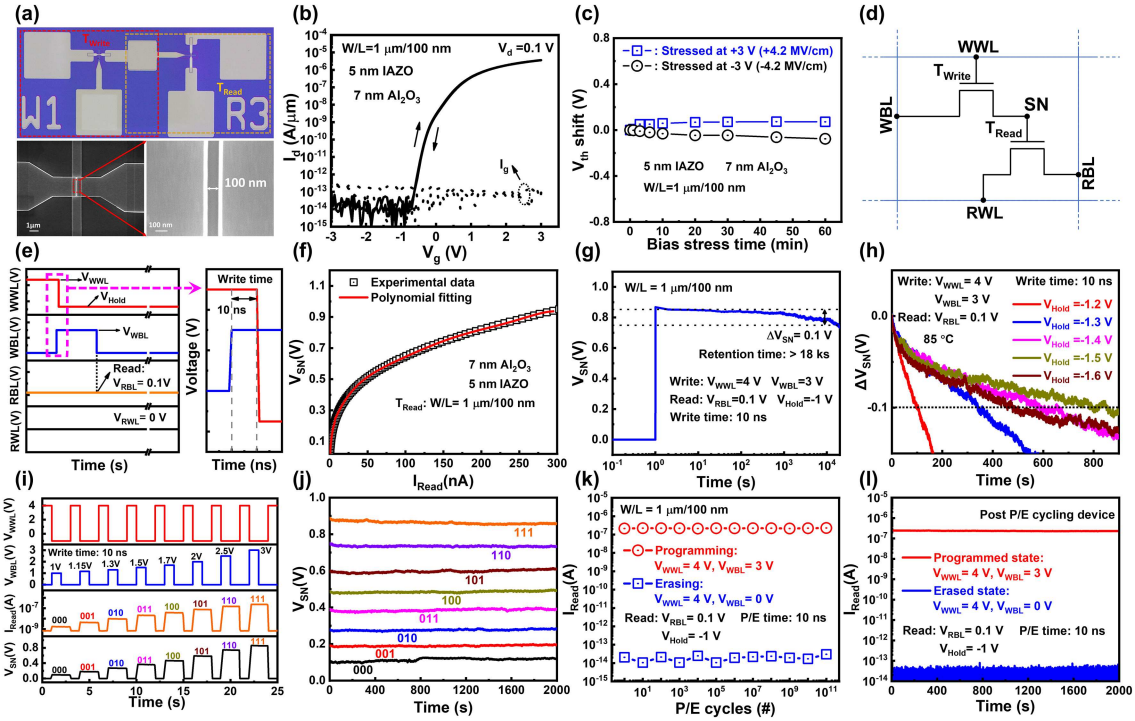

Figure 1 (Color online) (a) Optical image of the 2T0C DRAM cell and SEM images of the local channel area; (b) transfer curve of IAZO transistors; (c) $V_{\rm th}$ shifts of IAZO transistors as a function of stress time at 3 and −3 V, respectively; (d) circuit schematic and (e) operation timing diagram of the 2T0C DRAM cell; (f) polynomial fitting of $V_{\rm SN}$-$I_{\rm Read}$ data; (g) retention characteristics of the 2T0C DRAM cell at room temperature; (h) $\Delta V_{\rm SN}$ as a function of retention time for the 2T0C DRAM cell at various $V_{\rm Hold}$ at 85°C; (i) operation timing diagram and (j) retention characteristics of the 3-bit multilevel storage of 2T0C DRAM cell; (k) endurance characteristics of 2T0C DRAM cell; (l) retention characteristics of 2T0C DRAM cell after 10^{11} P/E cycles.

($I_{\rm leak}$) was calculated as follows:

$$I_{\rm leak} = \frac{0.1\ {\rm V} \times C_s}{t_{\rm retention}}, \tag{1}$$

which is about 8.2×10^{-20} A/μm. This low off-state leakage current is attributed to the large bandgap of the IAZO films. The retention characteristics of the 2T0C DRAM cells at 85°C were further evaluated at different $V_{\rm Hold}$, as shown in Figure 1(h), where the longest retention time of 800 s is achieved at $V_{\rm Hold}$ of −1.5 V. The significant decrease in retention time at 85°C is due to an increase in $I_{\rm leak}$ as the measurement temperature increases. The 3-bit multilevel storage characteristics of the 2T0C DRAM cells were realized by controlling $V_{\rm WBL}$, as shown in Figure 1(i). The retention characteristics of the eight states are presented in Figure 1(j). The $V_{\rm SN}$ corresponding to the eight states with memory windows over 10^5 are evenly distributed in the range of 0–0.9 V, and after a retention time of 2000 s, a sufficiently large gap between adjacent states remains. In addition, the endurance characteristics of the 2T0C DRAM cells were evaluated using continuous programming/erasing (P/E) cycles. For programming, $V_{\rm WWL}$ and $V_{\rm WBL}$ were set to 4 and 3 V, respectively. For erasing, $V_{\rm WWL}$ and $V_{\rm WBL}$ were set to 4 and 0 V, respectively. The P/E time was 10 ns. As shown in Figure 1(k), the memory window of $I_{\rm Read}$ is approximately 10^7 and shows no degradation after 10^{11} P/E cycles. Figure 1(l) shows that the DRAM cell still exhibits good retention characteristics after 10^{11} P/E cycles. These results indicate that 2T0C DRAM cells have excellent endurance.

Conclusion. High-performance 2T0C DRAM cells were successfully realized based on ALD IAZO transistors with excellent gate bias stress stability, demonstrating fast write speed (10 ns), long retention time (>18 ks), 3-bit multilevel storage characteristics, and excellent endurance (>10^{11}). These results indicate that the proposed 2T0C DRAM cell based on IAZO transistors is a promising candidate for the M3D integrated DRAM.

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