Supporting Information

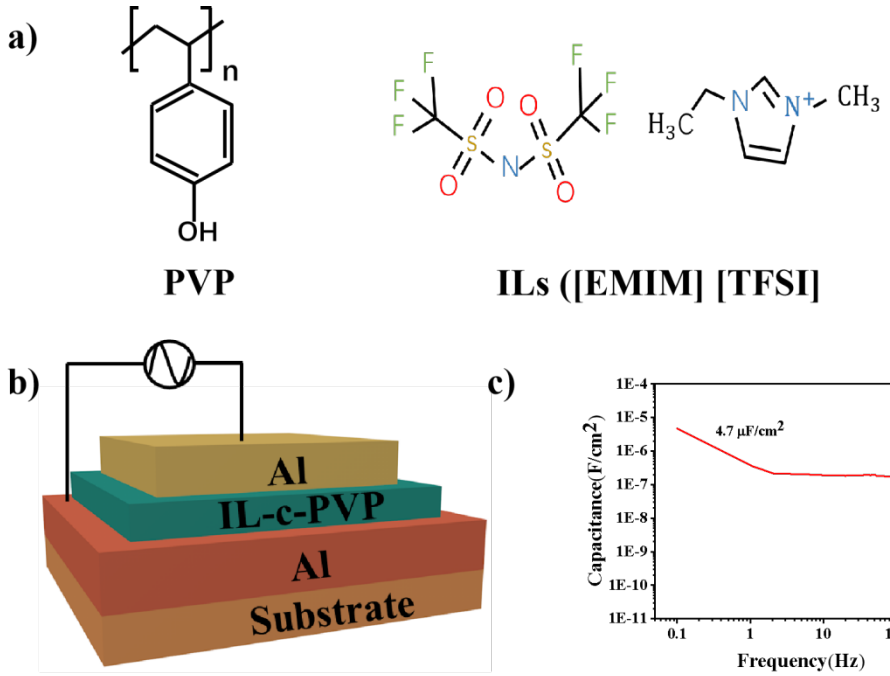

Figure S1 (a) The chemical structures of poly(4-vinylphenol) (PVP) and ILs ([EMIM][TFSI]). (b) The schematic diagram of the areal capacitance measurement for IL-c-PVP dielectrics and (c) the measured capacitance of the dielectric layer per unit area.

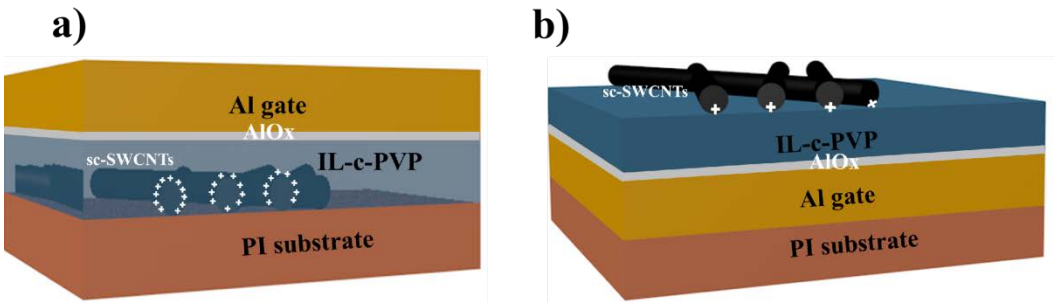

Figure S2 Schematic diagrams of the hole carrier generations and distributions in (g) top-gate and (h) bottom-gate SWCNT TFTs using IL-c-PVP dielectrics with the applied gate voltages.

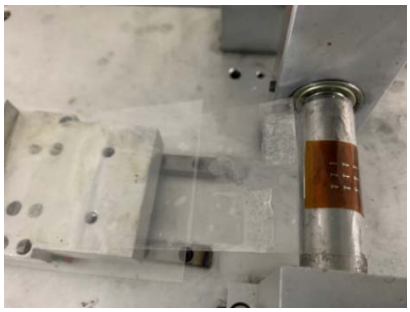

Figure S3 Optical image of the 3D CMOS inverters during the bending test.

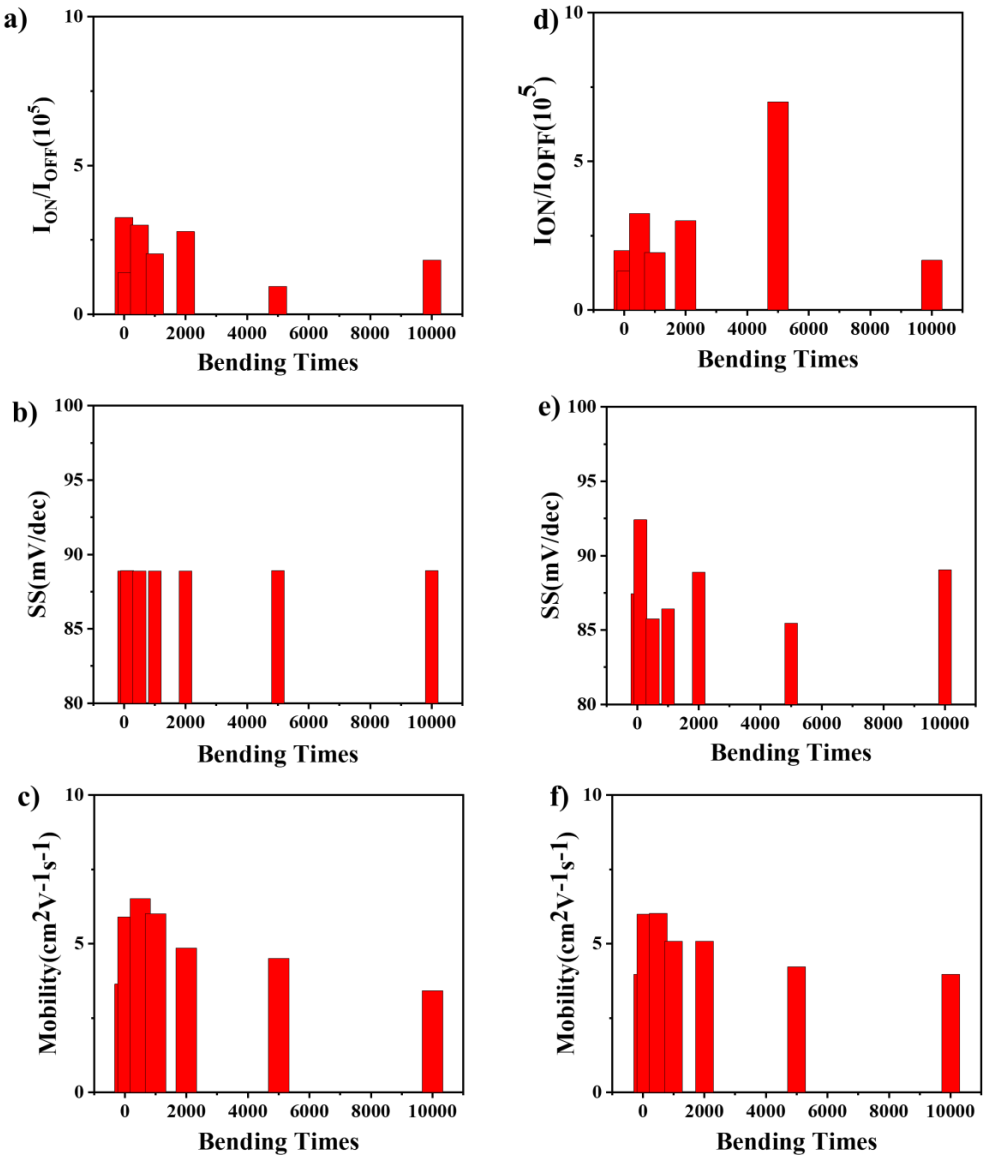

Figure S4 The changes I_{ON}/I_{OFF}, SS and mobility for (a-c) top-gate and (d-f) bottom-gate TFT devices during the course of bending test.

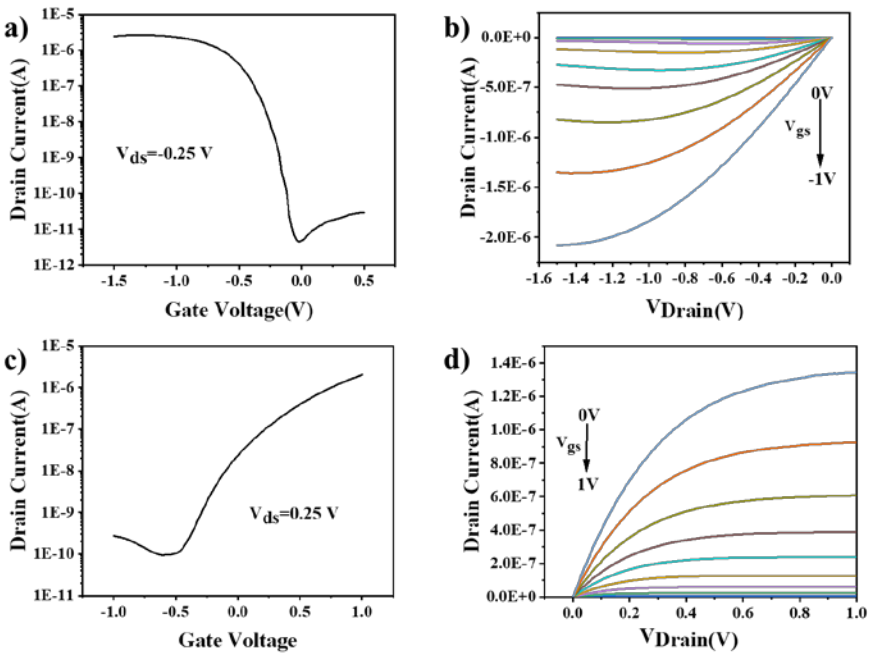

Figure S5 Transfer characteristics and output characteristics of P-type and N-type SWCNT TFT devices.

Table S1. Comparison of electrical properties of P-type SWCNT TFTs.

Log (on/off ratio)	μ_{max} ($cm^2V^{-1}s^{-1}$)	V_{th}(V)	V_{DS}(V)	SS (mV/dec)	Preparation technology	Substrate	Electrode material	Ref
5.5	15.7	-0.2	-0.25	140	Printing	Paper	Ag	10
6	14.9	0	-0.25	73	Printing	PI	Ag	46
6	>10	0.5	-0.25	80	Printing	PET	Ag	11
6	8.9	0.23	-0.25	92	Printing	Glass	Al/Ag	47
5	-	>0	-0.2	120	Evaporation	Si/SiO_2	Ti/Pd/Au	48
5	64.2	>1	-0.5	140	Evaporation	Parylene	Ti/Pd/Au	49
6	**8.54**	**-0.6**	**-0.25**	**61.4**	**Printing**	**PI**	**Al/Ag**	**This work**

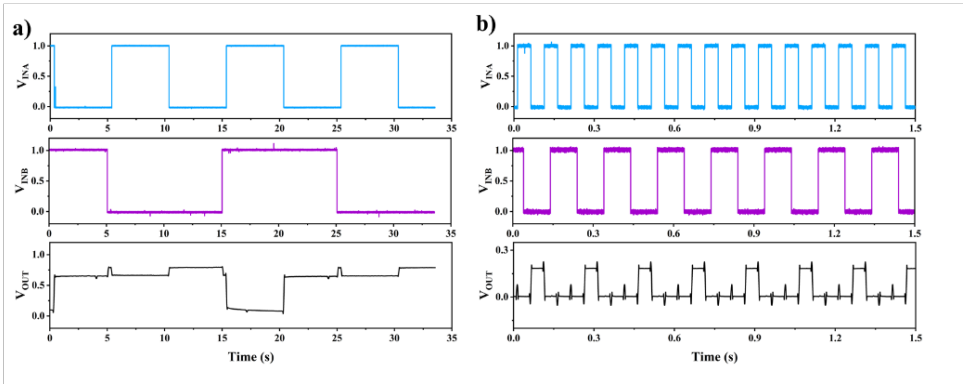

Figure S6 Input and output characteristics of flexible printed (a) NAND and (b) NOR gates.