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High precision current mirror circuit based on two-dimensional material transistors

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The emerging two-dimensional field-effect transistor (2D-FET) is considered an important candidate device for driving future integrated circuit technology toward higher performance, lower power consumption, and more functionalities [1,2]. Among the integrated circuits, analog circuits play a crucial role as they are responsible for sampling, amplifying, and transmitting signals. However, there is a significant challenge in realizing high-performance analog circuits using 2D-FETs, which limits the further development of high-performance integrated circuits based on 2D materials [3,4]. The primary challenge lies in the fact that 2D-FETs have not yet demonstrated ideal output current saturation characteristics and failed to meet the application requirements of analog circuits.

Here, we report excellent output current saturation characteristics with ultrahigh small-signal output impedance, which outperforms all published 2D-FETs. The P-channel field-effect transistor (P-FET) with exceptional output current saturation performance is achieved by utilizing WSe_2 as the channel material. By varying the gate voltage, we can tune the output current from 10^{-11} to 10^{-6} A, and regulate the corresponding small-signal output impedance from 10^{12} to 10^{7} Ω. With these advantages, we can demonstrate a typical high precision current mirror circuit that exhibits a relative current replication error below 16%. This performance surpasses that of a silicon current mirror circuit with a similar device size [5]. This study is the first to demonstrate the superiority of 2D materials in realizing typical analog circuits and may pave the way for developing high-performance integrated analog circuits based on 2D materials.

More information. The 2D semiconductor WSe_2 with excellent hole transport characteristics was selected as the channel material. In order to achieve ideal P-FET characteristics, we developed the device structure shown in Figure 1(a) to suppress the electron transport properties of WSe_2. The device was fabricated on the SiO_2 (300 nm)/Si substrate to facilitate the application of the substrate voltage (V_{sub}). The detailed fabrication and measurement processes of the device are illustrated in Appendixes A and B. During the operation of the device, the source was grounded and the drain-source voltage (V_{ds}) was set to negative. This ensured that the holes (electrons) were transported from the source (drain) to the drain (source). The device contains an asymmetric gate electrode that only overlaps with the source (see Figure 1(a)). As a result, the gate voltage (V_{gs}) can only control the hole injection behavior from the source, without affecting the electron injection from the drain. As for the electron injection, it can be suppressed by setting V_{sub} to −20 V. The detailed working mechanism is illustrated in Appendix C. Consequently, in the WSe_2 channel region, electron transport is successfully suppressed, while the hole transport characteristics can be effectively regulated, resulting in typical P-FET characteristics. In Figure 1(b), typical P-type field-effect transfer curves under different V_{ds} (−1 V, −3 V, and −5 V) of the device are demonstrated, and a $\sim 10^6$ on/off current ratio can be achieved. For the elaborate demonstration of the output current characteristics, we measured the I_{ds}-V_{ds} curves under different fixed V_{gs} (from −1 to −5 V, 0.2 V/step) (see Figure 1(c)). When V_{gs} is fixed, I_{ds} firstly increases linearly with V_{ds} (linear region), and then tends to remain unchanged (saturated region), namely output current saturation behavior. The $|V_{ds}|$ value at the turning point between the linear region and the saturated region increases with the enlarging $|V_{gs}|$. To clearly show the data characteristics at low current levels, we also use $\log I_{ds}$ as the ordinate for plotting the device's output current characteristics (see Appendix D). In order to quantify the saturation characteristics, we linearly fit the data of I_{ds}-V_{ds} within the V_{ds} range of −1 to −5 V (saturated region) with different fixed V_{gs}. Then the small-signal output impedance can be extracted as the reciprocal of the slopes of the fitted lines, shown in Figure 1(d) (corresponding error analysis shown in Appendix E). As V_{gs} increases, the output impedance decreases monotonically. When V_{gs} is −1 and −5 V, the small-signal output impedance is 1.67

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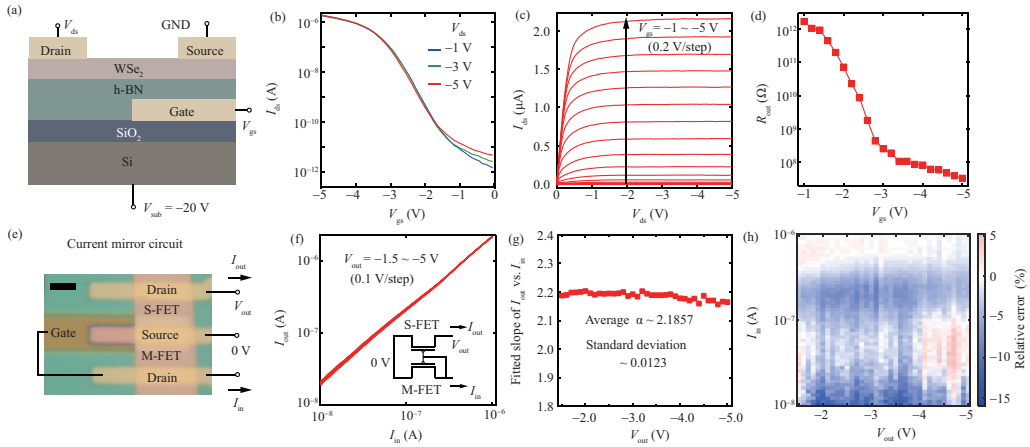

Figure 1 (Color online) (a) Schematic of the device architecture. V_{ds}, V_{gs}, and V_{sub} represent the voltages that are applied to the drain, gate, and substrate, respectively. GND means that the source electrode of the device is grounded. (b) The field effect transfer curves of the device. (c) The output current characteristics of the device. (d) The extracted small-signal output impedance of the device. These data points were extracted as the reciprocal of the slope of the linear fitted lines of current data in Figure 1(c) within the V_{ds} range of -1 to -5 V. (e) The optical image of the current mirror circuit (the scale bar is 3 μm). (f) The measured I_{out}-I_{in} curves of the current mirror circuit (the inset is the circuit schematic of the current mirror). (g) The fitted slope α of I_{out}-I_{in} curves in (f). (h) The relative error between the measured I_{out} and $\alpha \times I_{in}$ ($\alpha = 2.1857$), which can be used to represent the current replication precision of the current mirror.

$\times 10^{12}$ and 3.34×10^{7} Ω, respectively. The proposed device has demonstrated the highest output impedance compared to previously published 2D-FETs, which lays an important foundation for high-performance analog circuits.

As one of the most basic analog circuit elements, the current mirror was chosen to demonstrate the superiority of our device in implementing analog circuit functions. Figure 1(e) and the inset of Figure 1(f) show the optical image of the fabricated current mirror circuit and the corresponding circuit schematic, respectively. The typical current mirror circuit consists of a master FET (M-FET) and a slave FET (S-FET). The source of the M-FET and S-FET is both set to 0 V, and the drain of the M-FET is connected to the gate electrodes of both the M-FET and S-FET. The current I_{in} is input at the drain of the M-FET, and the corresponding output current I_{out} can be measured at the drain of the S-FET. The working mechanism of the current mirror circuit requires that the S-FET should operate in the output current saturation region. Therefore, the output voltage (V_{out}) applied to the drain of the S-FET should be set in the range of -1.5 to -5 V, according to the output current characteristics shown in Figure 1(c). As shown in Figure 1(f), under different V_{out}, the output current I_{out} and the input current I_{in} present an approximately linear relationship, and all the curves overlap. As a result, the circuit demonstrates stable replication performance regardless of the output voltage (V_{out}). The current copy ratio of the circuit (α) can be obtained by fitting the I_{out}-I_{in} curve using the current mirror input-output current relationship ($I_{out} = \alpha \times I_{in}$). In Figure 1(g), the fitted current copy ratio α remains a nearly constant value under different V_{out} from -1.5 to -5 V. According to statistical analysis of the fitting data, the average α of the current mirror is 2.1857 with a very small standard deviation of 0.0123, proving that the current mirror has stable current replication performance. In Figure 1(h), relative error analysis of the current replication process is performed to evaluate the current replication precision of the current mirror (the detailed analysis in Appendix F). The relative error between measured and predicted I_{out} is beneath 16%, which is better than silicon-based current mirror circuits of similar device size [5]. Consequently, the successful demonstration of the high precision current mirror has laid an important foundation for further high-performance analog circuits based on 2D materials.

Conclusion. We first report a 2D material-based P-FET with excellent output current saturation characteristics and demonstrate the highest small-signal output impedance characteristics among all previously published 2D-FETs. Further, we utilize the excellent performance of the device to demonstrate a current mirror circuit, which has better high precision current replication performance than silicon-based devices. This work provides a possible technical approach for the development of high-performance analog circuit devices based on 2D materials.

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Supporting information Appendixes A–F. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Das S, Sebastian A, Pop E, et al. Transistors based on two-dimensional materials for future integrated circuits. Nat Electron, 2021, 4: 786–799
2 Pan C, Shi J W, Wang P F, et al. Polarity tunable complementary logic circuits. Sci China Inf Sci, 2023, 66: 229401
3 Conti S, Pimpolari L, Calabrese G, et al. Low-voltage 2D materials-based printed field-effect transistors for integrated digital and analog electronics on paper. Nat Commun, 2020, 11: 3566
4 Polyushkin D K, Wachter S, Mennel L, et al. Analogue two-dimensional semiconductor electronics. Nat Electron, 2020, 3: 486–491
5 Marani R, Perri A G. CNTFET-based design of current mirror in comparison with MOS technology. ECS J Solid State Sci Technol, 2017, 6: M60–M68