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• **Supplementary File** •

High precision current mirror circuit based on two-dimensional material transistors

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Appendix A The fabrication of the device

The 20 nm thick WSe_2 is selected as the channel material and the 20 nm thick h-BN is selected as the gate dielectric. The WSe_2 (HQ-Graphene, Inc) and h-BN (HQ-Graphene) flakes were prepared onto SiO_2 (300 nm) /Si substrates using the tape mechanical exfoliation technique. The fabrication of vertical heterostructures was done using our home-made micromanipulation displacement system. The source, drain and gate electrodes were fabricated using Cr (5 nm) / Au (40 nm) through the electron beam evaporation process and the standard electron beam lithography process (FEI F50 with Raith pattern generation system).

Appendix B The measurement of the device and circuit

Electrical characterization of individual devices and current mirror circuits using a Keysight B1500A parametric analyzer with Cascade Summit Series Manual and Semi-Automated Probe Systems.

Appendix C The working mechanism of the device

During device operation, the substrate voltage (V_{sub}) regulates the drain region, while the gate voltage (V_{gs}) regulates the source region. As shown in Figure C1, when $V_{ds} < 0$, electrons (or holes) are injected from the drain (or source). In the drain region, the substrate voltage V_{sub} = -20 V lowers the Fermi level, causing the band of the WSe_2 at the drain to bend upward, thereby increasing the effective Schottky barrier height. This enlarged barrier height inhibits the injection of electrons from the drain electrode over the Schottky barrier into WSe_2.
In the source region, the gate voltage V_{gs} can effectively control hole injection. When V_{gs} = -5V (or 0V), the WSe_2 Fermi level in the source region decreases (or increases), causing the band of WSe_2 at the source to bend upward (or downward). Consequently, the effective Schottky barrier height, which dominates hole injection, will decrease (or increase). Thus, holes can (or cannot) be injected into WSe_2 from the source metal electrode.

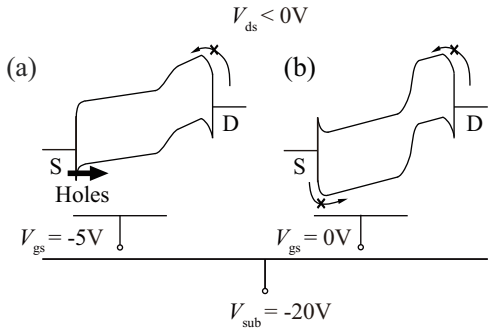

Figure C1 The band diagram of the device under different voltage bias conditions. (a) The device exhibits a hole-transport conduction state; (b) The device exhibits a current cutoff state.

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† Gao S and Pan C have the same contribution to this work.

Appendix D The detailed characteristics of the device's output current curves

To clearly demonstrate the characteristics of the device's output current, particularly the data characteristics at low current levels, we use log I_{ds} as the ordinate for plotting the device's output current characteristics(see Figure D1).

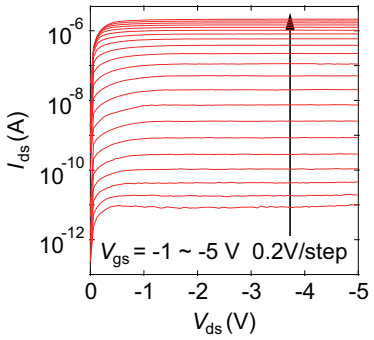

Figure D1 The log I_{ds} is used as the ordinate to perform the output current characteristics of the device.

Appendix E Error Analysis for Extracting Small-signal Output Impedance

The errors between the measured data and the fitted line are shown in Figure E1, and all errors are within 9 %. Based on the above fitting analysis, it is numerically proven that the device exhibits excellent saturation characteristics.

To explain the data processing process more clearly, in Figure E2, we illustrate the method of extracting the small signal output impedance in Figure 1(d) based on the output characteristic curve in Figure 1(c). We also illustrate the process of analyzing the relative error between the measured data and the fitted lines in Figure E1.

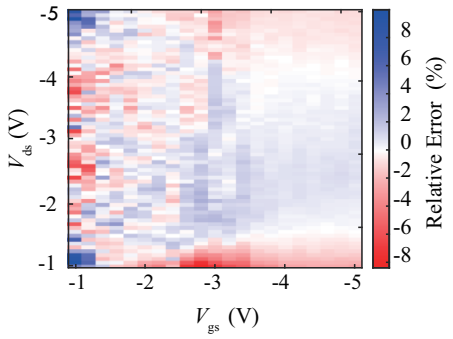

Figure E1 The relative errors between the measured data and the fitted line are based on the output characteristics of the device shown in Figure 1(c).

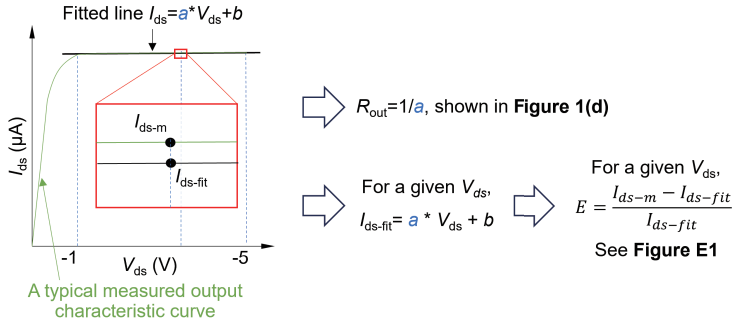

Figure E2 Detailed data analysis process related to Figure 1(d) and Figure E1.

Appendix F Error analysis of current mirror circuit

The root-mean-square error is used to assess the accuracy of the fitting results shown in Figure 1(f). As shown in the Figure F1, the root mean square error between the fitted line and the measured data is distributed between 8×10^{-9} and 16×10^{-9}, proving

that the measured data has very excellent linear characteristics. The detailed process of error analysis is shown in the Figure F2. The error analysis is implemented for the current replication process as follows. According to the working mechanism of the current mirror circuit, the predicted output current ($I_{\text{out-p}}$) is supposed to be equal to $\alpha \times I_{\text{in}}$ (α is the current copy ratio of the circuit), and is not affected by V_{out}. In the proposed circuit shown in Figure 1(e), the α=2.1857 can be measured by fitting the slope of the I_{out}-I_{in} curves as shown in Figure 1(f) and 1(g). Consequently, the relative error between the measured output current $I_{\text{out-m}}$ and $I_{\text{out-p}}$ can be defined as $\text{E}=\frac{I_{\text{out-m}}-I_{\text{out-p}}}{I_{\text{out-p}}} \times 100\%$. Here, $I_{\text{out-p}}=\alpha \times I_{\text{in}}$, $I_{\text{out-m}}$ is measured data under the fixed I_{in} and V_{out}. The result of the analysis is shown in Figure 1h. The detailed process of error analysis is shown in the Figure F2.

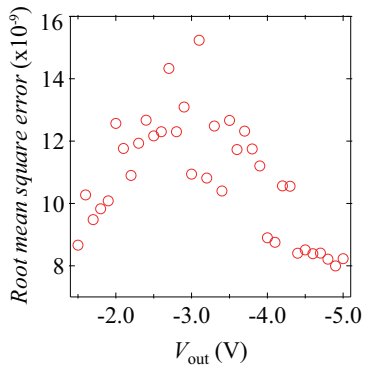

Figure F1 Error analysis of the linear fitted curves in Figure 1(f).

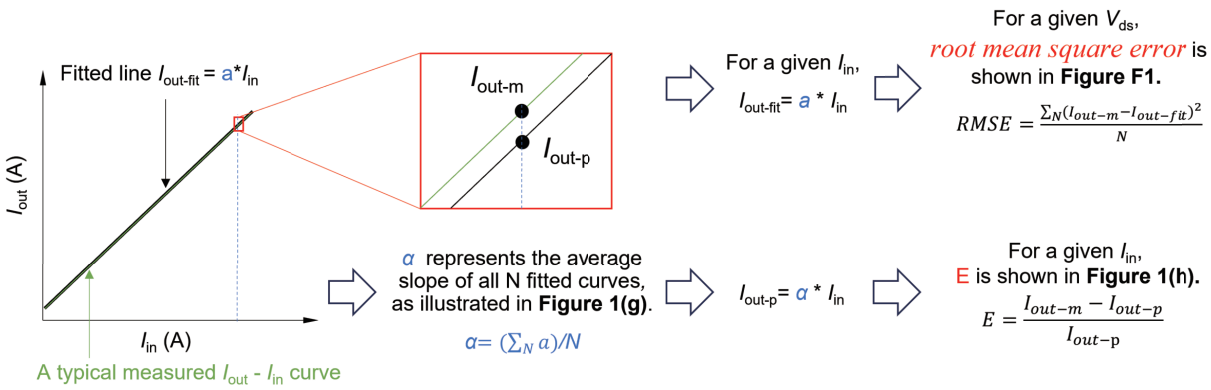

Figure F2 Detailed data analysis process related to Figure F1, Figure 1(g) and (h).