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A 10-GS/s 8-bit 2× time interleaved hybrid ADC with λ/4 reference T-Line sharing technique

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With the recent explosion in interactive machine learning and artificial intelligence, the ultra high-speed wireline or optical data links are evaluated as a crucial device that is handling the ever-growing data traffic in high-performance computing environments [1,2]. In practice, high-order modulation strategies, such as four-level pulse-amplitude modulation (PAM4), enable a significant increase in throughput without raising the baud (Nyquist) rate in transceivers. The bandwidth of the data-acquisition receiver is primarily limited by the radio frequency (RF) sampling frequency of the analog-to-digital converters (ADCs) with 5-6 effective bits of resolution. Time-interleaved (TI) successive approximation register (SAR) ADCs have been extensively employed in virtue of their superior power efficiency [3], in which the input signals are orderly distributed to each single-channel as per the multi-phase sampling clocks. However, the sub-channel sample rate is typically limited to <1 GS/s, necessitating the complicated calibration or randomization techniques to alleviate the mismatch and clock skew of each channel. Recently, time domain ADCs are gaining favor for high-speed applications owing to their superior power efficiency and promising process scaling. The traditional inverter-based time quantization step (T_{LSB}) suffers from device noise and process, supply voltage, and temperature (PVT) variations, which impose constraints on the operational speed of time-domain ADCs [4]. To address the challenges and boost the time-to-digital converter (TDC) speed, a passive λ/4 transmission line (T-Line) based TDC is introduced in [5]. Together with the traveling wave technique, the passive λ/4 T-Line based TDC achieves a sub-picosecond level T_{LSB}, demonstrating excellent PVT robustness. In the on-chip implementation, a pair of the additional reference T-Lines alongside a power-hungry current mode logic (CML) buffer is indispensable in [5], leading to a degeneration in power efficiency.

Strategies and circuit implementation. To mitigate the aforementioned issues of the λ/4 T-Line based TDC, a sharing reference T-Line technique is proposed to enable a significant development in area-power efficiency. A proof-of-concept ADC prototype is fabricated in 1P10M 28-nm CMOS process with 2× time interleaving to achieve 10-GS/s sampling rate with 38.11-dB signal-to-noise and distortion ratio (SNDR) at Nyquist frequency, as illustrated in Figure 1(a). Considering the trade-offs among speed, power consumption, and the noise requirements of voltage-time converters (VTC), the first stage adopts a 3-bit Flash ADC to achieve coarse quantization and generate the small-amplitude voltage-domain residue signal, and then the VTC converts the residue to modulated pulse time-domain signals ($\mathrm{VTC_P}$ and $\mathrm{VTC_N}$) before the next sampling clock CKs arrives. In the subsequent phase, a λ/4 5-bit T-Line based TDC is employed to quantize the $\mathrm{VTC_P}$ and $\mathrm{VTC_N}$ into digital codes. A sharing reference T-Line technique can offer the scale time signals for two interleaving channels, simultaneously. The area and power consumption can be saved by 25% compared to direct 2× interleaving structure. Meanwhile, it also avoids clock crosstalk between the two reference chains.

To optimize the practicality of the λ/4 T-Line based ADC for on-chip implementation, the T-Lines are fed with a high-frequency stable 20-GHz input to reduce the routing length. The power-hungry CML buffer is utilized to ensure the optimal propagation performance (e.g., jitter and amplitude) along with T-Lines [5]. In this work, the CML buffer is replaced by a 5th harmonic injection-locked oscillator (HILO) to improve the power efficiency and jitter performance [6]. With a 3.5-to-4.5 GHz external frequency reference, the 5th HILO can produce a high-frequency clock with a wide swing and low phase noise, tuned from 17.5 to 22.5 GHz after locking. It is worth noting that the output locking range of the HILO can be used to calibrate the parasitic variations and correlation mismatch between silicon validation and EM simulation. Based on the analysis and discussion in [7], the locking range can be expressed as follows:

$$\omega_L \approx \frac{\omega_o}{2Q}.\frac{2}{\pi}.\frac{I_{\mathrm{inj}}}{I_{\mathrm{osc}}}, \tag{1}$$

where ω_o is the frequency of the self-oscillation, I_{inj} is the harmonic current at the frequency of the injected signal harmonic, I_{osc} is the self-oscillation current from the cross-coupled pair and Q represents the quality factor of the resonant cavity. Regarding the HILO, the injected devices generate both fundamental and harmonic current components as specified in

$$i_{\mathrm{Minj}} = a_0 + a_1 v_{\mathrm{in}} + a_2 v_{\mathrm{in}}^2 + a_3 v_{\mathrm{in}}^3 + \cdots + a_n v_{\mathrm{in}}^n, \tag{2}$$

by substituting the 5th harmonic current from (2) into (1),

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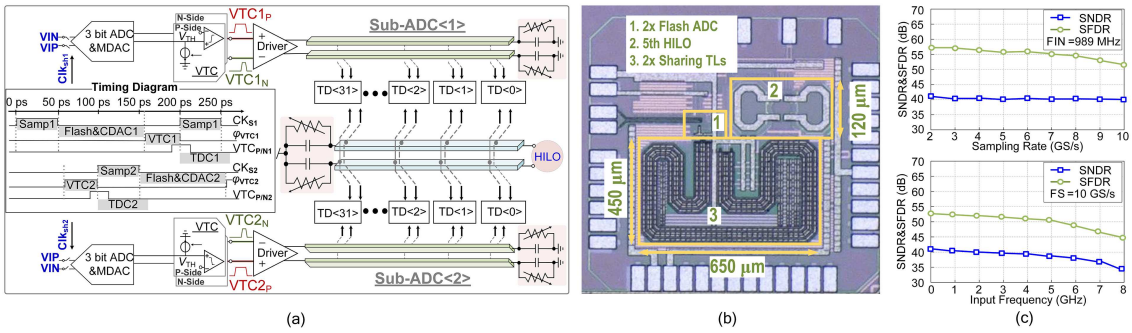

Figure 1 (Color online) (a) The architecture of the ADC; (b) the microphotograph of the proposed ADC; (c) measured SNDR and SFDR versus sampling rates, input frequencies.

we obtain the locking range of the 5th HILO:

$$\omega_L \approx \frac{\omega_o}{2Q}\cdot\frac{2}{\pi}\cdot\sqrt{\frac{\left(a_5 v_{\rm in}^5\right)^2}{\left(I_{\rm osc}\right)^2}} \approx \frac{\omega_o}{2Q}\left|\frac{a_5 v_{\rm in}^5}{I_{\rm osc}}\right|. \tag{3}$$

Reducing the Q value and $I_{\rm osc}$ can lead to the oscillator failing to meet the startup conditions, thus biasing the injection devices to their maximum 5th-order nonlinear region is employed to expand the locking range. The output phase noise follows approximately to the input phase noise by $20\log_{10}(N)$ dB, where N is the ratio of the output frequency to the input frequency, enabling better phase noise performance compared to fundamental frequency oscillators operating at the same frequency. In conjunction with the HILO and the $\lambda/4$ T-Lines, EM simulation is conducted to determine the resonant inductance value of 90 pH, and the Q of 25 is required to generate the 20 GHz center reference frequency, while attaining a wide locking range of 17.5–22.5 GHz. Additionally, directly cascading the HILO with the reference $\lambda/4$ T-Line removes the large size, power-hungry CML buffer and clock receiver, preventing circuit performance degradation caused by interconnecting parasitics and achieving output impedance matching for the oscillator.

Measurement results. The prototype 10-GS/s 8-bit ADC was fabricated in a 1P10M 28-nm CMOS process. Figure 1(b) shows the chip microphotograph, which occupies a core area of 0.324 mm^2 with the $\lambda/4$ T-Lines and HILO. The T-Lines are routed on the top thick layer of aluminum, ensuring the low insertion loss of T-Lines. As observed, a serpentine routing technique is adopted to implement the 2× time interleaved T-Lines alongside the sharing reference T-Lines, aiming to optimize chip area utilization. Meanwhile, symmetrical compensation is utilized for the bends to ensure an equal total path length for signal propagation. This strategy reduces bend curvature, ensuring that delay deviation remains within a few hundred femtoseconds, less than a quarter of the $T_{\rm LSB}$. In order to mitigate electromagnetic coupling, substrate isolation and metal shielding are implemented between the HILO and T-Lines.

Figure 1(c) presents the measured SNDR and spurious-free dynamic range (SFDR) results, showing dependencies on sampling rates at an input frequency of 989 MHz, alongside performance across various input frequencies at a constant sampling rate of 10 GS/s. At a sampling rate of 10 GS/s, the ADC achieves the SNDR of 38.11 dB and the SFDR of 50.23 dB at Nyquist input frequency. Over Nyquist 7.89 GHz input, it still maintains 34.2-dB SNDR and 44.6-dB SFDR. Benefiting from the inherent low-jitter and high-swing properties of the 5th HILO, an enhancement in the overall TDC noise floor is observed. Specifically, at a 5-GS/s sampling rate, SNDR improves by 1.26 dB and SFDR by 5.6 dB compared to the results reported in [5]. At a Nyquist input frequency and a supply voltage of 0.9 V, the core circuit consumes 31.22 mW at 10 GS/s, which corresponds to a Schreier figure of merit (FoM$_{\rm S}$) of 147.14 dB and Walden FoM (FoM$_{\rm W}$) of 47.5 fJ/conversion-step.

Conclusion. A 10-GS/s 8-bit 2× time interleaved hybrid ADC with $\lambda/4$ reference T-Line sharing technique has been demonstrated. Meanwhile, an on-chip 5th HILO with a center frequency of 20 GHz is embedded to generate the low-jitter propagation signal for T-Lines. The proposed sharing reference T-Line technique and serpentine routing enable a significant improvement on silicon-area efficiency. The ADC achieves a measured 3-dB effective bandwidth close to 6.7 GHz and an ENOB exceeding 5.5. The hybrid ADC chip fabricated in 0.9-V 28-nm CMOS achieves a 10-GS/s sampling frequency with a 31.22-mW power consumption. At Nyquist input, the SNDR is 38.11 dB, while at over-Nyquist 7.89 GHz input, the SNDR is 34.2 dB.

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