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A 56 Gb/s DAC-DSP-based transmitter with adaptive retiming clock optimization using inverse-PR-based PD achieving 8-UI converge time in 28-nm CMOS

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With the growing demand for communication bandwidth, transmitters (TXs) are operating at higher rates, compressing the timing margin for the last 4:1 or 2:1 multiplexer (MUX). To alleviate the timing constraints, the retimer is introduced before the last-stage MUX. However, owing to process, voltage, and temperature (PVT) variations, the phase relationship between the retiming clock and the input data is uncertain, leading to insufficient setup and hold time for the successive retimer. Therefore, the retiming clock adjustment techniques are proposed to optimize the timing margin [1,2]. In this study, an adaptive retiming clock selection scheme based on the phase rotator (PR) and inverse-PR-based phase detector (PD) is proposed for high-speed transmitters, ensuring rapid convergence while reducing hardware overhead.

Principle. The proposed retiming clock selection scheme is shown in Figure 1(a) and is compared with prior studies in Appendix A. Existing technologies commonly adopt multiple phase interpolators (PIs) or PRs plus finite state machine (FSM), requiring hundreds of unit interval (UI) to arrive at the steady state [1,2]. To address the issues of convergence time and hardware overhead, the proposed retiming clock selection scheme first detects the phase differences between the rising edge of data-synchronized clock (CK_8) and the original recovered phase clock (CK'_4), generating the corresponding pulse signals, where CK_N stands for $1/N$ baud rate clock. By comparing the widths of these pulse signals, the optimal clock phase is selected for retiming. Since the phase relationship between CK_8 and CK'_4 can be determined by a single comparison, only one CK_8 cycle (8 UI) is required for the clock selection. Furthermore, the proposed scheme increases a few hardware overheads, featuring only 12 D flip-flops (DFFs) and 8 MUXs.

Implementation. The architecture of the proposed retiming clock selection scheme is shown in Figure 1(b), consisting of two essential blocks, i.e., the retiming clock selector and the Inv-PR PD. The phase differences between CK_8 and CK_{4_PR} are converted into the widths of the low-level of the PW signals (PW_0 to PW_{270}). The pulse widths of these PW signals are subsequently compared by NAND-gates-based comparators. The comparison results between PW_{OUT1} and PW_{OUT2} are encoded into SEL_1 and SEL_2, selecting the clock with the 2nd-longest pulse width as the retiming phase. Thanks to the proposed clock selection scheme, the retimer exhibits a setup time of at least 2 UI and a hold time of 1 UI. As 1 UI is 35 ps for 28 Gbaud/s, there is enough timing margin for retiming. The falling edge of CK_8 consistently samples the results, avoiding the PR control codes toggling during phase detection. Furthermore, a logic is designed to eliminate metastability by controlling LOCK_SYN. The timing and eye diagrams in Appendix B illustrate the operation and effectiveness of the proposed retiming scheme.

The selector employs a PR to shift the order of 4-phase divided clocks (CK_4) to optimize the retiming clock. Note that the proposed PD first employs an Inv-PR to recover the initial phase (CK'_{4_PR}), ensuring the stability of the detection results. Subsequently, the phase differences between CK_8 and CK_4 are detected by two tri-state phase/frequency detectors (PFDs). Since the conventional PFD fails when its two inputs operate at different frequencies (CK_4 and CK_8), CK_8 is adopted as an extra reset signal.

As a prototype, a DAC-DSP-based transmitter with the PR + Inv-PR PD-based retiming scheme is implemented. It consists of 7-bit digital-to-analog converter (DAC), clock path, and digital signaling processor (DSP) for pattern generation, feedforward equalizer, and encoding, which is detailed in Appendix C. The TX is fabricated in 28 nm CMOS technology where Figure 1(c) shows the die photo. The area for clock path, DSP, serializer, and DAC are 0.01, 0.1, 0.07, and 0.03 mm^2, respectively. Note that the proposed PD only occupies 1473 μm^2 extra area.

Measurement. The adaptive retiming clock optimization is measured by a real-time oscilloscope, as shown in Figure 1(d). The falling edge of RST is used as the trigger to capture a retiming clock optimization process. Note that data is synchronized with CK_8, and it is expected that the rising edge of CK_{4_PR0} is located in the center of the stable

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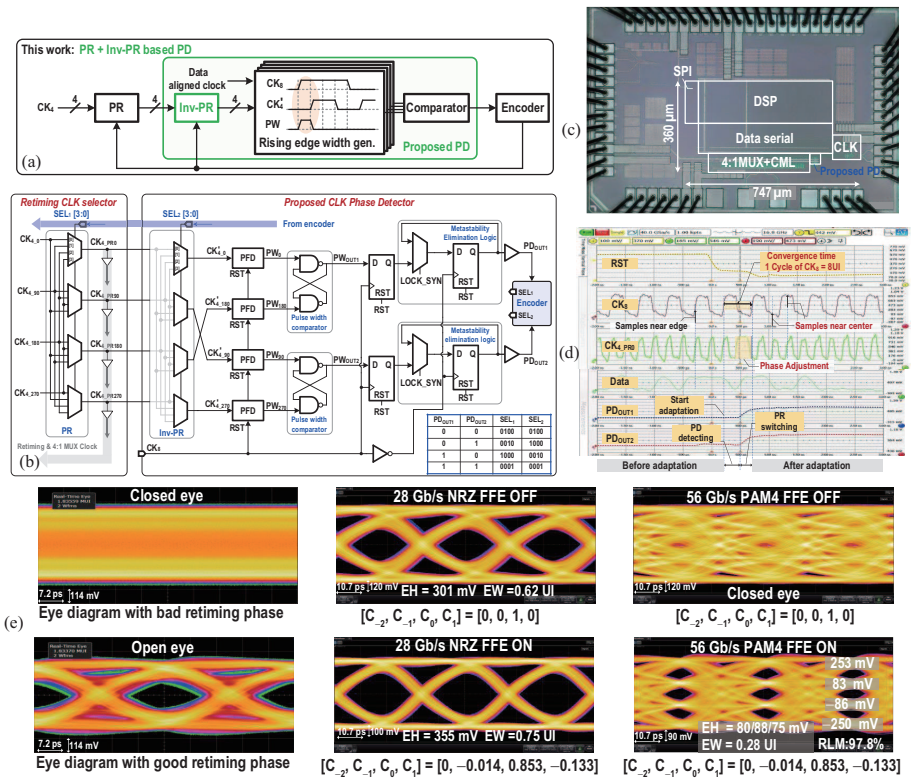

Figure 1 (Color online) (a) Proposed adaptive retiming clock scheme; (b) schematic of the proposed retiming clock selection scheme; (c) die micrograph of the TX prototype; (d) measured adaptive retiming timing diagram; (e) measured eye diagrams of the TX prototype.

level of CK_8 to obtain more timing margin. Before adaptation, the edges of CK_{4_PR0} and CK_8 are close to each other, which is not desired. When the rising edge of CK_8 comes after the falling RST, the loop starts working. As shown in Figure 1(d), the PD detecting consumes half a cycle of CK_8. Afterwards, PD_{OUT1} and PD_{OUT2} jump, indicating that the phase re-selection is completed. It can be observed that CK_{4_PR0} has phase adjustments in the PR switching period. After that, the rising edge of CK_{4_PR0} is located in the center of CK_8 high/low level, providing a larger timing margin.

The output of TX is measured by a sample oscilloscope, the test setup is detailed in Appendix D. Eye diagrams in bad and good retiming clock phases are shown at the top of Figure 1(e), verifying the effectiveness of the proposed adaptive retiming scheme. Afterwards, four measured eye diagrams are presented to show the effect of feed-forward equalizer (FFE) for the non-return-to-zero (NRZ) and the four-level pulse amplitude modulation (PAM4) signaling. For the NRZ mode with FFE enabled, the eye height and eye width exhibit an increase of 17.9% and 20.9%, respectively. In the case of PAM4 signaling, the eye diagram is closed when FFE is turned off. With appropriate equalization, the eye diagram achieves 80/88/75 mV eye heights and 0.28 UI eye widths, achieving the RLM of 97.8%. The measured power consumption is 164.5 mW at 56 Gb/s PAM4 signaling. Compared with other studies, the proposed retimed clock scheme shows the fastest convergence speed of 8 UI with only 2.8 mW and 1473 μm^2 extra power and area, respectively, as shown in Appendix E.

Conclusion. This work presents an adaptive clock optimization scheme for TX to alleviate the timing constraints for the retimer. Using the PR and inverse-PR-based phase detector, the optimal clock phase is selected for retiming with only 8 UI convergence time. By adopting the proposed technique, we realize a 1–56 Gb/s DAC-DSP-based TX in 28-nm CMOS. Measurement results show that the rising edge of retiming clock is located in the center of data when the phase adjustment completed. The total TX consumes 164 mW at 56-Gb/s PAM4 signaling with 97.8% RLM in 0.25 mm^2 area. Therefore, the proposed retiming clock optimization scheme is a promising scheme for high-speed TX.

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Supporting information Appendixes A–E. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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