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• **Supplementary File** •

A 56 Gb/s DAC-DSP-based transmitter with adaptive retiming clock optimization using inverse-PR-based PD achieving 8-UI converge time in 28-nm CMOS

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Appendix A Comparison of the adaptive retiming clock scheme

As shown in Figure A1, [1] employed a DFF-based phase detector (PD) along with two phase interpolators (PIs) for the retiming clock adjustment. Whereas, the two PIs increase the hardware cost, and the traversal of 7bit-PI also enlarges the convergence time. A simplified scheme entails clock phase adjustment through a phase rotator (PR) to shift the order of the 8-phase clocks and select one of them as the retiming clock. Compared with the PI-PD scheme, it reduces the hardware complexity at cost of the precision [2]. Notice that both of PI and PR are controlled by the finite state machine (FSM) according to the results of the PDs, which limits the convergence speed.The proposed adaptive retiming clock scheme only need 12 DFFs and 8 MUXs, achieving 8-UI convergence time.

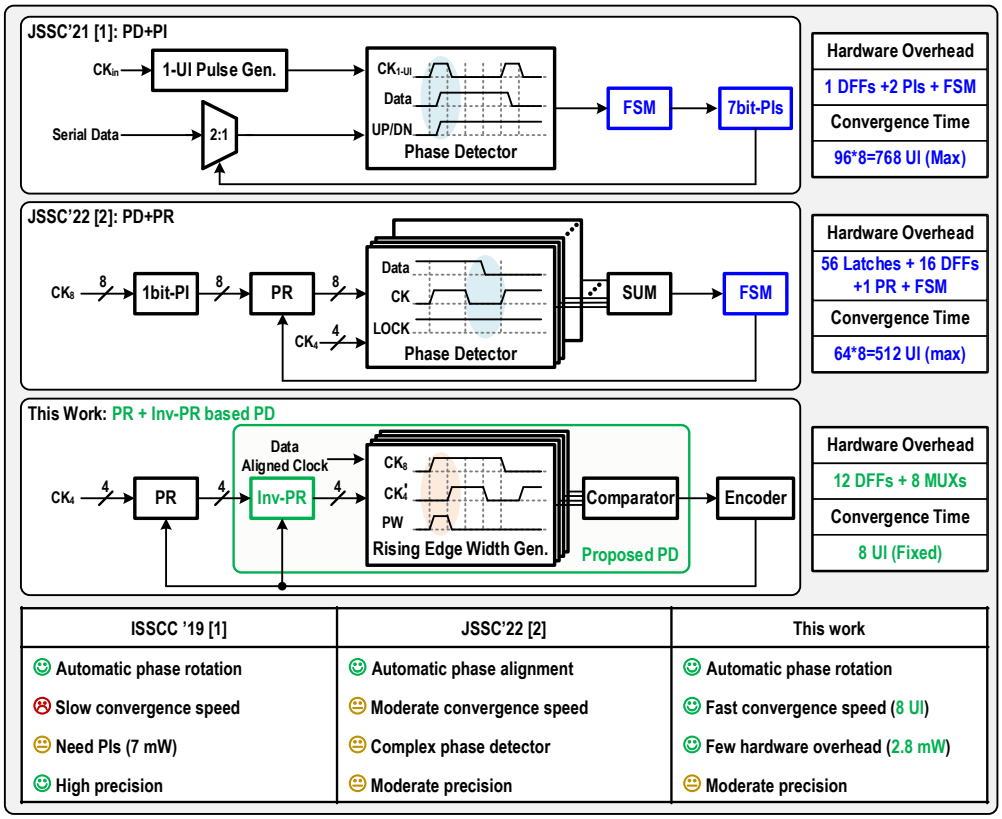

Figure A1 Comparison of different adaptive retiming clock schemes.

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Appendix B Simulated results and analysis of the adaptive retiming clock scheme

Simulated timing and eye diagrams are shown in Fig. B1, verifying the proposed scheme. In the 1st phase, the insufficiency setup time (T_{SETUP}) results in a distorted eye diagram. Differently, when the retiming clock adjustment completed within 8UI, plentiful T_{SETUP} relaxes the timing constraints and leads to an open eye diagram (2nd phase), as shown in Figure B1(b).

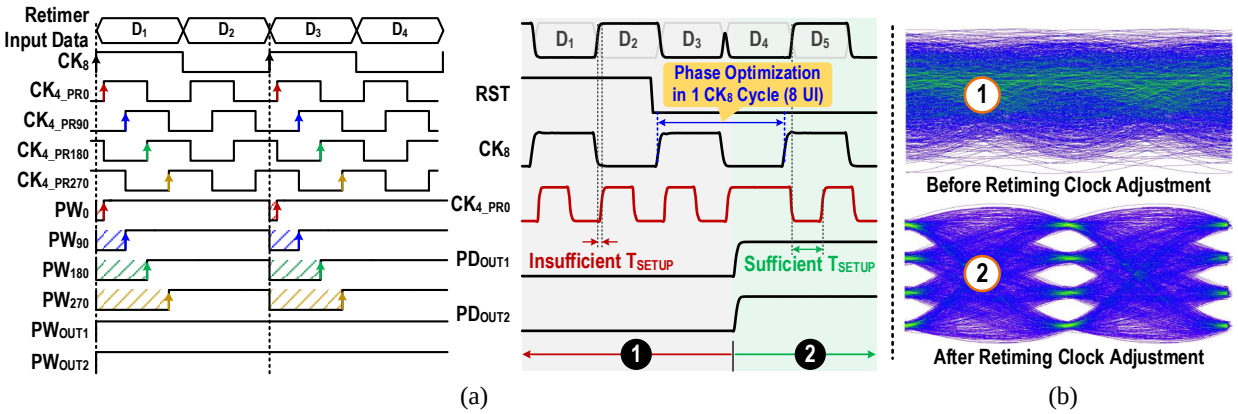

Figure B1 (a) Timing diagram of the proposed retiming clock selection scheme; (b) Simulated eye diagrams of the TX output before and after retiming clock adjustment.

Considering two extreme cases CK_{4_PR0} and CK_8 are almost aligned but PW_0 are judged as the shortest and longest pulse width respectively, which is shown in Figure B2. For the case in Figure B2(a), CK_{4_PR180} corresponds to the 2^{nd}-longest pulse with about 2UI setup time and hold time. CK_{4_PR270} corresponds to the 2^{nd}-longest pulse with about 3UI setup time and 1UI hold time for the case in Figure B2(b). As for 28 Gbaud, 2UI corresponds to 71.4 ps, hence there is enough timing margin for retiming.

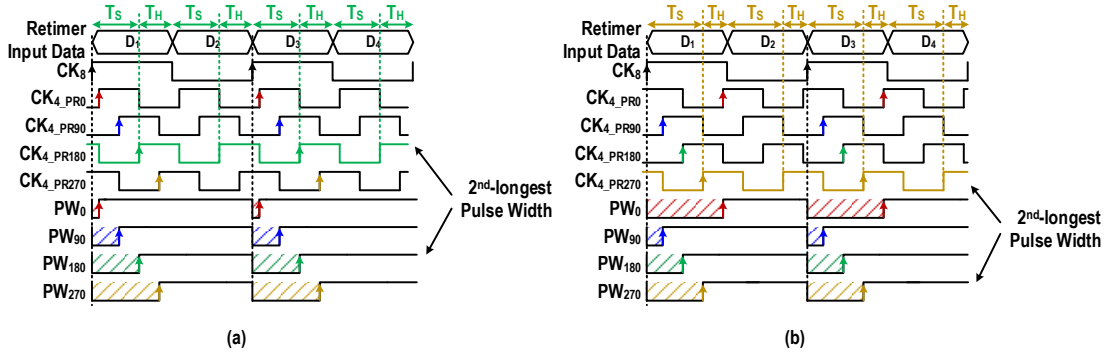

Figure B2 Timing diagram of two extreme conditions of the proposed technique; (a) CK_{4_PR0} phase lags behind CK_8; (b) CK_{4_PR0} phase leads ahead CK_8.

In practical fabrication, the 1/8-rate clock located at retimer (CK_8) and that located at PD (CK_{8_PD}) may suffer from clock skew due to the parasitic delay, as shown in Figure B3, which is based on the two cases presented in Figure B2, respectively. In the case of Figure B3(a), T_D should be less than 2UI-T_{SR} since T_{SR}+T_D=2UI, where T_D represents CK_8 parasitic delay and T_{SR} represents the minimum setup time required by the retimer DFF. For the other case in Figure B3(b), T_D should be less than 1UI-T_{HR} since T_{HR}+T_D=1UI, where T_{HR} represents the minimum hold time required. Considering the two cases, the proposed technique could ensure enough timing margin as long as the parasitic delay is less than min{2UI-T_{SR}, 1UI-T_{HR}}.

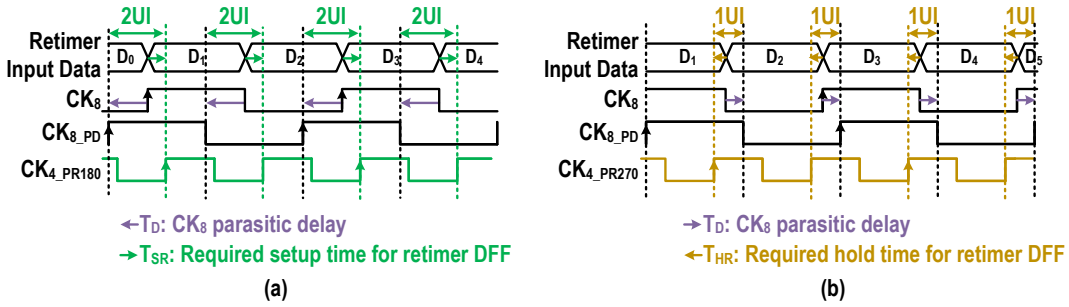

Figure B3 Timing diagram with parasitic delay; (a) CK_{4_PR0} phase lags behind CK_8; (b) CK_{4_PR0} phase leads ahead CK_8.

Appendix C Overall architecture

Figure C1 shows the overall architecture of the proposed TX. The clock path receives a half-rate CML clock, and then divides it to produce quadrature 1/4 baud rate clocks (CK_4). Afterwards, CK_4 will be buffered into two parts, one of which are differential clocks sent to the next stage divider to generate sub-rate clocks. The other part is the 4-phase clocks used for the retimer and 4:1 MUX after the PR. The design of the replication clock avoids the phase variation of CK_4 that may crash the successive circuits. The rotated 4-phase clocks will pass through duty-cycle error corrector (DCC) and quadrature-error corrector (QEC) based on current-starved inverter, compensating for the error introduced by the PR. CK_{8_PR} is a replication of CK_8, matching data path delay to ensure the detection accuracy of the PD. As for the data path, PRBS generators produce 64-channel parallel data to the feed-forward equalizer (FFE). The FFE is based on lookup tables with 4-tap configurable coefficients, supporting both NRZ and PAM4 signaling. The 64 parallel data are converted to 32 symbols by combining 2 bits into 1 symbol. The quantization bit width of the FFE is 7, in which the most two significant bits are coded from binary to 3-bit temperature code for better linearity. Each slice of the data path involves a 32:4 serializer, a retimer, a 4:1 MUX, and a CML output driver consisting of 3 temperature code plus 5 binary weighted segments.

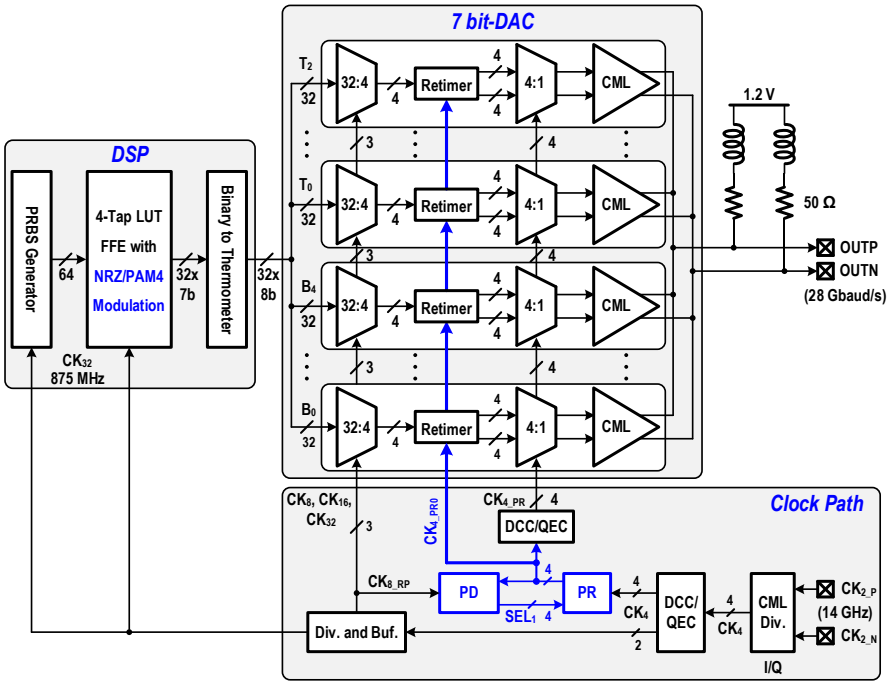

Figure C1 Overall architecture of the proposed TX.

Appendix D Measurement setup

The block diagram and test platform are shown in Figure D1 (a) and (b), respectively. The TX differential outputs are connected to the sampling oscilloscope (Keysight N1094B) via a pair of 2.92-mm connectors, 0.8-m cables, and DC blocks. A half-baud-rate clock is forwarded from the Rohde & Schwarz SMA 100B RF and microwave signal generator. It is distributed to the proposed TX and the sampling oscilloscope by two baluns. Besides, an FPGA is used to control the on-chip SPI for the DSP configuration.

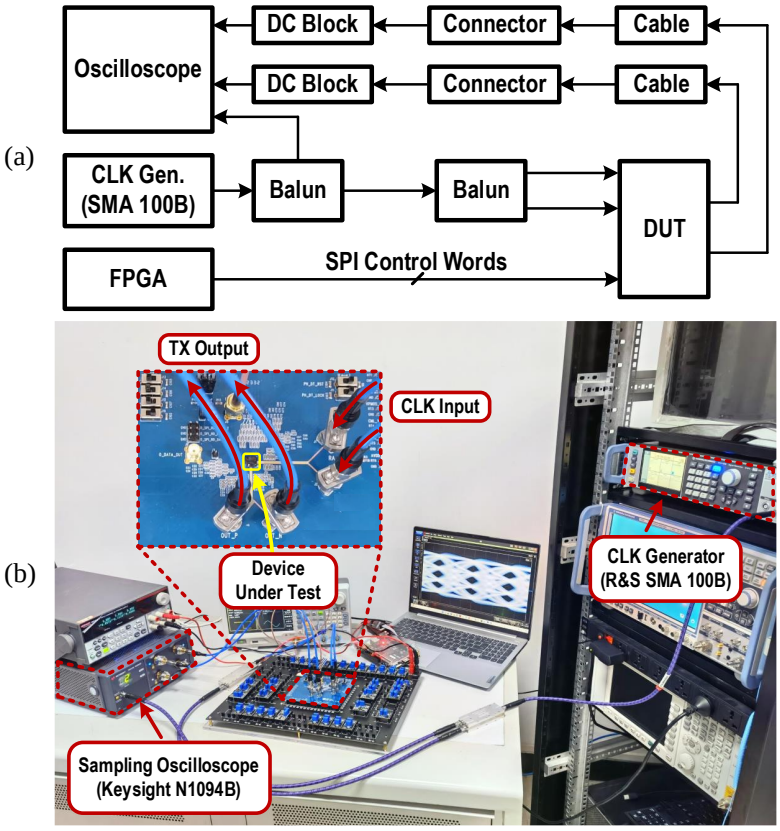

Figure D1 Test setup for the proposed TX.

Appendix E Performce comparison

Table E1 Performance comparison with previous works

	ISSCC'20 [4]	JSSC'19 [3]	JSSC'22 [5]	JSSC'22 [6]	JSSC'22 [2]	JSSC'21 [1]	This Work
Architecture	DAC-DSP	Analog	DAC-DSP	Analog	DAC-DSP	Analog	**DAC-DSP**
Retiming Clock Scheme	PR	N/A	PI+DCDL	PI+DCDL	PD+PR	PD+PI	**PD+PR**
Automatic Retiming Adjustment?	No	N/A	No	No	Yes	Yes	**Yes**
Overhead of Automatic Retiming Clock	N/A	N/A	N/A	N/A	56 Latches + 16 DFFs + 1 PR + FSM	1 DFFs + 2 PIs + FSM	**12 DFFs + 8 MUXs**
Retiming Clock Convergence Time	N/A	N/A	N/A	N/A	*512 UI (Max)	*768 UI (Max)	**8 UI (Fixed)**
Data Rate (Gb/s)	100	64	56	200	224	112	**1-56**
FFE Taps	8	4	2	5	8	4	**4**
Modulation	NRZ	PAM4/NRZ	PAM4/NRZ	PAM4/NRZ	PAM2/4/8	PAM4/NRZ	**PAM4/NRZ**
Output Driver	CML(tailless)	SST	CML	CML	CML	SST	**CML**
Power (mW)	619	135	93	926	390	436	**164.5**
Efficiency (pJ/bit)	6.19	2.1	1.73	4.63	1.74	**3.89	**2.94**
Technology (nm)	40	28	40	28	10	40	**28**
Area (mm^2)	0.504	0.12	0.468	0.4323	0.0875	0.56	**0.25**

* Estimated from the papers. ** With on-chip clock.

References

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2 Kim J, Kundu S, Balankutty A, et al. A 224-Gb/s DAC-based PAM-4 quarter-rate transmitter with 8-tap FFE in 10-nm FinFET. IEEE J Solid-State Circ, 2022, 57: 6-20

3 Depaoli E, Zhang H, Mazzini M, et al. A 64 Gb/s low-power transceiver for short-reach PAM-4 electrical links in 28-nm FDSOI CMOS. IEEE J Solid-State Circ, 2019, 54: 6-17
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5 Peng P J, Lee P L, Huang H E, et al. A 56-Gb/s PAM-4 transmitter/receiver chipset with nonlinear FFE for VCSEL-based optical links in 40-nm CMOS. IEEE J Solid-State Circ, 2022, 57: 3025-3035
6 Wang Z, Choi M, Lee K, et al. An output bandwidth optimized 200-Gb/s PAM-4 100-Gb/s NRZ transmitter with 5-tap FFE in 28-nm CMOS. IEEE J Solid-State Circ, 2022, 57: 21-31