SCIENCE CHINA
Information Sciences

• LETTER •

August 2024, Vol. 67, Iss. 8, 189401:1–189401:2
https://doi.org/10.1007/s11432-024-4079-x

A column-shared histogramming TDC with pixel-to-pixel coincidence detection and compact analog counters for Flash LiDAR sensor

Haoran WU[1,2], Kaiming NIE[1,2*], Jiangtao XU[1,2], Qinglong LIN[1,2] & Yingying JIAO[1,2]

[1]*School of Microelectronics, Tianjin University, Tianjin* 300072*, China;*
[2]*Tianjin Key Laboratory of Imaging and Sensing Microelectronic Technology, Tianjin* 300072*, China*

Received 20 January 2024/Revised 20 March 2024/Accepted 15 June 2024/Published online 10 July 2024

In recent years, Flash LiDAR sensors based on direct time-of-flight (DToF) have been playing an increasingly important role in various 3D imaging fields. In order to perform a histogram on the chip to reduce the data rate, it is inevitable to use a large-size histogramming time-to-digital converter (hTDC) in a Flash LiDAR sensor. However, a large-size hTDC limits the spatial resolution of the sensor. The successive approximation method [1] and quaternary searching method [2] have been proposed to reduce the number of memories in hTDC. However, due to the large area of the digital counter, the area of the proposed hTDC in [1, 2] is still too large.

In this study, we propose a column-shared hTDC based on pixel-to-pixel coincidence detection and compact 9-bit analog counters to reduce the pixel area and improve the resolution of the DToF sensor. The column-shared architecture eliminates the need for additional comparators and memories in pixels. The proposed pixel-to-pixel coincidence detection technology makes each pixel only need one single photon avalanche diode (SPAD), rather than multiple SPADs. The proposed analog counter has a high dynamic counting range without large capacitance. Through the above two techniques, the pixel size is only 36 × 36 μm.

Architecture of the proposed hTDC. The architecture of the proposed hTDC is shown in Figure 1(a). The pixel contains a SPAD, quenching and monostable circuit, pixel-to-pixel coincidence detection circuit, two analog counters and a window generator. The column ADC is composed of a three-stage comparator, a 9-bit digital counter and a 15-bit memory. The quenching and monostable circuit is used to shape the output of SPAD and output a narrow pulse. And then the pixel-to-pixel coincidence detection circuit is used to convert narrow pulses from different pixels into serial output pulses and filter out background light noise. The window generator is used to provide a pulse counting window, and the analog counter is used to receive pulses in different windows and perform counting operations. After the counting of the analog counter is completed, the column ADC quantizes the voltage of the analog counter for each pixel row by row, and then the memory stores the digital codes and reads them out. Since there is no additional area consumption caused by ADC and memories in each pixel, and thanks to the application of pixel-to-pixel coincidence detection and analog counters, the proposed architecture can better reduce the pixel area. The quantization method of hTDC is divided into two stages: coarse quantization and fine quantization. Coarse quantization is based on successive approximation, and fine quantization is based on phase detection technology. The specific quantification method is given in Appendix A.

Pixel-to-pixel coincidence detection. The circuit of pixel-to-pixel coincidence detection is shown in Figure 1(b). First, each pixel has a SPAD, which is connected to a quenching circuit. The monostable circuit is connected after the quenching circuit, thereby shortening the pulse width generated by the quenching circuit. This is to enable the subsequent coincidence detection circuit to receive more pulses. Then, the coincidence detection circuit of each pixel will receive not only the pulse given by its own monostable circuit, but also the pulse signal given by the monostable circuit of four adjacent pixels. The pixel-to-pixel coincidence detection circuit converts the parallel input pulses from different pixels into a serial output signal $\mathrm{SiPM_L}$ through a NAND gate. Thanks to the application of this technology, only one SPAD is needed in each pixel without multiple SPADs, which greatly reduces the pixel area.

9-bit compact analog counter. The digital counter used in hTDC usually causes huge area consumption. Therefore, an analog counter with a smaller area can be used instead of a digital counter. The charge-injection analog counter is proposed in [3]. It has good linearity and anti-noise performance, but there are still additional charge Q_{L} leakage caused by high-level path, and charge Q_{I} caused by charge injection and clock feedthrough. Then the actual counting step ΔV_{O} of this structure can be calculated as

$$\Delta V_{\mathrm{O}} = \frac{C_1}{C_2} \times (V_{\mathrm{DD}} - V_{\mathrm{REF}}) + \frac{Q_{\mathrm{L}} + Q_{\mathrm{I}}}{C_2}. \qquad (1)$$

In order to reduce the area of the analog counter, it is necessary to reduce the charge Q_{L} and charge Q_{I}, so that the area of the capacitor C_2 can be reduced. The improved charge injection structure is shown in Figure 1(c). On the basis of the switches S_1 and S_2, a switch S_3 is added. The

* Corresponding author (email: nkaiming@tju.edu.cn)

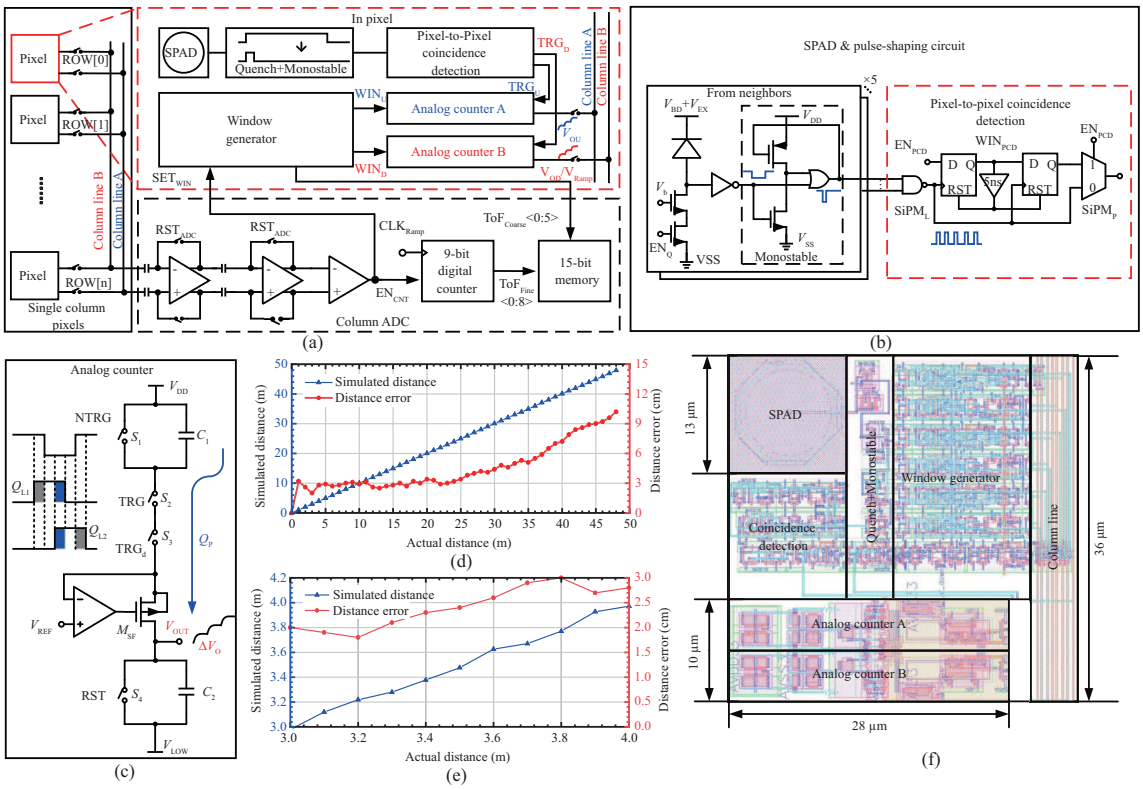

Figure 1 (Color online) (a) Architecture of the proposed hTDC; (b) schematic of SPAD and pulse-shaping circuit; (c) schematic of the proposed analog counter; (d) distance error of the proposed hTDC from 1 to 48 m under 30 klux background light intensity; (e) distance error of the proposed hTDC from 3 to 4 m under 30 klux background light intensity; (f) layout of the proposed hTDC.

control signals of S_1 and S_2 are unchanged, and the control signal $\mathrm{TRG_d}$ of S_3 is obtained by NTRG through an inverter. When the control signal TRG of S_2 is low level, both ends of the capacitor C_1 are reset to V_{DD}. When S_2 receives the pulse signal, S_1 and S_2 are connected and S_3 is disconnected. After a delay, while S_2 and S_3 are connected, S_1 is disconnected and the charge Q_{P} is transferred from C_1 to C_2. Finally, when S_1 and S_1 are connected, S_2 is disconnected. By the switch S_3, even if two of the switches are still connected at the same time due to the delay, there must be another switch disconnected, so that the charges Q_{L1} and Q_{L2} are blocked. In order to eliminate the influence of charge injection and clock feed-through, complementary CMOS switches are used in S_1, S_2 and S_3. For the auxiliary amplifier, the bias current is set to 3 μA, and the DC gain is 35 dB. In order to achieve 9-bit linearity, C_1 is set to 1 fF, C_2 is set to 150 fF, and V_{REF} is set to 3 V. After simulation, the counting step ΔV_{O} is about 2.098 mV. In addition, for the transistor M_{SF}, the substrate and source are shorted to eliminate the influence of V_{th} change on the output, so as to improve the linearity.

Simulation results. The proposed hTDC is designed and simulated in a standard 110 nm CMOS process. All simulation results are based on post-simulation. The layout of the single pixel is shown in Figure 1(f). The size of a pixel is only 36 × 36 μm. The size of the single 9-bit analog counter is 28 × 5 μm, which is a relatively small area consumption. The simulation results of the distance error are shown in Figures 1(d) and (e). It is shown that when the background light intensity is 30 klux, the maximum distance error is 10.6 cm, and the distance accuracy is about 0.22% in Figure 1(d). It is shown that the distance error of fine quantification is 3 cm corresponding to the accuracy of 200 ps in Figure 1(e). The specific simulation is given in Appendix C.

Conclusion. This study presents a column-shared hTDC with pixel-to-pixel coincidence detection and compact analog pulse counters. The column-shared architecture allows the hTDC to have no large area consumption caused by ADC and memories in pixels. Thanks to the pixel-to-pixel coincidence detection, only one SPAD is needed in each pixel. The application of the analog counter greatly reduces the area occupied by the counter. The simulation results show that the proposed hTDC can effectively reduce the pixel area while ensuring accuracy under high background light conditions, so it is suitable for outdoor applications.

Acknowledgements This work was supported by National Key R&D Program of China (Grant No. 2022YFB2804401).

Supporting information Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Kim B, Park S, Chun J, et al. A 48 × 40 13.5mm depth resolution Flash LiDAR sensor with in-pixel zoom histogramming time-to-digital converter. In: Proceedings of IEEE International Solid-State Circuits Conference, 2021. 108–110
2 Park S, Kim B, Chun J, et al. An 80 × 60 Flash LiDAR sensor with in-pixel histogramming TDC based on quaternary search and time-gated Δ-intensity phase detection for 45m detectable range and background light cancellation. In: Proceedings of IEEE International Solid-State Circuits Conference, 2022. 98–100
3 Park B, Park I, Park C, et al. A 64 × 64 SPAD-based indirect time-of-flight image sensor with 2-tap analog pulse counters. IEEE J Solid-State Circ, 2021, 56: 2956–2967