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A wide load-range OTA using a digitally assisted compensating technique

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To keep pace with rapid advancements in high-quality liquid crystal displays (LCDs), there has been a growing focus on the development of low-power, high-speed output drivers in recent years. An LCD column driver typically compromises registers, data latches [1], digital-to-analog converters [2], and output buffers. Among these core building blocks, the performance of the entire driver largely depends on the output buffers, which are implemented using transconductance amplifiers (OTAs). These factors strongly determine the performance of the entire driver in terms of speed, resolution, voltage swing and power dissipation. Furthermore, OTAs should be able to drive capacitors across a wide range to handle the glitch energy produced during the digital-to-analog conversion. The increasing demand for LCD panels with high color depth and resolution further complicates the OTA, particularly for applications that require varying the load capacitance by several orders of magnitude (from pF to nF). To address these requirements, the OTA usually calls for high open-loop gain and rail-to-rail features, leading to widespread use of multistage amplifier architectures.

Ensuring closed-loop stability of multistage OTAs across a broad range of C_L is crucial. Recent advances have focused on compensating topologies based on frequency compensation. Although these approaches can maintain closed-loop stability at a maximum load range of 500×, they lead to significant fluctuations in settling time as a function of C_L. This variation is quantified using settling time drifts (STDs), calculated as $t_{\mathrm{setmax}}/t_{\mathrm{setmin}}$, where t_{setmax}, t_{setmin} refer to the maximum and minimum settling times, respectively. Notably, fluctuating STDs deteriorate the frame rate of an LCD panel and affect human color vision. To suppress performance degradation as C_L increases, researchers have sought to enhance the slew rate (SR) and gain bandwidth product in single-stage OTAs. These topologies offer small STDs and enhanced energy efficiency but are limited to a load-range expansion of only 10× owing to either the high-Q conjugate poles from intrinsic parasitic capacitance or the finite current set by the analog output stage.

This study presents a multistage amplifier that leverages a digitally assisted compensating loop (DACL) to overcome the bottlenecks of traditional analog compensating topologies. The design includes digitally assisted current sources at the output stage, which significantly enhance the outer SR. Furthermore, digitally controlled switches block the parasitic capacitance introduced by the current sources, thereby removing the high-quality-factor poles at low frequencies. This addresses the ringing in transient response which deteriorates STD. Moreover, the DACL-generated digital words are reused to create a programmable active zero, which ensures closed-loop stability over a wide load range. The prototype amplifier demonstrates an unprecedented load-range capability of 1500 (over 2.7× improvement) and almost the best STD of 2.86 ever reported.

Implementation of OTA core. Figure 1(a) depicts the proposed overall multistage amplifier, consisting of the main amplifier (MA) and DACL. The MA features a three-stage amplifier core embedded with programmable active zero and SR-enhanced current sources. It employs a transconductance capacitance feedback compensation topology [3] to achieve a high gain and robust closed-loop stability. The current detector depicted in Figure 1(b) monitors the biased state of the output stage (V_{GP} and V_{GN}) to trigger the SR-enhancement procedure. Once the output V_{CD} is acquired, the slewing-detect loop in Figure 1(c) determines whether there is a need for a current source or sink. Finally, the dynamic logic illustrated in Figure 1(d) latches the comparison results ($D_P[i]$, $D_N[i]$)$_{i=1,2,3,4}$ and controls the source followers ($M_{\mathrm{SP}[1,2,3,4]}$, $M_{\mathrm{SN}[1,2,3,4]}$). Consequently, the compensating current sources ($M_{P[1,2,3,4]}$, $M_{N[1,2,3,4]}$) are conducted so that SR-enhancement commences. The operational principle of DACL is detailed below. First, the current detector continuously monitors the bias states of the class AB output stage, where the output voltage V_{CD} indicates whether slewing occurs. Then, V_{CD} is fed into a quantizer composed of N-type input and P-type input comparators (NCMP and PCMP), generating comparison results based on V_{refH} and V_{refL}, which are the compensation-threshold voltages to determine whether SR enhancement is necessary. In this design, VDD equals 1.2 V, with the threshold voltage of the low-V_{TH} (lvt) transistor being approximately 270 mV. Therefore, V_{refL} and V_{refH} are set to 390 and 790 mV, respectively. If $V_{\mathrm{refL}} < V_{\mathrm{CD}} < V_{\mathrm{refH}}$, both NCMP and PCMP comparators output a logic high, and RES equals VDD. In this scenario, the dynamic logic does not start but remains reset, corresponding to a small-signal settling state. CLK_C is an event-driven asynchronous clock signal gener-

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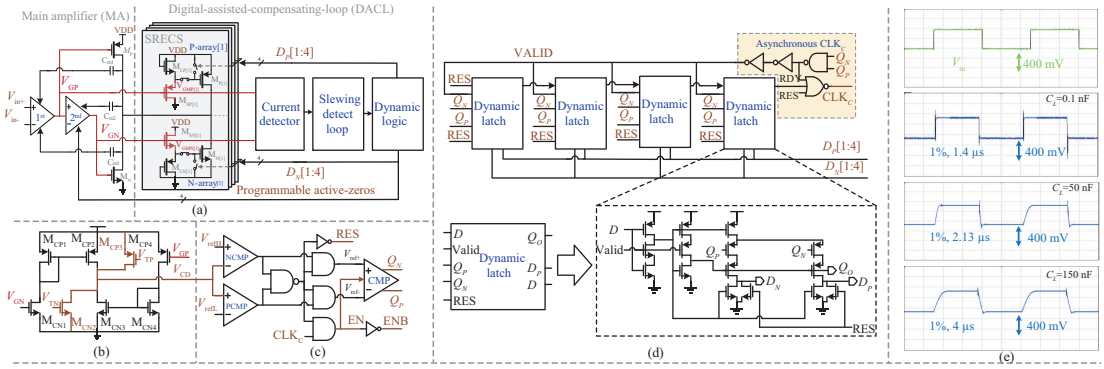

Figure 1 (Color online) Proposed digitally assisted OTA. (a) Overall architecture; (b) current detector; (c) slewing-detect loop; (d) dynamic logic; (e) measured transient response.

ated to control reset and compare operations without an external clock input. While $V_{\rm CD} > V_{\rm refH}$, $V_{\rm ref+} = 0$ and $V_{\rm ref-} = 1$. CLK$_C$ flips to high through asynchronous logic and CMP (dynamic comparator) valuates $V_{\rm ref+}$ and $V_{\rm ref-}$. Once the corresponding results Q_P and Q_N are obtained, the dynamic latch stores them into $(D_P[i], D_N[i])_{i=1,2,3,4}$, followed by CLK$_C$ reverting to low, resetting Q_P and Q_N to high. The asynchronous loop allows for sequential storage of Q_P and Q_N into 4-bit dynamic logic. The resolution of DACL, balancing both the convergence speed and compensating accuracy against the load range, is determined. Each latch performs ($D_P[i]$, $D_N[i]$), controlling the compensating N-arrays ($M_{N[i]}$) connected to the output stage to provide a current sink. When $V_{\rm CD} > V_{\rm refL}$, $V_{\rm ref+} = 1$, $V_{\rm ref-} = 0$, the compensating P-arrays ($M_{P[i]}$) are connected to provide a current source. The compensating loop stops once $V_{\rm CD}$ satisfies $V_{\rm refL} < V_{\rm CD} < V_{\rm refH}$ or all 4-bit digital words have been utilized. The accumulated outer SR can be obtained as

$$\mathrm{SR}_{\rm out} = \frac{[\sum_{i=1}^{4} D_P(i) I_{\rm source}, \sum_{i=1}^{4} D_N(i) I_{\rm sink}]_{\rm min}}{C_L}, \quad (1)$$

where $I_{\rm source}$ and $I_{\rm sink}$ represent the unit compensating currents of DACL. According to (1), the outer SR is released by the constraints of analog current headroom. In this work, the maximum output current has been boosted from 5 µA to 15 mA. Since $t_{\rm set}$ under heavy load conditions is not constrained by the outer SR, STDs can be smaller than 2.86.

Programmable active-zero technique. Overall, DACL enables obtaining a small STD, while $C_{L,\rm max}$ is still constrained to 80 nF owing to the static frequency response. Notably, in this work, the binary codes ($D_P[i]$, $D_N[i]$)$_{i=1,2,3,4}$ directly reflect the load size, which can be reused to produce dynamic active zero, typically through programmable R_Z controlled by the stated binary codes. The transfer function of the circuit, consisting of $M_{15–19}$ along with R_Z, C_Z, can be deducted as

$$H(s)|_{\rm ACT} \approx -\frac{g_{m15}(1+sR_ZC_Z)}{g_{m19}+sC_Z+s^2R_ZC_ZC_p}, \qquad R_Z = \sum_{i=1}^{4} D(i)R(i), \quad (2)$$

where C_p represents the parasitic capacitance at the drain of $M_{17,19}$. Eq. (2) highlights that C_Z is important for determining the value of $z_{\rm act}$ and the derived poles. To minimize the effects of derived parasitics, R_Z was designed to have a programmable range spanning from 42 to 393 kΩ. Despite the constraints on compensating accuracy, this design ensures a phase margin exceeding 45°. C_Z was chosen as 200 fF to suppress the effect of the derived pole ($-g_{m19}/C_Z$).

Experimental results. The proposed amplifier was fabricated using a 65-nm CMOS process. Its transient response was evaluated in a unit-gain feedback configuration inspired by a pulse of 400 mVpp at 20 kHz, as illustrated in Figure 1(e). The load range was externally varied from 0.1 to 150 nF. The measured t_A is presented in Figure 1(e). Owing to the induced current sources, the step transient response recorded achieves 1.4 and 4 µs at 0.1 and 150 nF, respectively, with a settling error less than 1%. Overall, the proposed amplifier demonstrates a wide load range and excellent STD facilitated by the digitally assisted technique. The proposed topology offers a scalable solution applicable to other amplifier designs.

Conclusion. This study demonstrated a digitally assisted multistage amplifier that achieves an extensive load range with small variations in settling time. The DACL was proposed and implemented to obtain a small STD while maintaining power efficiency. The digital words generated from DACL were reused to enhance the closed-loop stability across a wide load range. Future studies will focus on enhancing the accuracy of programmable active zeros through active resistance, aiming to extend load-range stability. Increasing the resolution of DACL could help meet requirements for improved human color vision.

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