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A 26.5–29.5-GHz Doherty PA with enhanced linearity and efficiency based on adaptive bias circuit for 5G MIMO arrays

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Power amplifiers (PAs) play a crucial role in achieving key performance metrics such as efficiency, power, and linearity. However, in the millimeter-wave frequency range, the performance of active devices rapidly deteriorates with increasing frequency. The typical Doherty architecture, through load modulation techniques, can achieve high back-off efficiency [1]. To enhance the linearity of the PA, adaptive bias circuits (ADBs) have been widely adopted [2,3]. These circuits provide bias voltages that increase monotonically with input power, compensating for gain compression and thereby improving linearity. However, in high input power modes, the monotonically increasing bias voltage can lead to excessive voltage swings for the transistors, posing a potential risk. In addition, in multi-beam arrays, the performance of the transceiver is significantly influenced by the mutual coupling between closely spaced radiating elements. This leads to a loading or voltage standing wave ratio (VSWR) condition that varies with the beam-steering angle [4].

This study proposes an adaptive bias-based Doherty PA with enhanced linearity and efficiency, featuring excellent VSWR characteristics. The proposed ADB consists of adaptive boost and buck circuits, allowing for efficient turn-off of the auxiliary PA in low-power mode, gain compensation in large signal mode, and over-saturation protection in high-power mode. Using RC feedback and matching networks, the Doherty PA achieves excellent port reflection. Additionally, neutralization capacitor technology is introduced to counteract transistor parasitic capacitance, thereby improving circuit gain and stability.

The proposed ADB comprises an adaptive buck circuit and a boost circuit. The output voltage of the adaptive buck circuit decreases consistently as input power increases, while the output voltage of the adaptive boost circuit increases consistently with rising input power. When combined, they yield the effect illustrated in the right portion of Figure 1(a), where the output voltage exhibits an initial increase followed by a decrease as input power rises. By configuring the circuit parameters, the desired adaptive biasing effect can be attained. When only the adaptive buck circuit is operational, the current relationship can be expressed as

$$i_{D1} = (1+\beta)i_{D2} + i_{D3}, \tag{1}$$

where, i_{D1} represents the current flowing out from the N_1 emitter, i_{D2} represents the current entering the N_2 base, β denotes the current gain factor of N_2, and i_{D3} represents the current flowing out of R_3. An increase in input power results in a rise in V_1, leading to an increase in i_{D2}, which in turn significantly reduces i_{D3}. The output voltage of the adaptive buck circuit can be expressed as

$$V_{\mathrm{Down}} = V_{\mathrm{BE}} + i_{D3}R_B. \tag{2}$$

In the adaptive boost circuit, the equivalent resistance of the diode, denoted as R_{diode}, decreases as the input power increases, resulting in an increase in i_{U3} [2]. The output voltage of the adaptive boost circuit can be expressed as

$$V_{\mathrm{Up}} = V_{\mathrm{BE}} + i_{U3}R_B. \tag{3}$$

Hence, the total voltage provided by the ADB for N_{RF} can be expressed as

$$V_{\mathrm{ADB}} = V_{\mathrm{BE}} + (i_{D3} + i_{U3})R_B. \tag{4}$$

The output voltage of the ADB is determined by both i_{D3} and i_{U3}. The regulation of the adaptive boost and buck circuits is shown in Appendix A. Adjusting the resistor R_{D3} in the adaptive buck circuit, the bias voltage of the auxiliary PA in low-power mode can be effectively tuned. Adjusting the resistor R_{U3} in the adaptive boost circuit can effectively tune the bias voltage in high-power mode.

With the proposed ADB, in the back-off mode, the auxiliary PA can be biased into a deep shutdown state, effectively approaching an open-circuit condition. The output impedance of the main PA in the back-off mode approaches 100-Ω impedance (see Appendix B). As power increases, the Doherty PA enters the large-signal mode, and the adaptive bias enters the boost region, causing the auxiliary PA to turn on and gradually enter saturation. Beyond the power saturation region, the output voltage of this ADB decreases with increasing input power, preventing excessive voltage swings for the transistors in the auxiliary PA at high bias states and thus serving to protect the transistors. In the

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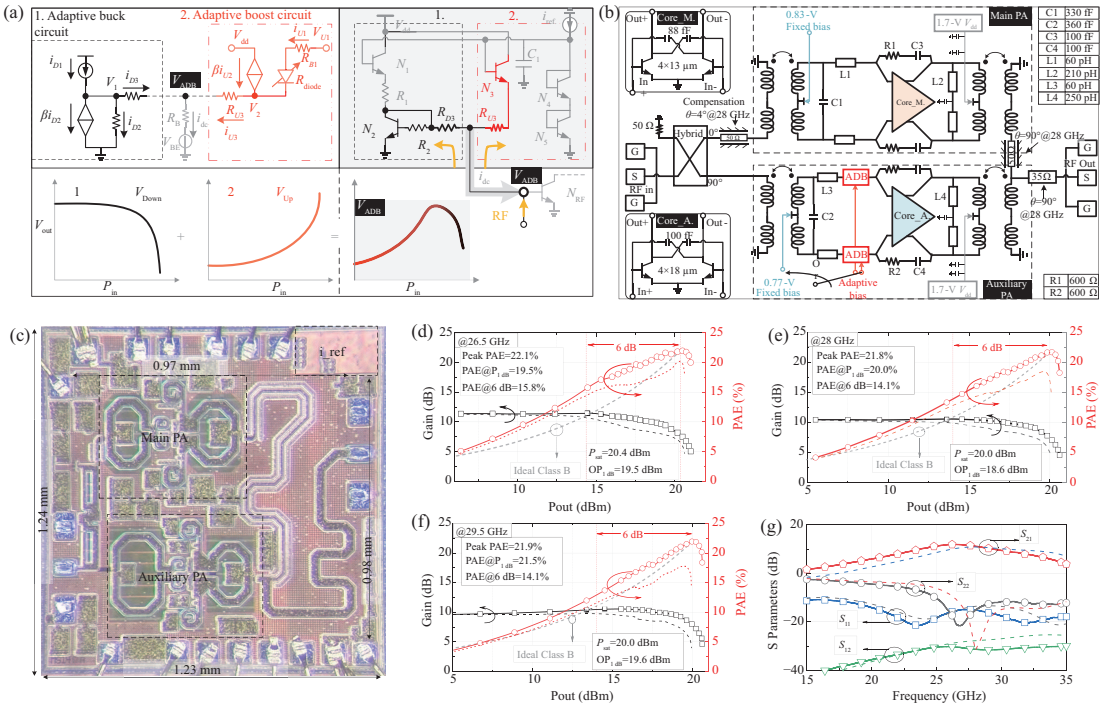

Figure 1 (Color online) (a) Schematic of the proposed ADB. (b) Schematic of the proposed Doherty PA based on ADB. (c) Photograph of the proposed Doherty PA. Measured large signal performance at (d) 26.5 GHz, (e) 28 GHz, and (f) 29.5 GHz. (g) S-parameters.

design, neutralization capacitors are employed to counteract the influence of this parasitic capacitance thus improving the gain and the stability (see Appendix C). The relatively large transistor dimensions result in a lower matching impedance, producing a higher impedance transformation ratio. To achieve good VSWR performance, two design methods are employed: (1) RC feedback to improve port impedance characteristics while enhancing circuit stability; (2) Balun matching to reduce the impedance transformation ratio. Compared to a direct synthesis structure, balun offers advantages such as reducing the 50 Ω load impedance, decreasing the impedance transformation ratio, enhancing impedance matching efficiency, and reducing matching network losses [5]. Figure 1(b) presents the schematic of the proposed Doherty PA. The ADB is implemented in the auxiliary PA. To facilitate testing and comparing the differences between adaptive and fixed bias, this circuit allows switching between adaptive bias and fixed bias modes. Both main and auxiliary PAs utilize differential structures to provide power combining and common-mode suppression capabilities.

Fabricated in a 0.13-μm SiGe BiCMOS process, this proposed chip has a core size of 0.97 mm × 0.98 mm (see Figure 1(c)). Figures 1(d)–(f) demonstrate the linearity and efficiency performance. At 26.5/28/29.5 GHz, the measured $P_{\rm sat}$ is 20.4/20.0/20.0 dBm, the $\rm OP_{1dB}$ is 19.5/18.6/19.6 dBm, with the peak power-added efficiency (PAE) of 22.1/21.8/21.9%, and 6-dB back-off PAE of 15.8/14.1/14.1%. It can be observed that with the introduction of adaptive bias (solid lines), the linearity and efficiency of this Doherty PA are effectively improved compared to the fixed bias scheme (dashed lines). As shown in Figure 1(g), this Doherty PA features a gain of 11.9 dB, with a gain variations of less than 2 dB in 24–29.5 GHz frequency band. The S_{22} is from −12 to −22 dB, while the S_{11} is less than −15 dB over 26.5–29.5 GHz.

In this study, we proposed a 26.5–29.5 GHz Doherty PA with enhanced linearity and efficiency based on an ADB. The proposed ADB enables the Doherty PA to achieve relative ideal impedance modulation for efficiency improvement, gain compensation in large signal mode, and oversaturation protection in high-power mode. By utilizing RC feedback and matching networks, it achieves outstanding VSWR, which enhances its immunity to mutual coupling in multiple-input multiple-output (MIMO) arrays. Neutralization capacitor technology is introduced to improve circuit gain and stability. This millimeter-wave Doherty PA is well-suited for application in 5G large-scale MIMO arrays.

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Supporting information Appendixes A–H. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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