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• **Supplementary File** •

A 26.5–29.5-GHz Doherty PA With Enhanced Linearity and Efficiency Based on Adaptive Bias Circuit for 5G MIMO Arrays

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Appendix A Regulation of the adaptive boost and buck circuits

The output voltage of the adaptive bias circuit is determined by both i_{D3} and i_{U3}. It is worth noting that the impact of the adaptive boost and buck circuits on the output bias voltage is not equivalent and their inconsistency is primarily reflected in the power range over which they operate. This can be observed from the simulation data as Fig. A1. The magnitude of the impact of both adaptive bias circuits can be adjusted by modifying the values of resistors R_{D3} and R_{U3} to regulate the strength of the adaptive buck and boost circuits. According to the simulation data in Fig. A1(a), it is evident that by adjusting the resistor R_{D3} in the adaptive buck circuit, the bias voltage of the auxiliary PA in low-power mode can be effectively tuned. Similarly, based on the simulation data in Fig. A1(b), adjusting the resistor R_{U3} in the adaptive boost circuit can effectively tune the bias voltage of the auxiliary PA in high-power mode.

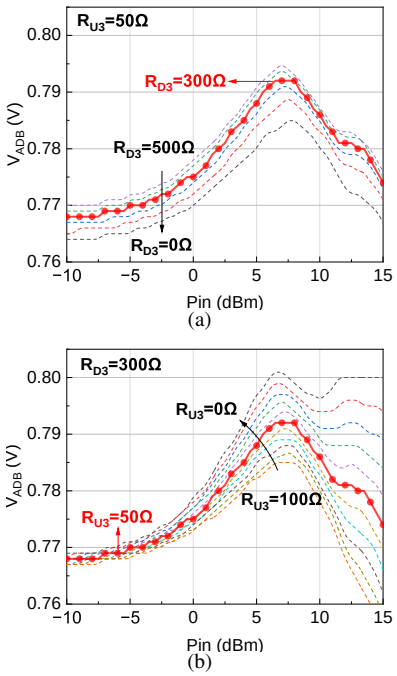

Figure A1 (a) Output voltage of the adaptive bias circuit versue the resistance R_{D3} in the buck circuit, and (b) resistance R_{U3} in the boost circuit.

Appendix B Impedance characteristic

According to Fig. B1(a) and (b), in the fixed bias mode (dashed lines), during power back-off, the output impedance of the auxiliary PA falls below 300 Ω, and the impedance seen by the main PA cannot reach 100 Ω. However, with the proposed adaptive bias circuit (solid lines), it can be observed that in the back-off mode, the auxiliary PA can be biased into a deep shutdown state, effectively

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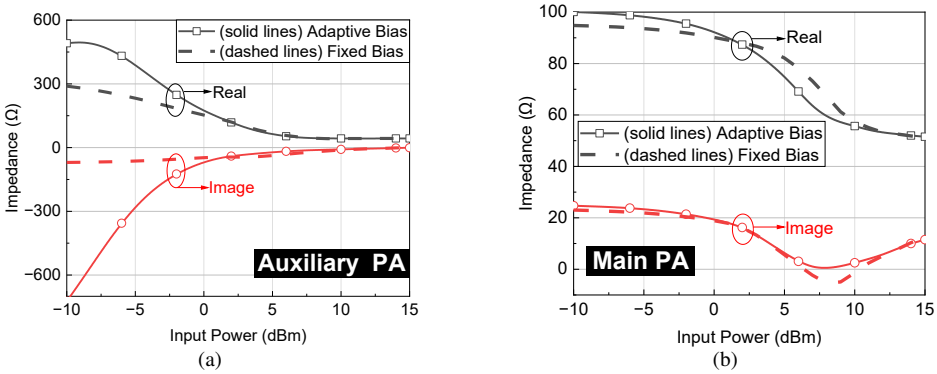

Figure B1 Output impedance of the (a) Auxiliary and (b) main PA in adaptive (solid lines) and fixed bias (dashed lines) modes.

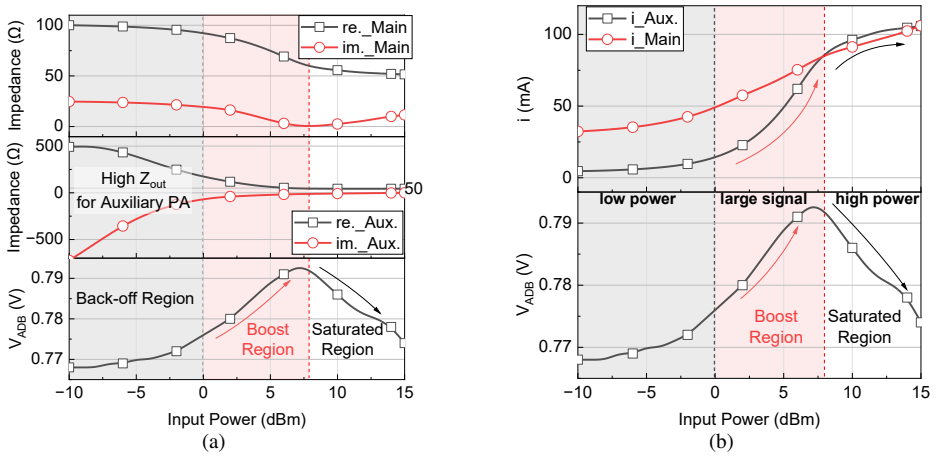

Figure B2 (a) Output impedance and (b) dynamic current of the main and auxiliary PAs versus the ADB output voltage (V_{ADB}).

approaching an open-circuit condition. At this point, the output impedance of the main PA in the back-off mode approaches the theoretically expected 100 Ω impedance. Fig. B2(a) and (b) display the output impedance and current of the main and auxiliary PAs versus the output voltage (V_{ADB}) of the adaptive biasing. It is observed that due to the sufficiently low biasing of the auxiliary PA in the back-off mode, both the main and auxiliary PAs exhibit more ideal impedance characteristics, and the adaptive current of the auxiliary PA is low. As power increases, the Doherty PA enters the large-signal mode, at which point the adaptive bias enters the boost region, causing the auxiliary PA to turn on and gradually enter saturation. Beyond the power saturation region, the output voltage of this adaptive bias circuit decreases with increasing input power, preventing excessive voltage swings for the transistors in the auxiliary PA at high bias states and thus serving to protect the transistors.

Appendix C Neutralization capacitor and RC feedback

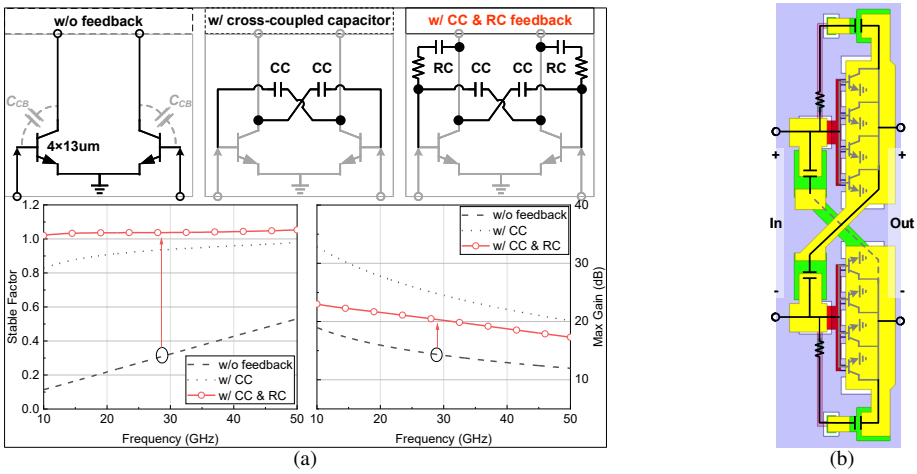

Figure C1 (a) Stable factor and maximum gain versus feedback. (b) Layout of the differential 4 x 13-μm PA core with neutralization capacitors and *RC* feedback.

For the common-emitter structure (CE), the parasitic capacitance C_{CB} between the collector and base deteriorates device gain, reverse isolation, and affects device stability. In the design of this differential PA, neutralization capacitors are employed to counteract the influence of this parasitic capacitance. According to load-pull simulation results, by introducing an 88 fF neutralization capacitor, the maximum output power increases from 18.49 dBm to 19.34 dBm. In this design, the RC feedback was also included to enhance stability while improving output impedance matching. With the introduction of this RC feedback structure, the stability factor of the PA differential core exceeds 1 (see Fig. C1).

Appendix D Mismatch conditions

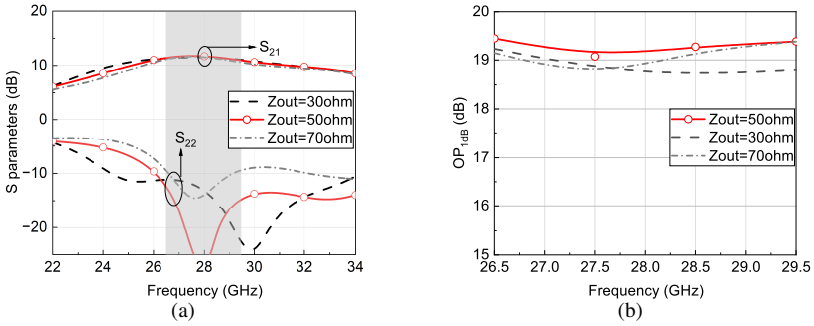

Figure D1 (a) S21 and S22 versus load impedance. (b) OP1dB versus load impedance.

To evaluate the performance of the Doherty PA under mismatch conditions. The S parameters and OP1dB with load impedances of 30 ohms and 70 ohms are simulated, respectively, representing ±20 ohm impedance mismatch from the ideal 50 ohm load. As illustrated in Fig. D1, the simulation results demonstrate that even under these mismatch conditions, the gain remains stable, and the output return loss is still less than -10 dB. Additionally, the variation in OP1dB is less than 1 dB, indicating robust performance of the Doherty PA in the presence of load impedance mismatches.

Appendix E Lange coupler

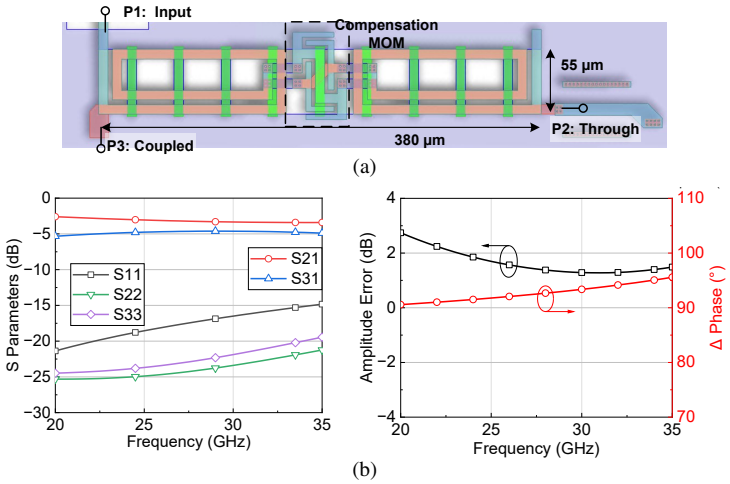

Figure E1 (a) Layout view of the lange. (b) Simulated S-parameters and balance performance of the Lange.

The Lange coupler used in this work, as depicted in Fig. E1, exhibits characteristics such as compact dimensions, excellent port matching performance, and high balance. The area of this 28 GHz Lange coupler is 380 $\mu m \times 55$ μm. The compensation MOM capacitor is employed to enhance the coupling between the coupling lines, thus avoiding the need to create larger window structures in the ground plane to reduce ground coupling. Using the thick metal layer (AM) for the design of this capacitor bring two advantages: 1) reduced capacitance variations caused by process errors. 2) enhanced Q-factor of the capacitor and reduce unnecessary losses it may introduce. Simulation results in Fig. E1(b) shows that within the desired frequency band, the port reflection coefficients are all better than -17 dB. In the frequency range from 24 to 30 GHz, the amplitude difference between the through port and the coupled port of this coupler is about 1.5 dB. This is an overall optimization result aimed at achieving deeper efficiency back-off for Doherty PA. The phase difference varies between 91°to 92°.

Appendix F Simulated OP_{1dB}

Fig. F1 illustrates the simulated OP_{1dB} of the Doherty PA under adaptive bias and fixed bias conditions. It can be observed that the introduction of adaptive bias significantly improves the linearity of this Doherty PA.

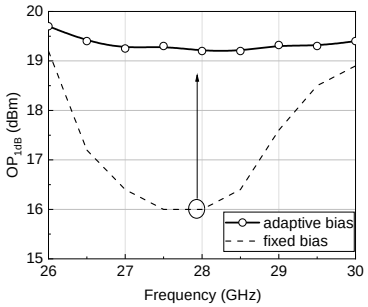

Figure F1 Simulated OP_{1dB} of the PA with adaptive (solid line) and fixed (dashed line) bias.

Appendix G Measurement setup

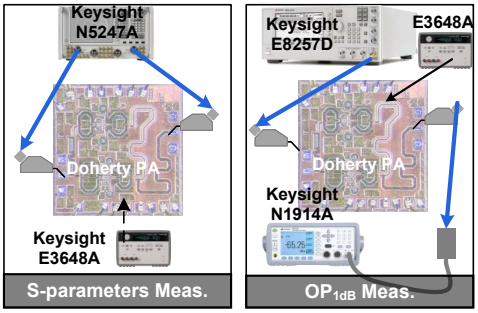

Figure G1 Measurement setup.

Fig. G1 illustrate the small-signal and large-signal measurement setup. Small-signal measurements were carried out using the Keysight N5247A. The OP_{1dB} performance was obtained using the Keysight E8257D signal source and the Keysight N1914A power meter.

Appendix H Comparison table

Table I presents a comparison with previous silicon-based adaptive bias-based or Doherty PAs. The proposed Doherty PA offers a balanced combination of good linearity, back-off efficiency, port VSWR performance, and compact size characteristics, making it suitable for 5G large-scale MIMO arrays.

Table H1 A comparison with previous silicon-based adaptive bias-based or Doherty PAs.

	This Work	[1] TCASII'21	[2] JSSC'23	[3] RFIC'19	[4] ISSCC'15	[5] JSSC'19
Process	**0.13-μm SiGe**	0.13-μm SiGe	45-nm SOI	28-nm CMOS	0.13-μm SiGe	0.13-μm SiGe
Architecture	**Adaptive bias-based Doherty**	Adaptive bias-based Class-AB	Coupled-inductor-based three-way Doherty PA	DAT	Digital 8-way Dynamic Load Modulated	Multiband Analog Doherty
Frequency/GHz	**26.5**	29	38	39	46	28
Gain/dB	**11.9**	35	15	38	13	18.2
S_{11}/S_{22}**/dB**	**-15 / -12∼-22**	-5	-8 ∼-9	<-10	N.A.	N.A.
P_{sat}**/dBm**	**20.4**	21	18.9	26	28.9	16.8
OP_{1dB}**/dBm**	**19.5**	20.1	18.4	21.5	N.A.	15.2
Peak PAE/%	**22.1**	23	23.3	26.6	18.4	20.3
PAE@OP_{1dB}**/%**	**19.5**	22	23	13.6	N.A.	19.5
PAE@6dB/%	**15.8**	11.5	17.1	10%	11%	13.9%
Core size/mm^2	**0.95**	0.58	2.0	0.95	11.3	1.3

References

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