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# Effects of the $V_{GS}$ sweep range on the short channel effect in negative capacitance FinFETs

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As the CMOS technology scaling is reaching fundamental limits, there is a substantial demand for energy-efficient devices with lower operating voltage. Negative capacitance field-effect transistors (NCFETs) exhibit the capability to amplify the gate voltage and become promising candidates for future advanced process nodes. Ferroelectric (FE) $HfO_2$-based materials, with impressive scalability and compatibility with CMOS processes, show the feasibility of integration into NCFETs to achieve nanoscale high-performance transistors. Due to the introduction of the NC effect, the short channel effects (SCEs) in $HfO_2$-based NCFETs differ from conventional devices, which have undergone extensive research [1]. Specifically, drain-induced-barrier-lowering (DIBL) plays a key role in determining the severity of SCEs, exhibiting a reverse behavior in NCFETs. Despite the acknowledged influence of applied voltage on the performance of NCFETs [2], the impact of gate voltage sweep range ($V_{GS,range}$) on the DIBL in advanced short channel NC-FinFETs still lacks study.

In this study, we experimentally investigate the impact of $V_{GS,range}$ on the DIBL in $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based NC-FinFETs for different gate lengths ($L_G$s). The NC-FinFETs exhibit notable improvements in DIBL compared with the $HfO_2$ devices, the degree of which significantly depends on the $V_{GS,range}$. Subsequent analyses reveal that such DIBL modulation behavior varies significantly across different $L_G$s, which is attributed to the coupling mechanism involving fringing electric field and voltage-dependent FE layer characteristics.

*Device fabrication.* Figure 1(a) depicts the schematic of the fabricated FinFETs. The NC-FinFETs, integrating a 3 nm HZO layer, were developed using a metal gate all-last approach implemented within a standard manufacturing process. The fabrication process is fundamentally compatible with the previous study [3]. The interfacial layer (IL) was grown by $O_3$ oxidation after the dummy poly-Si gate removal for better interface quality and device reliability. Furthermore, the gate insulator of 3 nm FE HZO was deposited through atomic layer deposition (ALD) at a temperature of 300°C. A forming gas annealing (FGA) at 450°C/30 min was carried out for alloy processes. The devices without ferroelectricity were also fabricated, featuring a 4 nm $HfO_2$ gate insulator. The $L_G$ of the FinFETs ranged from 20 to 500 nm for investigating the DIBL characteristics.

*Results and discussion.* The transmission electron microscope (TEM) view of the gate stack along $xx'$ in Figure 1(b) illustrates the Metal/3 nm HZO/IL/Si stack, which achieves highly conformal HKMG films on the 3D Fin. The cross-sectional structure along $yy'$ of an NC-FinFET with $L_G$ of 20 nm is shown in Figures 1(c) and (d). The transfer characteristics of 20 nm $L_G$ NC-FinFET at drain linear voltage ($V_{DLIN}$) of −0.1 V and drain saturation voltage ($V_{DSAT}$) of −0.8 V are shown in Figure 1(e). Figure 1(f) depicts the corresponding point subthreshold swings (SSs) as a function of drain current ($I_{DS}$). In comparison to the electrical characteristics of paraelectric $HfO_2$ devices depicted in Figures 1(g) and (h), the HZO FinFET demonstrates a minimum SS of 34.1 mV/decade, manifesting a discernible NC effect.

To investigate the DIBL effect under various $V_{GS,range}$, the $I_{DS}$-$V_{GS}$ curves were measured as shown in Figures 1(i) and (j). The HZO NC-FinFET was subjected to $V_{GS,range}$s of ±0.6, ±0.8, and ±1 V. Due to the thicker gate insulator in $HfO_2$ devices, a higher maximum $V_{GS,range}$ of ±1.2 V was applied. The threshold voltage ($V_T$) was determined using the constant current method at $I_{DS}$ of $10^{-9}$ A. The insets of Figures 1(i) and (j) reveal a shift in $V_T$ under varying $V_{GS,range}$. The DIBL was extracted using $V_T(V_{DSAT}) - V_T(V_{DLIN})/(V_{DSAT} - V_{DLIN})$ and summarized in Figure 1(k). Evidently, an enhancement in DIBL can be found for NC-FinFETs compared to $HfO_2$ devices. It is worth noting that the DIBL of the NC-FinFET exhibits an increase with the rising $V_{GS,range}$, indicating a $V_{GS,range}$-dependent NC effect. The DIBL is notably influenced by the differential capacitance from the top of the energy barrier to the gate ($C_G$) [1, 4]. It has been reported that the $P_r/E_c$ of the HZO capacitor increases with the augmentation of $V_{GS,range}$, which leads to a larger capacitance of the FE layer ($|C_{FE}|$) [2]. Considering that the gate stack capacitance, a main component of $C_G$, can be

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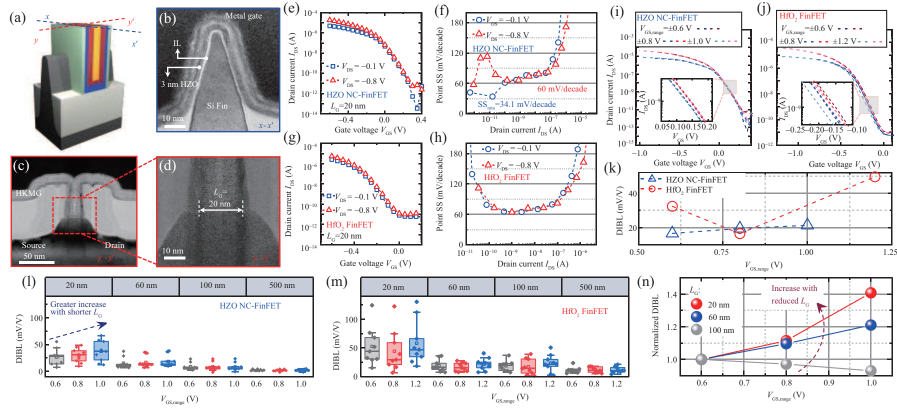


**Figure 1** (Color online) (a) Schematic of the fabricated negative capacitance (NC) FinFET. Cross-sectional transmission electron microscope (TEM) images along (b) $xx'$, (c) $yy'$, and (d) its local magnification. $I_{\rm DS}$-$V_{\rm GS}$ curves of (e) HZO and (g) $\rm HfO_2$ FinFETs with a gate length of 20 nm. The corresponding subthreshold swing (SS) versus $I_{\rm DS}$ characteristics are shown in (f) and (h), respectively. (i, j) $I_{\rm DS}$-$V_{\rm GS}$ curves measured with various $V_{\rm GS,range}$. The insets provide amplified views near the threshold voltage. (k) The DIBL versus $V_{\rm GS,range}$ extracted from (i) and (j). Extracted DIBL under various $V_{\rm GS,range}$ of (l) HZO and (m) $\rm HfO_2$ FinFETs, measured for different $L_{\rm G}$. (n) The relative change in mean DIBL values for NC-FinFETs with varying $V_{\rm GS,range}$.

expressed as $C_{\rm stack} = (C_{\rm FE^{-1}} + C_{\rm IL^{-1}})^{-1}$, a more negative $C_{\rm FE}$ resulting from the increased $V_{\rm GS,range}$ leads to a reduced $C_{\rm G}$, suggesting a weakened NC effect and an increase in DIBL. Therefore, the observed rise in DIBL with increased $V_{\rm GS,range}$ can be attributed to the modulation effect of the voltage across the FE layer on the FE characteristics.

Herein, more results with varying $L_{\rm G}$s are presented to further analyze the impact of $V_{\rm GS,range}$ on the DIBL with size scaling. Figure 1(l) summarizes the measurement results of NC-FinFETs with gate lengths ranging from 20 to 500 nm. Compared with the results of $\rm HfO_2$ devices illustrated in Figure 1(m), a pronounced improvement in DIBL can be found for NC-FinFETs with different $L_{\rm G}$s and $V_{\rm GS,range}$. Notably, negative DIBL (N-DIBL) is also observed. Furthermore, an evident trend of escalating DIBL magnitude with increased $V_{\rm GS,range}$ is discernible for short $L_{\rm G}$, while for longer $L_{\rm G}$, it exhibits a comparable DIBL across various $V_{\rm GS,range}$. In NC-FinFETs with an $L_{\rm G}$ of 20 nm, the mean DIBL increases from 26.5 to 37.3 mV/V as $V_{\rm GS,range}$ varies from ±0.6 to ±1 V, with most devices showing a significant difference, particularly between 0.6 and 0.8 V, compared to $\rm HfO_2$ devices. Figure 1(n) summarizes the relative magnitude of the increase in DIBL with $V_{\rm GS,range}$ variation. The impact of $V_{\rm GS,range}$ becomes progressively more pronounced as the $L_{\rm G}$ decreases.

Subsequently, the underlying mechanism of the highly $L_{\rm G}$-dependent DIBL modulation behavior by $V_{\rm GS,range}$ is analyzed. As mentioned above, the $C_{\rm FE}$ modulated by the $V_{\rm GS,range}$-dependent FE layer parameters determines the DIBL effect. Hence, the distinct influence of $V_{\rm GS}$ on DIBL at various $L_{\rm G}$s suggests that the relationship between $C_{\rm FE}$ and $V_{\rm GS,range}$ varies for different $L_{\rm G}$s. The expression for $C_{\rm FE}$ is given by $(\varepsilon_{\rm r}\varepsilon_0 + 1/(2\alpha + 12\beta P_{\rm FE}^2 + 30\gamma P_{\rm FE}^4))/t_{\rm FE}$, where FE material parameter $\alpha$, $\beta$ <0 and $\gamma$ >0, and $\varepsilon_{\rm r}$, $P_{\rm FE}$, and $t_{\rm FE}$ are the dielectric constant, FE polarization, and thickness of the FE layer, respectively [1]. It has been reported that the impact of the fringing electric field becomes stronger with $L_{\rm G}$ scaling, which changes the $P_{\rm FE}$ in the sub-threshold [1, 5]. According to the expression for $C_{\rm FE}$, apparently, a larger $|P_{\rm FE}|$ implies that the variation of high-order term FE parameters ($\beta$ and $\gamma$) influenced by $V_{\rm GS,range}$ exerts a more pronounced impact on $C_{\rm FE}$, consequently having a higher influence on DIBL performance. Note that the polarization gradient energy term for multi-domain is ignored herein, which further enhances the influence of the fringing electric field. Therefore, it can be concluded that scaling $L_{\rm G}$ can induce a larger $|P_{\rm FE}|$ due to the resulting fringing electric field, leading to distinct DIBL modulation behavior by $V_{\rm GS,range}$ at different $L_{\rm G}$s.

*Conclusion.* In summary, this study has investigated the impact of $V_{\rm GS,range}$ on the DIBL in FE HZO NC-FinFETs with different $L_{\rm G}$s. The observed improvement in DIBL for NC-FinFETs, as compared to $\rm HfO_2$ devices, demonstrates an enhancing trend with a decreasing $V_{\rm GS,range}$. Furthermore, the pronounced impact of $V_{\rm GS,range}$ on DIBL modulation is notable in short-channel devices, diminishing with increasing $L_{\rm G}$. This behavior is elucidated through the coupling mechanism involving fringing electric field and voltage-controlling FE layer parameters. This work contributes to a deeper understanding of SCEs in NCFETs for the development of advanced CMOS applications.

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