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• RESEARCH PAPER •
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Solid-state non-volatile memories based on vdW heterostructure-based vertical-transport ferroelectric field-effect transistors

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Abstract Driven by the explosive development of data-centric computation applications, it is becoming urgent to develop in-memory computing devices that are beyond the von Neumann architecture with an arrangement of separated logic and memory components. The transistor-type solid-state non-volatile memories, such as ferroelectric field-effect transistors (FeFETs), have long been regarded as a competitive candidate for future in-memory computing architectures. However, the density scaling towards high-density arrays would require advanced FeFETs with reduced footprints, which remains a great challenge so far. Here, a vertical-transport (VT) FeFET that flips the charge transport channel perpendicular to the substrate plane is proposed, in which a ferroelectric gate and a van der Waals (vdW) heterojunction channel are vertically integrated, effectively reducing the device footprints. The proposed VT-FeFET shows not only the robust binary non-volatile memory states but also several key synaptic functionalities at the device level. An artificial neural network with supervised learning was simulated based on the device conductance switching properties, showing excellent classification accuracy for the MNIST handwritten digits. These findings suggest that the proposed VT-FeFET could offer a new solution for future non-volatile memories as well as more advanced neuromorphic systems.

Keywords vdW heterostructure, non-volatile memory, vertical-transport transistor, ferroelectric field-effect transistor, memristive devices

1 Introduction

Van der Waals (vdW) heterostructures, which are composed of direct stacking of dissimilar vdW materials without the stringent requirement of lattice matching, could offer unprecedented advances in creating various material systems [1, 2]. Importantly, being able to combine distinct attributes of the constituent materials by design, vdW heterostructures have now been regarded as a viable solution for the creation of functional devices that are unattainable through traditional material platforms [1, 2]. A plethora of functional devices based on vdW heterostructures have emerged recently, covering a wide spectrum of semiconductor applications including but not limited to logic devices [3], memories [4], neuromorphic nanoelectronics [5], optoelectronics [6], and spintronics [7]. In particular, the merits of feasible

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construction of high-quality vertically-integrated heterojunctions have ignited the explosive development of vdW heterostructure-based vertical-transport field-effect transistors (VTFETs) [8–14]. In stark contrast with the conventional lateral-transport FETs (LTFETs), the VTFETs flip the charge transport direction that is perpendicular to the substrate plane [14–16]. With such a vertical arrangement of the device components, the VTFET device concept is thus promising to significantly reduce the device footprints and further enhance the density scaling of logic transistor technology [15–17]. Besides, benefiting from the excellent physical properties of vdW heterostructures, enhanced device performance metrics, such as large current density, high on-off ratio, and ultra-scaled channel length, can be realized in vdW heterostructure-based VTFETs [14]. Moreover, the intrinsic superior mechanical properties of vdW materials could make vdW heterostructure-based VTFETs tolerable to bending or stretching, thus suitable for flexible electronics [18].

Driven by the booming of artificial intelligence (AI) related applications, the computing scheme is currently rapidly evolving in a dramatically different way [19]. Beyond the traditional logic technology enabled classical von Neumann computing, high performance in-memory computing schemes based on non-volatile memories have been actively developed to support nowadays data-centric applications [20,21]. Constructing vdW heterostructure-based VTFETs with permanent control of device electronic properties could lead to a new type of solid-state memory, which is appealing to in-memory computing architectures in terms of the device area-efficiency. To date, various vdW heterostructure-based VTFETs have been reported, showing great promise for dimensional scaling of logic transistors. However, those reported vdW heterostructure-based VTFETs are particularly based on conventional linear dielectrics, and thus only exhibit volatile gate modulation of their electronic properties [8–14]. Therefore, it necessitates the further development of VTFETs for non-volatile memory functionalities.

Diversification of the functions of vdW heterostructure-based VTFETs would require a smart design of the constituent materials. Replacement of the linear dielectric component layer with a ferroelectric layer has been identified as an efficient approach to create non-volatile transistor-structure memories, which is termed as ferroelectric field-effect transistors (FeFETs) [4, 22, 23]. In fact, new device concepts of FeFET have been extensively explored in recent years due to their important roles in advancing non-volatile memory-based in-memory computing [4]. For example, FeFETs with new device structures including dual-ferroelectric-gate transistors [22], ferroelectric-semiconductor field-effect transistors [24, 25], and ferroelectric-enabled 2D Schottky barrier transistors [26] have been shown to exhibit fantastic device performance as a basic in-memory computing cell. However, these FeFETs still feature a lateral-transport channel structure, which could be challenged for future downscaling. In this regard, a vertical type of the device structure would become a potential solution for future ultra-scaled FeFETs.

In this work, we present a proof-of-concept demonstration of a class of solid-state memories based on vdW heterostructure/ferroelectric-based vertical-transport ferroelectric field-effect transistors (VT-FeFETs). In such a device concept, the synergistic coupling between the band alignment of the vertical vdW semiconductor heterojunction channel and the ferroelectric polarization can be exploited to enable a permanent switching of the device conduction states with an on-off ratio exceeding 10^5, thus rendering a high-performance solid-state non-volatile memory. Beyond the conventional long-term control of the high resistance state (HRS) and low resistance state (LRS) of the devices, the proposed VT-FeFETs also exhibit excellent memristive properties with multiple levels of robust conduction states, which can further extend their application to synaptic devices. To explore its suitability in neuromorphic applications, we simulated an artificial neural network (ANN) based on the analog device properties, presenting high image classification accuracy. The demonstrated VT-FeFET could offer a promising device concept for future solid-state memories, which can serve as the fundamental hardware unit of in-memory computation systems.

2 Results and discussion

The device structure of the proposed VT-FeFET is schematically presented in Figure 1(a). The MoS_2/$MoTe_2$ vdW heterostructure was employed here as the vertical transport semiconductor channel. The graphene (Gr) layer was placed underneath the vdW heterostructure serving the purpose of drain electrode (D), and the Au metal stripe was deposited atop the MoS_2 lateral channel as the source electrode (S). The flakes of MoS_2, $MoTe_2$, and Gr were produced by mechanically exfoliating their bulk single crystals and transferred onto the SiO_2 substrate via location-precise layer-by-layer stacking using a stan-

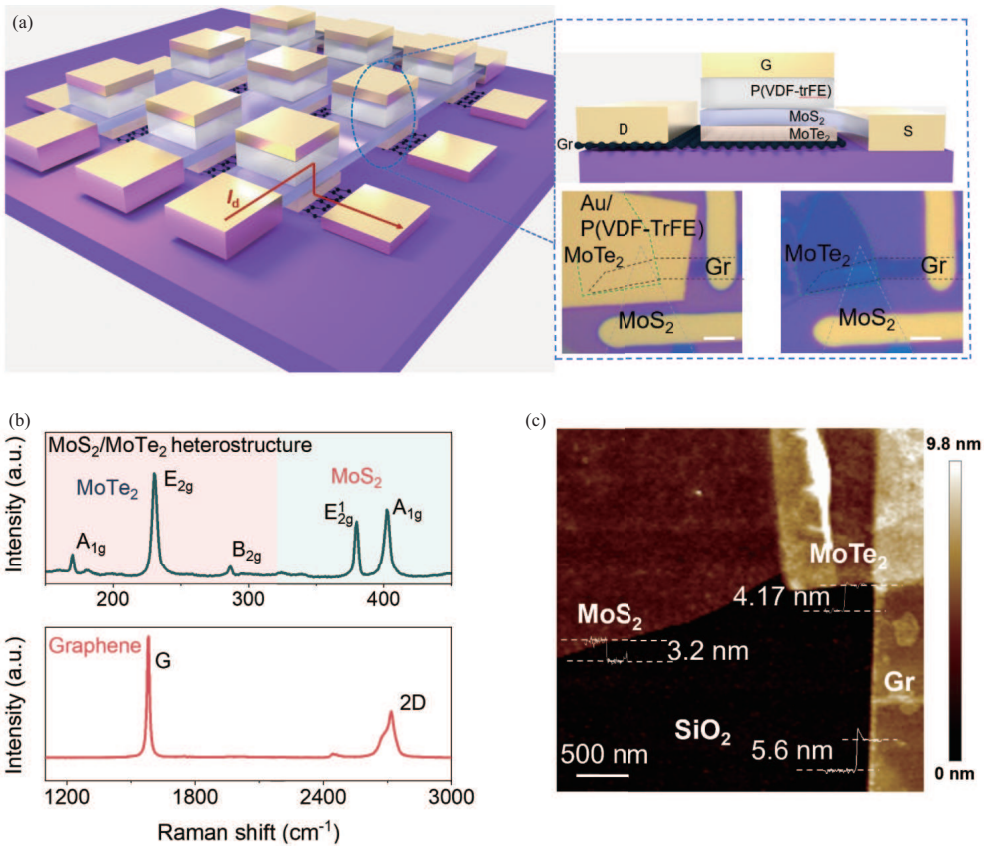

Figure 1 (Color online) Device architecture and structural characterization of the VT-FeFETs. (a) Schematic demonstration of the VT-FeFET composed by the P(VDF-TrFE) ferroelectric dielectric layer and the $MoS_2/MoTe_2$ vdW heterostructure vertical transport channel. The inset shows the optical images of the VT-FeFETs before and after coating with the P(VDF-TrFE) thin film. (b) Raman spectra of the $MoS_2/MoTe_2$/Gr heterostructure were collected by a 532 nm laser at 1 mW. (c) Topography and height profiles of the $MoS_2/MoTe_2$/Gr heterostructure.

dard dry transfer method [22]. To enable the ferroelectric modulation of the semiconductor channel, high-quality polymer ferroelectric thin film poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) of 100 nm was deposited on the $MoS_2/MoTe_2$ vdW heterostructure as the ferroelectric dielectric layer. Polymer ferroelectric thin films have been practically proven as a compatible dielectric material for vdW semiconductor-based devices, which present great interface coupling and can massively suppress the detrimental interfacial effects as always observed in oxide thin film/vdW semiconductor heterojunctions [22, 27]. Obviously, the gate dielectric and the transport channel are integrated vertically, which could thus maximize the 3D construction capability of the VT-FeFETs and decrease the device footprints. Such a prominent feature would lead to a compact device architecture when integrated into the large-scale crossbar arrays as shown in Figure 1(a) and further enables the density scaling during scalable chip manufacture. The optical image of a presentative VT-FeFET device is shown in the inset of Figure 1(a), where the overlapping area of the MoS_2 and the $MoTe_2$ flakes forms the vertical transport channel. A detailed device fabrication process can be found in Supplementary Note 1. As shown in Figure 1(b), the crystalline quality of the constituent vdW materials was examined using a Raman spectroscopy with a 532 nm excitation source, showing the sustained great structural quality of the flakes after the device fabrication process. We verified the thickness of the vdW heterostructures using atomic force microscopy (AFM) prior to the P(VDF-TrFE) spin-coating process. Figure 1(c) presents the topography and height profiles of the $MoS_2/MoTe_2$ vdW heterostructure along with the underlying Gr electrode, indicating a sub-10 nm transport channel length. Such an ultra-scaled semiconductor channel would enhance the electrostatic coupling towards high-performance devices and is highly desired for dimensional scaling of transistor-type logic and memory devices [28].

We next investigate the transport properties of the VT-FeFETs. During the electrical measurement, the metal contact to the MoS_2 lateral channel is always grounded as the source electrode. As shown in Supplementary Note 2, the coercive voltage for ferroelectric polarization switching of the 100 nm thick

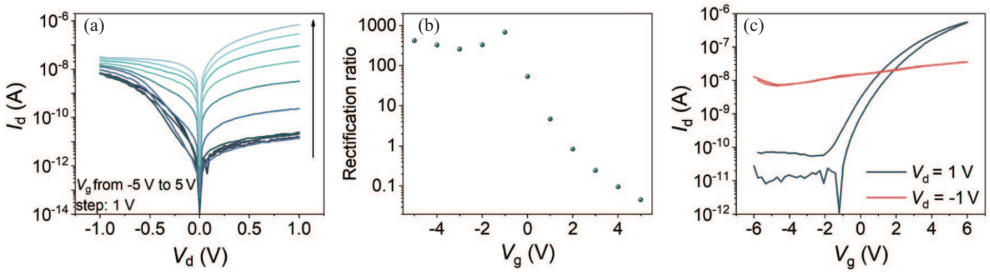

Figure 2 (Color online) Transport measurements of the VT-FeFET without reversal of the ferroelectric polarization in P(VDF-TrFE) (∼100 nm). Output curves (a) and rectification ratio (b) under various applied gate voltages. Note that the applied voltage is well below the coercive voltage of the ferroelectric layer. (c) Transfer curves of the VT-FeFET with the gate voltage sweeping below the coercive voltage.

P(VDF-TrFE) thin film is around 10 V. As shown in Figure 2(a), we measured the output properties of the VT-FeFET under various gate voltages (V_g) that are well below the coercive voltage of 100 nm thick P(VDF-TrFE) thin film. Here, the ferroelectric P(VDF-TrFE) thin film is biased in the linear dielectric regime, showing an electrostatic doping effect that is the same as the conventional linear dielectrics [29]. At $V_g = -5$ V, the $MoS_2/MoTe_2$ heterojunction demonstrates strong rectification behaviour, see Figures 2(a) and (b). Note that the devices in this work were measured at ambient as the 2D channel can be well protected by the top ferroelectric polymer. By gradually increasing V_g to 5 V, the drain current-gate voltage (I_d-V_g) curves turn to a symmetrically conducting state and the rectification ratio also drops. The evolution of the output curves of the $MoS_2/MoTe_2$ heterojunction-based VT-FeFET is related to both V_d and V_g. At the negative V_d regime, the strong electric field in the ultrathin n-type MoS_2/p-type $MoTe_2$ heterojunction would lead to the depletion state of majority carriers in both MoS_2 and $MoTe_2$ layers [10]. The $MoS_2/MoTe_2$ heterojunction thus behaves like a reverse-biased tunnel diode, where the band-to-band tunneling (BTBT) current onset voltage increases with lowering the gate voltage due to the weakened band titling of the $MoS_2/MoTe_2$ tunnel diode. When changing V_d to be positive, the $MoS_2/MoTe_2$ heterojunction can be operated as a forward biased p-n diode since the electrons and the holes are accumulated in the MoS_2 and $MoTe_2$ layer, respectively [10]. The drain current thus would grow as a function of the applied V_g due to the increased doping level in the n-type MoS_2 layer. As can be observed by the I_d-V_g curves of the $MoS_2/MoTe_2$ heterojunction-based VT-FeFET, the device transport behavior is dominated by the vertical junction as analyzed above. Thus, the proposed VT-FeFET can be regarded as a genuine vertical-transport device regardless of the remaining lateral MoS_2 channel. In consistency with the proposed working mechanism, the proposed VT-FeFET exhibits distinct transfer properties at different applied V_d, see Figure 2(c). At $V_d = 1$ V, superior conduction state switching is observed in the VT-FeFET showing a high on-off ratio beyond 10^5. At $V_d = -1$ V, due to the large BTBT current at different gate voltages, only a quite small current variation as a function of the V_g can be obtained here. The above results indicate that the proposed VT-FeFET can also function as a conventional logic transistor with volatile current switching properties, subjecting to the applied gate voltage.

We then applied gate voltages larger than the coercive voltage of the P(VDF-TrFE), which can sufficiently trigger the reversible polarization switching in the ferroelectric layer [4]. The remanent ferroelectric polarization can induce permanent and strong electrostatic doping into the adjacent semiconductor layer, thus resulting in the stable depletion and accumulation states of the MoS_2 layer corresponding to the polarization up and down situations, respectively. At $V_d = 0.5$ V, the VT-FeFET shows typical hysteretic current switching behavior by sweeping the gate voltage beyond the coercive voltage of the P(VDF-TrFE), see Figure 3(a). Upon withdrawal of the gate voltage, the VT-FeFET can be set with different conduction states as evidenced by the output curves, see Figure 3(b). These results unambiguously prove that the ferroelectric polarization can permanently modulate the electronic properties of the $MoS_2/MoTe_2$ heterojunction, which thus leads to the non-volatile memory function. A high on-off ratio exceeding 10^5 can be obtained in the proposed VT-FeFET by reversible switching of the ferroelectric layer, see Figure 3(c). The HRS and LRS of the VT-FeFET as set by -15 and 15 V gate voltage pulses, respectively, demonstrate time-dependent stability for at least 1000 s. This indicates a great retention attribute of the proposed device, which is essential for practical non-volatile memory applications. Memories should endure a large number of voltage cycles during the frequent data writing process. We performed endurance

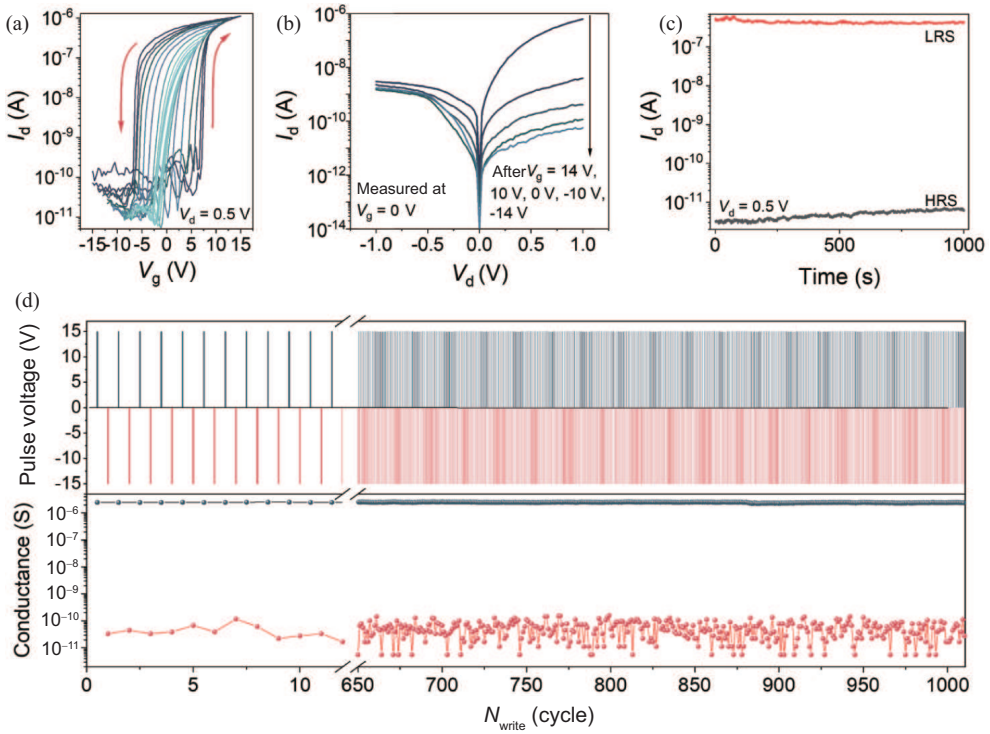

Figure 3 (Color online) VT-FeFET as a non-volatile memory. (a) Transfer curves of the VT-FeFET as a function of applied gate voltages. Hysteretic drain current switching at high gate voltage indicates the typical non-volatile memory effect. (b) Output curves of the VT-FeFET measured at zero gate voltage, after the application of different gate voltage pulses of a fixed duration at 50 ms. (c) The retention time of the VT-FeFET at HRS and LRS states after applying 50 ms long −15 and 15 V gate voltage pulses, respectively. (d) Reversible resistance switching of the VT-FeFET for 1000 cycles. The consecutive gate voltage pulses (50 ms long) are separated by a 0.5 s interval. The read voltage is 0.5 V.

measurements over 1000 write cycles by reversibly switching the device using −15 and 15 V gate voltage pulses. As depicted in Figure 3(d), the proposed VT-FeFET demonstrates high stability during voltage switching cycles where no obvious conduction variation can be observed. The above results suggest that the proposed VT-FeFETs are of great non-volatile memory performance metrics, positioning them as a potential alternative solid-state memory device concept to the existing transistor-type memories such as planar FeFETs and floating-gate transistor memories.

Having demonstrated the non-volatile memory properties of the VT-FeFET, we now show that the proposed device can be further used as a synaptic device. As shown in Figure 4(a), corresponding to the applied gate voltage amplitude and numbers, the VT-FeFET shows a gradual change of the device conductance, which is beyond the simple two memory states as presented in Figure 3. The presented conductance switching behavior is related to the mixed ferroelectric domain states in the P(VDF-TrFE) layer, which results in different remanent polarization values and thus a number of doping levels in the semiconductor channel [30]. This can be verified by measuring the retention properties of different conductance states in the fabricated device (see Figure 4(b)), which indicates that the mixed domain states along with the multiple conductance states in the proposed VT-FeFET are stable against time. Such a dynamic conduction state switching in the proposed VT-FeFET features several prominent characteristics of a memristive device [5], including multiple states, non-volatile switching, and amplitude dependence, thus firmly suggesting that this device could behave as a memristive transistor. Moreover, the memristive-type analog conductance switching behavior is reminiscent of the synaptic plasticity in biological synapses, which renders the VT-FeFET an equivalent electronic element to the synapse. To verify the stability of the VT-FeFET as a synaptic device, we carried out repeatable long-term potentiation (LTP) and depression (LTD) tests with 32 non-volatile states in a specific conductance range between 1 and 40 nS, see Figure 4(c). The obtained LTP/LTD cycles demonstrated negligible cycle-to-cycle variation, indicating excellent durability of the VT-FeFETs.

Lastly, based on the LTP/LTD results of the VT-FeFET, the performance of the supervised learning using a back-propagation algorithm ANN simulator has been evaluated, see Figure 5(a). The ANN

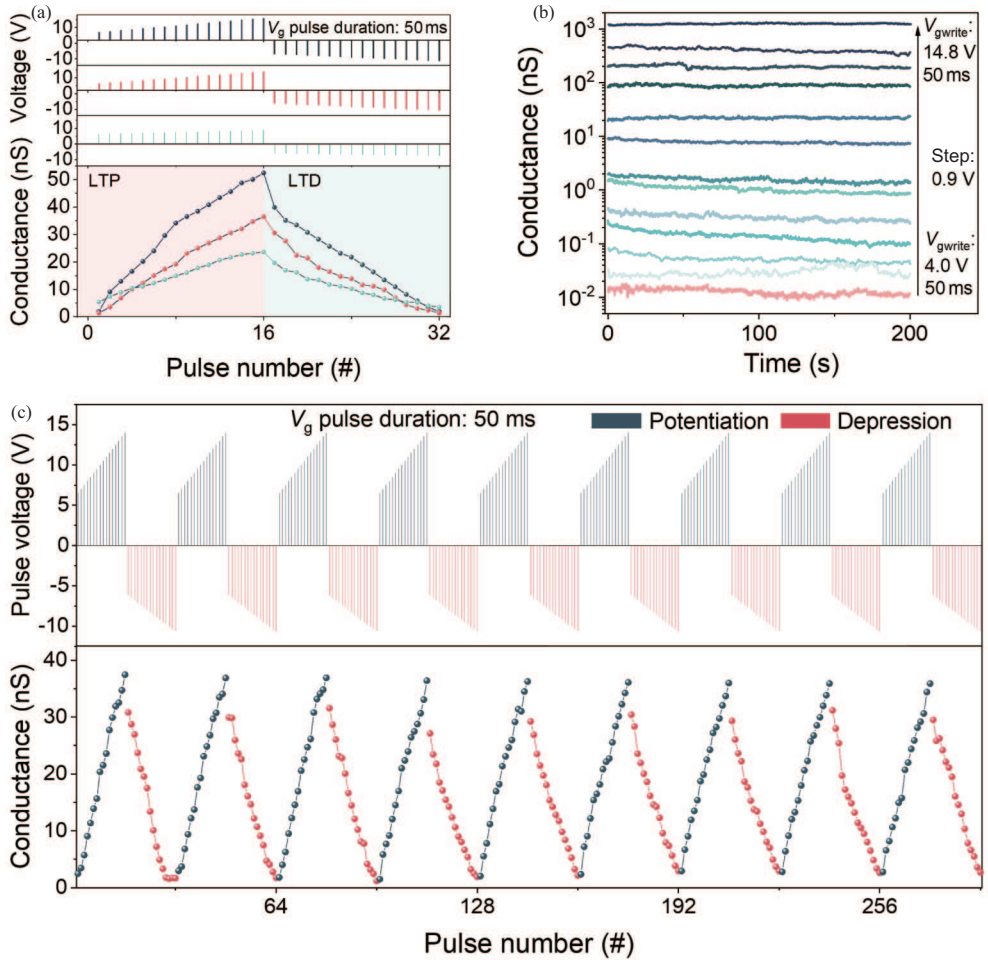

Figure 4 (Color online) Memristive properties of the VT-FeFET. (a) Gradual conductance switching as a function of voltage pulse amplitude and numbers. From the top panel to the bottom panel, the applied gate voltage schemes are: V_g pulse ranging from 7 V (−6.8 V) to 16 V (−11.3 V) in a step size of 0.6 V (−0.3 V), top panel; V_g pulse ranging from 6.5 V (−6.2 V) to 14 V (−10.7 V) in a step size of 0.5 V (−0.3 V), middle panel; V_g pulse ranging from 6.35 V (−6 V) to 8.6 V (−7.5 V) in a step size of 0.15 V (−0.1 V), bottom panel. All the voltage pulses are fixed at 50 ms. (b) Multiple non-volatile conductance levels of the VT-FeFET. V_{reset} pulse: −15 V, 50 ms; V_{read} = 0.5 V. The gate voltage pulses used for modulation of the device conductance states vary from 4 to 14.8 V at a step size of 0.9 V. (c) Long-term potentiation and depression with 32 discrete states for 9 cycles. The voltage pulse scheme for potentiation (depression) is 6.5 V (−6.2 V) to 14 V (−10.7 V) in a step size of 0.5 V (−0.3 V). The read voltage is 0.5 V for all the measurements.

was trained using the Modified National Institute of Standards and Technology (MNIST) handwritten digits [31]. Nonlinearity in the nonideal LTP/LTD weight updating scheme would significantly influence the learning accuracy, so it is crucial to improve the device properties accordingly. For the proposed VT-FeFET, we have successfully applied the asymmetric voltage pulsing scheme to suppress the nonlinearity of the weight updating process [32], see Figure 4(d). As demonstrated in Figure 5(b), this unique voltage pulsing scheme leads to largely improved LTP/LTD properties, resulting in a nonlinearity (α) of 0.06 and 0.43 for LTP and LTD processes, respectively. A detailed discussion of the nonlinearity calculation is presented in the Supplementary Note 4. For the ANN simulation, the multiply-and-accumulate (MAC) operation is achieved using Kirchhoff's law and Ohm's law, where the input voltage and the corresponding conductance in a crossbar array are processed parallelly [33]. Here, 32 states have been selected to map the neural network parameters. The neural network was trained on 60000 selected images from the MNIST dataset, and the remaining 10000 images in the MNIST dataset were used for performance validation. We employed the widely adopted training scheme, which consists of 50 epochs using a stochastic gradient decent optimizer with an early stop strategy. With float-based operators, the computer software achieved an accuracy of 98.27%. With the 32 conduction states as presented in Figure 5(b), the neural network based on our device is capable of performing 5-bit float operations, which achieved a high recognition accuracy of 92.27%. It is also necessary to investigate the tolerance of the VT-FeFET-based ANN

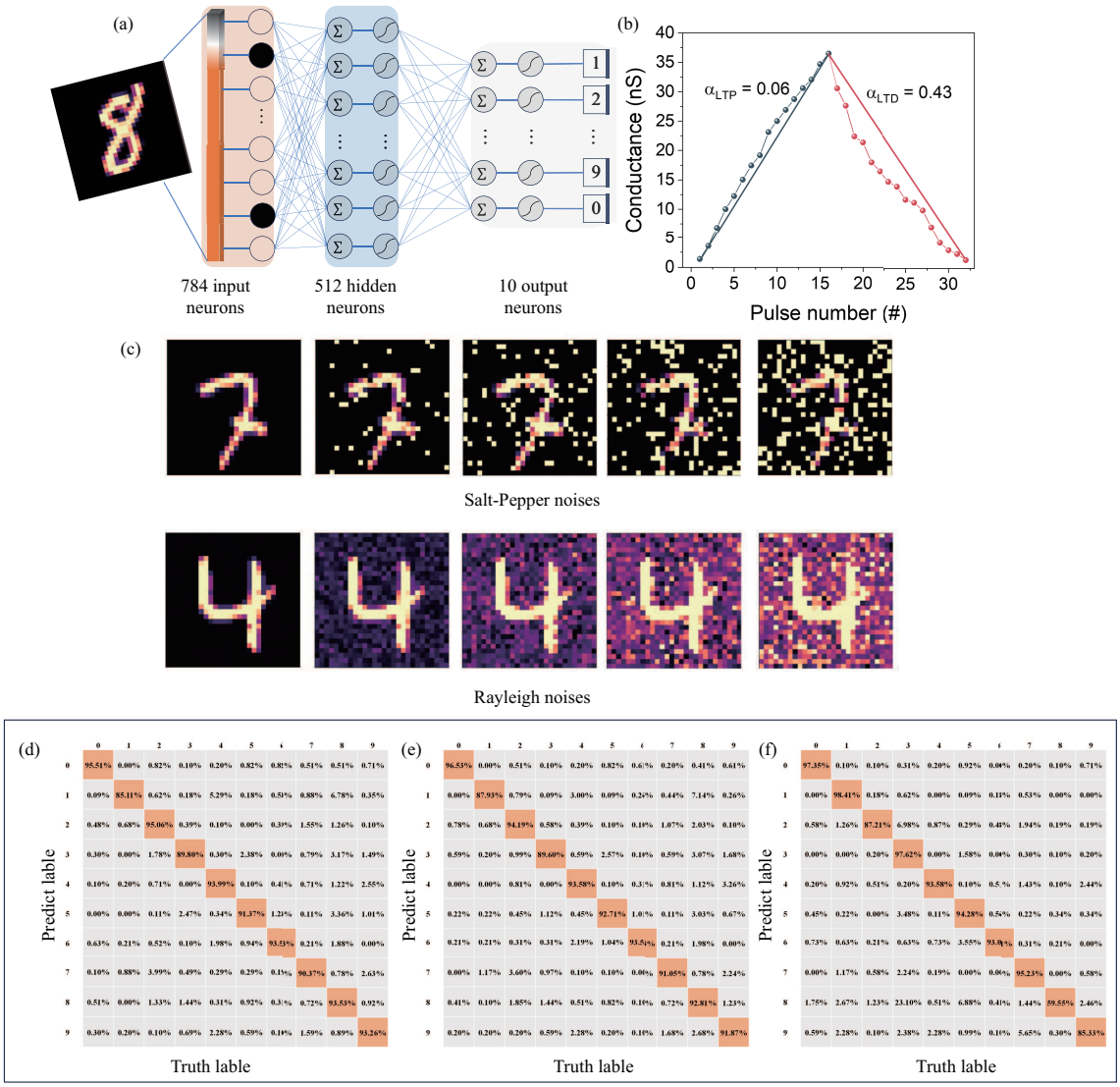

Figure 5 (Color online) ANN simulation based on the LTP/LTD properties of the VT-FeFET. (a) Schematic illustration of the back-propagation algorithm-based three-layer deep learning ANN simulator. (b) LTP/LTD used for the simulation. In contrast with the perfectly linear weight updating (the dashed line), the measured LTP and LTD have a low nonlinearity of 0.06 and 0.43, respectively. (c) MNIST handwritten digit images with Salt-Pepper noise and Rayleigh noise for different levels. The simulated confusion matrix results obtained by adding no noise (d), Salt-pepper noise at $\gamma = 0.85$ (e), and Rayleigh noises at $\varsigma = 80$ (f), respectively.

against environmental noise to verify its robustness. We thus further carried out the ANN simulation on the MNIST database with different levels of Salt-Pepper noises and Rayleigh noises, see Figure 5(c). For Salt-Pepper noise, the grayscales of some randomly chosen pixels were set to be white or black, and the ratio γ of the chosen pixel number to the total pixel number is defined as the noise level. For Rayleigh noise, noises sampled from a Rayleigh distribution with scale ζ were added to the images, and the scale ζ is defined as the noise level for Rayleigh noise. As can be seen from Figures 5(d)–(f), with Salt-Pepper noises and Rayleigh noises introduced, the recognition task became more challenging. Impressively, the ANN simulations based on the results of VT-FeFET still present robust performance with accuracy drops only within 2% under $\gamma = 0.85$ and $\zeta = 80$. The presented stable and excellent recognition rate validates the advantages of VT-FeFET synaptic devices for practical neuromorphic computing architectures.

3 Conclusion

To summarize, we have shown a new type of solid-state non-volatile memory based on the vdW heterostructure VT-FeFETs. The proposed device concept combines the advantages of the FeFETs and

vdW heterostructure-based vertical transistors, which lead to excellent non-volatile memory properties as well as significantly reduced device footprints. Beyond the robust binary memory states with a large on-off ratio exceeding 10^5, the proposed device also shows synaptic functionalities with continuously tunable resistance states. The LTP/LTD weight updating scheme was further exploited to enable the ANN simulation at the system level, which demonstrates excellent recognition accuracy of MNIST handwritten digits even against a noisy environment. Overall, we believe that the vdW heterostructure-based VT-FeFETs may pave the way for the downscaling of transistor-type solid-state memories, and further provide a versatile platform for in-memory computation applications.

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Supporting information Supplementary Notes 1–7. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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