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• **Supplementary File** •

Solid-state nonvolatile memories based on vdW heterostructure-based vertical-transport ferroelectric field-effect transistors

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1 Supplementary note 1: Fabrication process for the VT-FeFET

The graphene, MoS_2 and $MoTe_2$ flakes were mechanically exfoliated onto polydimethylsiloxane (PDMS, Gel-Pak@) stamps using the Scotch tape method. The graphene flakes were transferred via PDMS stamps onto the 285 nm SiO_2/Si substrates. And then the $MoTe_2$ and MoS_2 flakes were transferred onto the graphene flakes of interest to form the MoS_2/$MoTe_2$/graphene heterostructures by dry transfer method using a location-precise transfer platform. After each transfer step, the sample was annealed at 200 ℃ in vacuum for 1 h to remove polymer residue. Au electrodes pre-defined by photolithography on Si substrate were transferred using PDMS onto the 2D flakes to form the source contact on MoS_2 and contact on graphene. The as-fabricated VT-FETs were annealed at 200 ℃ in vacuum for 2 h to improve the contact between the transferred metal electrodes and 2D materials. Next, two-layer P(VDF-TrFE) (70:30 in mol%) thin films (∼100 nm in thickness) as gate dielectric layer were spin coated to the sample for two times, followed by an annealing at 135 ℃ in vacuum for 6 h. Au metal stripes were transferred onto the vertical channel by dry transfer method, and the Au/P(VDF-TrFE)/MoS_2/$MoTe_2$/graphene structures were finally annealed at 120℃ in vacuum for 1 h.

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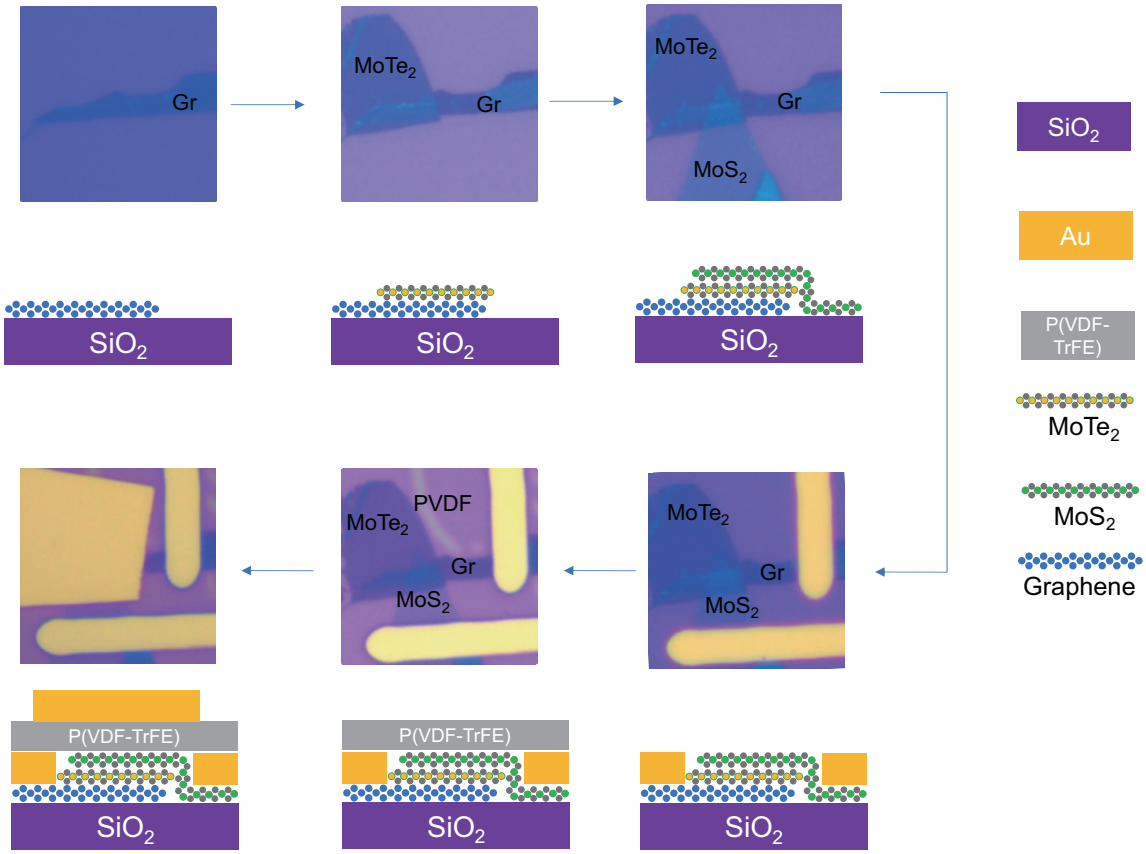

Figure 1 The optical image of fabrication process for the VT-FeFETs.

2 Supplementary note 2: P-V hysteresis loop of P(VDF-TrFE) capacitor

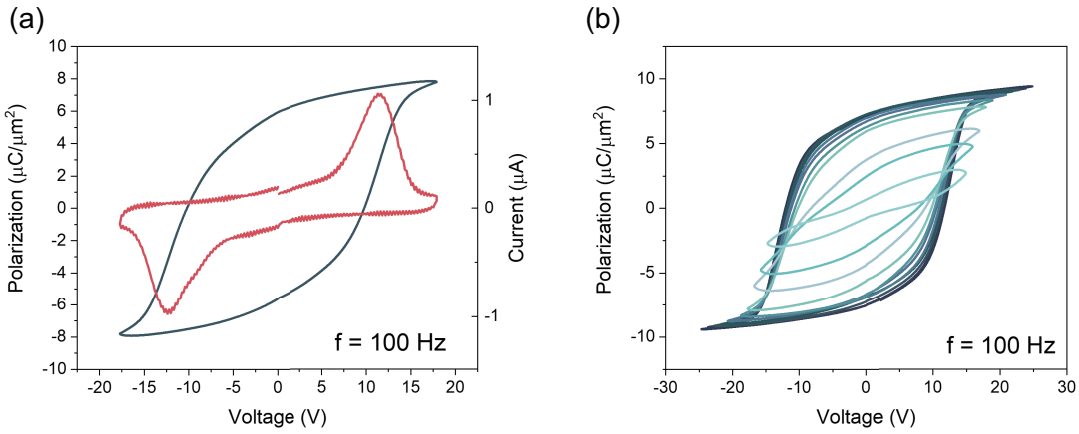

Figure 2 Ferroelectric hysteresis loop of Au/P(VDF-TrFE) (100 nm)/Si capacitor. (a) Ferroelectric hysteresis loop and polarization switching current measured at 100 Hz. (b) A set of ferroelectric minor loops measured at different sweeping voltage at 100 Hz. The ferroelectric minor loops indicate that P(VDF-TrFE) films can exhibit multiple polarization levels, which is the physical origin for the realization of memristive switching in P(VDF-TrFE) based VT-FeFET.

3 Supplementary note 3: Transfer characteristics at different memory states for VT-FeFETs

As the ferroelectric P(VDF-TrFE) thin film is biased in the linear dielectric regime, the VT-FeFETs show an electrostatic doping effect that is the same as the conventional linear dielectrics. As shown in Fig. S3a, the Vth with the memory states, which is generated from the polarization orientation. As the ferroelectric P(VDF-TrFE) gate is biased in the linear dielectric regime, e.g. the VT-FeFET operates in a regular FET mode, the repeatedly measured transfer curves remain a stable V_{th} for up to 20 cycles.

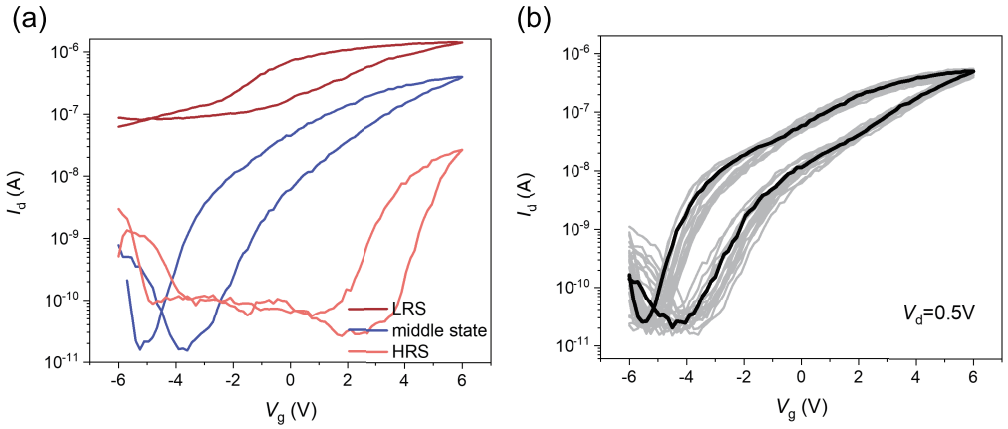

Figure 3 Transfer curves of the P(VDF-TrFE)/MoS_2/$MoTe_2$ VT-FeFET (a) Transfer curves under different memory states. (b) Vg sweeping cycle at regular FET mode.

4 Supplementary note 4: Calculation of nonlinearity in weight updating process

An ideal weight update characteristic of synapse should be linearly proportional to the number of programming voltage pulses. However, realistic devices reported in the literatures do not follow this ideal curve, and the conductance typically changes rapidly at the beginning of LTP and LTD and then gradually saturates. We have adopted a device behaviour model [1] to capture the nonlinear weight update behaviour, where the variation of conductance with the number of pulses (P) is described by the following formulas:

$$G_P = B(1 - e^{-P/A}) + G_{min} \tag{1}$$

$$G_D = -B(1 - e^{P-P_{max}/A}) + G_{max} \tag{2}$$

$$B = (G_{max} - G_{min})(1 - e^{-P_{max}/A}) \tag{3}$$

$$\alpha = 1.726/(A + 0.162) \tag{4}$$

Here, G_P and G_D are conductance of LTP and LTD. G_{max} represents the maximum conductance value, G_{min} is the minimum conductance value and P_{max} is the maximum pulse number to switch between the maximum and minimum conductance states, which are all extracted from the experimental data. A is a parameter that controls the nonlinear behaviour of weight updates, which can be positive or negative. B is a function of A which fits the range of memristive switching. The nonlinear parameter A is obtained by fitting the curve with LTP and LTD. α is a parameter describing the nonlinearity of weight update. The higher α is, the more nonlinear the curve is. [2]

5 Supplementary note 5: Current density for the VT-FeFET

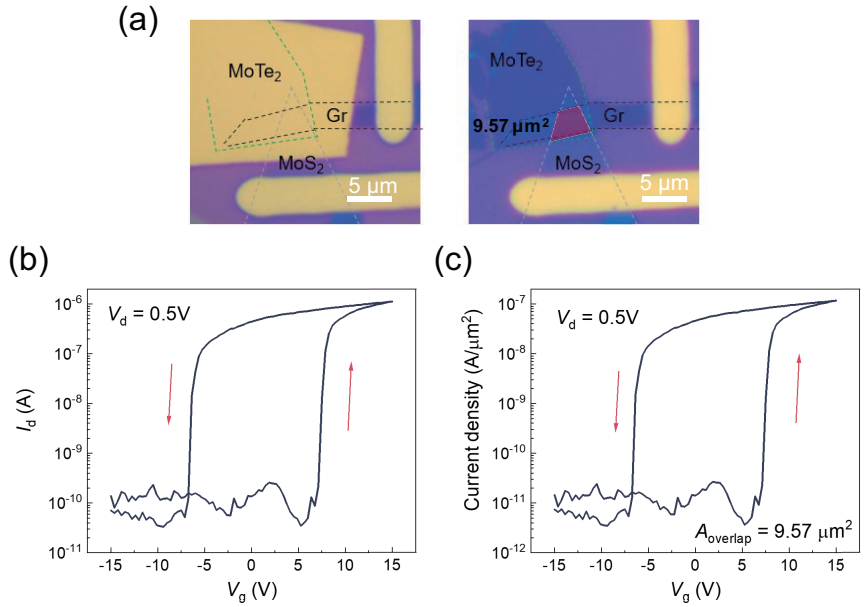

Figure 4 Current density of VT-FeFET. (a) Illustration of the $MoS_2/MoTe_2$ overlapping area. The heterojunction region is highlighted in red. (b) Transfer curve of VT-FeFET. The vertical axis represents drain current (a) Current density calculated form transfer curve in (b).

6 Supplementary note 6: Operation mechanism for VTFETs

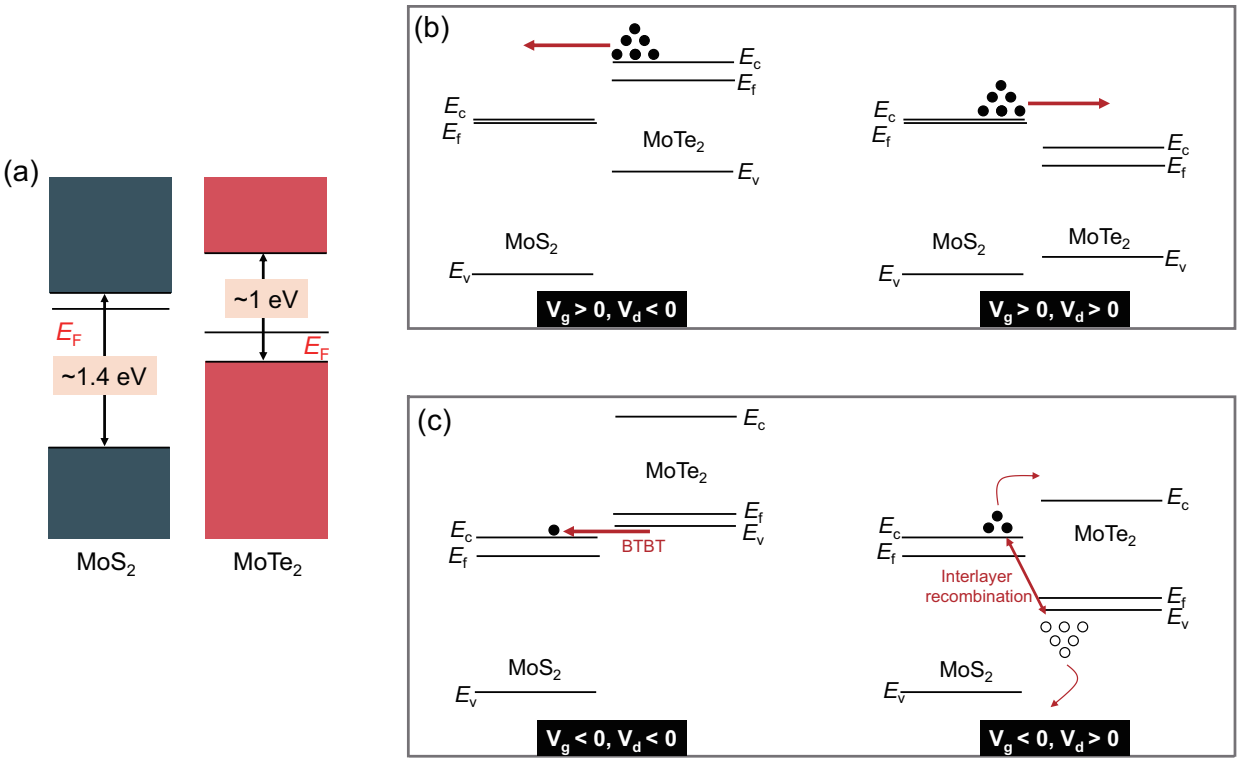

Figure 5 Band profiles of the $MoS_2/MoTe_2$ VTFET under different conditions. (a) Band diagram of MoS2/MoTe2 heterojunction before contact. (b) Band diagram of the $MoS_2/MoTe_2$ heterojunction under different applied gate and drain voltage.

7 Supplementary note 7: Benchmark the device performance metrics of 2D FeFETs

Table 1 Benchmark of the device performance metrics of 2D FeFETs

Structure	Material	On/Off ratio	Conductance states	Endurance (cycles)
MFS LT-FeFET [3]	PZT/WS_2	NA	10	NA
MFS LT-FeFET [4]	pSi/HZO/MoS_2	10^5	40	NA
MFS LT-FeFET [5]	pSi/HZO/SnS_2	10^6	64	1.4×10^4
MFS LT-FeFET [6]	Au/Ni/$CuInP_2S_6$/MoS_2	$>10^3$	NA	NA
Dual-gate MFS LT-FeFET [7]	Au/P(VDF-TrFE)/MoS_2	10^5	100	NA
MFIS LT-FeFET [8]	Au/$CuInP_2S_6$/hBN/InSe	$>10^4$	NA	1×10^3
MFIS LT-FeFET [9]	Gate/$CuInP_2S_6$/hBN/ReS_2	104	25	NA
MFIS LT-FeFET [10]	Au/$CuInP_2S_6$/hBN/WSe_2	10^4	NA	NA
MFMIS LT-FeFET [11]	W/HZO/W/Al_2O_3/MoS_2	10^7	64	5×10^4
MFMIS LT-FeFET [12]	$CuInP_2S_6$/Gr/hBN/Te	10^3	NA	NA
Ferroelectric semiconductor channel LT-FeFET [13]	Au/hBN/3R MoS_2/Graphene	10^6	NA	1×10^4
Ferroelectric semiconductor channel LT-FeFET [14]	Au/hBN/α-In_2Se_3	10^3	30	500
Ferroelectric semiconductor channel LT-FeFET [15]	pSi/HfO_2/α-In_2Se_3 pSi/SiO_2/α-In_2Se_3	10^8	NA	NA
Vertical channel MFS VT-FeFET (This work)	Au/P(VDF-TrFE)/ MoS_2/$MoTe_2$/Gr	$>10^4$	16	1×10^3

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