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• RESEARCH PAPER •
Special Topic: Silicon-compatible 2D Materials Technologies

Heterogeneous integration of 2D materials on Si charge-coupled devices as optical memory

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Abstract Optical memory integrates the function of optical sensing in memory devices, remarkably promoting the interconnection between sensory and memory terminals. Silicon charge-coupled photodetectors and floating gate memory have been widely used in imaging and storage technologies, respectively. However, the heterogeneous integration of the two devices requires technological innovation and complex electrical connections. In this work, we adopt a three-dimensional layer stacking method to design a novel optical memory device. On the top of Si charge-coupled photodetectors, we successively deposit two-dimensional graphene, hexagonal boron nitride, and molybdenum disulfide as a floating gate layer, a tunneling layer, and a readout layer, respectively. By applying a gate bias on lightly doped Si, a deep depletion layer is formed with a high voltage potential drop. Under dark conditions, the depletion layer cannot be filled, and the electric field across the h-BN tunnel barrier is relatively small. Under light irradiation, the deep depletion layer is gradually filled, and the h-BN tunneling layer withstands the increasing electric field, resulting in charge storage in the floating gate layer. Based on this mechanism, the device exhibits a gate voltage-dependent operation mode, including an integrated optical sensing-memory mode and an electrically driven storage mode. Under moderate gate voltage, the device can effectively detect the optical information with varied intensity and store the optical information in the floating gate, displaying optically controlled memory characteristics. Our work demonstrates a compact device structure for optical memory and displays excellent optically controlled memory performance, which can be applied in artificial vision systems.

Keywords heterogeneous integration, charge-coupled device, floating gate, optical memory, molybdenum disulfide, lightly doped silicon

1 Introduction

Toward the trend of "More than Moore" technologies, functional diversification is highly demanded for electron devices that can collect (sensors), store (memories), and process (computing units) information [1–8]. A device that integrates the function of optical sensing and data storage can accelerate the image data processing in both data center and edge devices, which makes it a valuable component for future energy-efficient and miniaturized electronic systems [9–13]. Although traditional silicon-based sensor and storage technologies are well-established, the heterogeneous integration of sensors and memories requires technological innovation and complex electrical connections. Time latency and power consumption act as a bottleneck to impede further optimization of the system [14]. It is imperative to break through conventional architectures and achieve the integration of diverse functionalities within a single device. Silicon-based charge-coupled devices (CCD), such as widely used photodetectors, convert incident light signals into charge outputs featuring high responsivity and low noise [15–17]. These advantages position silicon-based CCD as photosensitive components in cameras for high-quality imaging, such as space photography [18]. Floating gate memory, the commercially employed storage device, displays excellent long-term storage capabilities [19, 20]. Gate voltage can control the tunneling of channel carriers across the tunnel barrier into the floating gate and program the channel conductivity between high- and low-conductance states [21, 22]. It is promising to design a compact device structure to integrate silicon-based

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CCD and floating gate memory. Two-dimensional (2D) materials, owing to their unique layered structure, high mobility, and tunable bandgap, have attracted widespread attention [23–25]. Because of the van der Waals interaction between layers, 2D materials can overcome the constraint of lattice matching, rendering them pivotal constituents for fabricating Si-2D heterogeneous integrated devices with multifunctionality [26–29]. Furthermore, the Si-2D device is compatible with the silicon fabrication process, making it suitable for achieving multifunctional integration [30, 31].

In this work, we successively place graphene, hexagonal boron nitride (h-BN), and molybdenum disulfide (MoS_2) on the SiO_2/Si (lightly doped) substrate. The deep depletion region at the interface between lightly doped Si and SiO_2 acts as charge-coupled photodetectors, and 2D heterostructures work as floating gate memory. The device achieves the switching between high- and low-conductance states by controlling the electric field across the h-BN tunnel barrier. Based on this mechanism, the device exhibits gate voltage-dependent operation modes, including an integrated optical sensing-memory mode and an electrically driven storage mode. Under moderate gate voltage, the device can effectively detect optical information with varied intensity and store it in the floating gate, displaying optically controlled memory characteristics. Furthermore, the use of light and electrical pulses as dual input signals can realize NAND logic gates. Our work demonstrates a compact device structure for optical memory and shows the potential application of optical memory in artificial vision systems.

2 Materials and methods

To fabricate optical memory devices, we use lightly n-doped Si with 100-nm-thick thermal oxide as the substrate; the resistivity of the lightly doped n-type Si wafer is 1–10 $\Omega \cdot$ cm. Few-layer two-dimensional materials, including graphene (∼3 nm thick), hexagonal boron nitride (∼15 nm thick), and molybdenum disulfide (∼3 nm thick), were successively mechanically exfoliated onto thin polydimethylsiloxane (PDMS) and then precisely stacked on the substrate using the dry transfer method to form van der Waals heterostructures. The metal contacts were patterned by laser direct writing, followed by the thermal evaporation of a 40-nm-thick gold layer as a source and drain electrode.

3 Results and discussion

Figure 1(a) shows the schematic of the device structure. The device contains three functional units. The bottom unit comprises n-type lightly doped silicon/100-nm-thick silicon dioxide, which serves as the photosensitive layer. The middle unit displays the function of charge storage, which is composed of graphene as the floating gate and h-BN as the tunnel barrier. The top layer employs MoS_2 as the channel to read out the current signal. Figure 1(b) displays the optical microscopic image of the fabricated device, in which graphene (marked by the white dashed line) is placed directly on the substrate, followed by the sequential stacking of h-BN (marked by the blue dashed line) and MoS_2 (marked by the red dashed line) on top of the graphene and the h-BN layer. The source and drain electrodes are used to read out the channel conductivity, and the bottom Si layer works as the gate electrode.

By applying a positive gate bias on the Si, the lightly doped Si can be driven into a nonequilibrium deep-depletion state. A potential well is formed in the SiO_2/Si interface for photon absorption and charge integration. Under dark conditions, the majority of the electric potential drops at the potential well, leading to a low electric field across the tunnel barrier. Upon receiving a light signal, the photon-induced charge carriers fill the deep depletion potential well, resulting in a decreasing electric potential drop on Si and an increasing electric field across the h-BN tunnel barrier. The graphene floating gate can be charged/discharged by the electric field across the tunnel barrier, which is controlled by the light signal in our devices. The charges can be retained in the graphene layer after removing the electric field, regulating the conductivity of the MoS_2 channel. Overall, the optical signal can modulate the electric field across the tunnel barrier, affect the charge tunneling between the graphene floating gate and the MoS_2 channel, and be read out from the conductivity change of the MoS_2 channel. Our optical device exhibits a distinct operating mechanism and an integrated sensing/storage functionality.

Figure 1(c) shows the typical transfer curves of the MoS_2 optical memory device. The source-drain current I_d has been acquired by sweeping the Si gate voltage (V_g) from negative to positive values and then back to negative values (±30 V), with floating graphene and a fixed drain-source bias (V_d) of 0.05 V. A memory window width (ΔV) is defined as the shift in the threshold voltage during the dual-swept V_g.

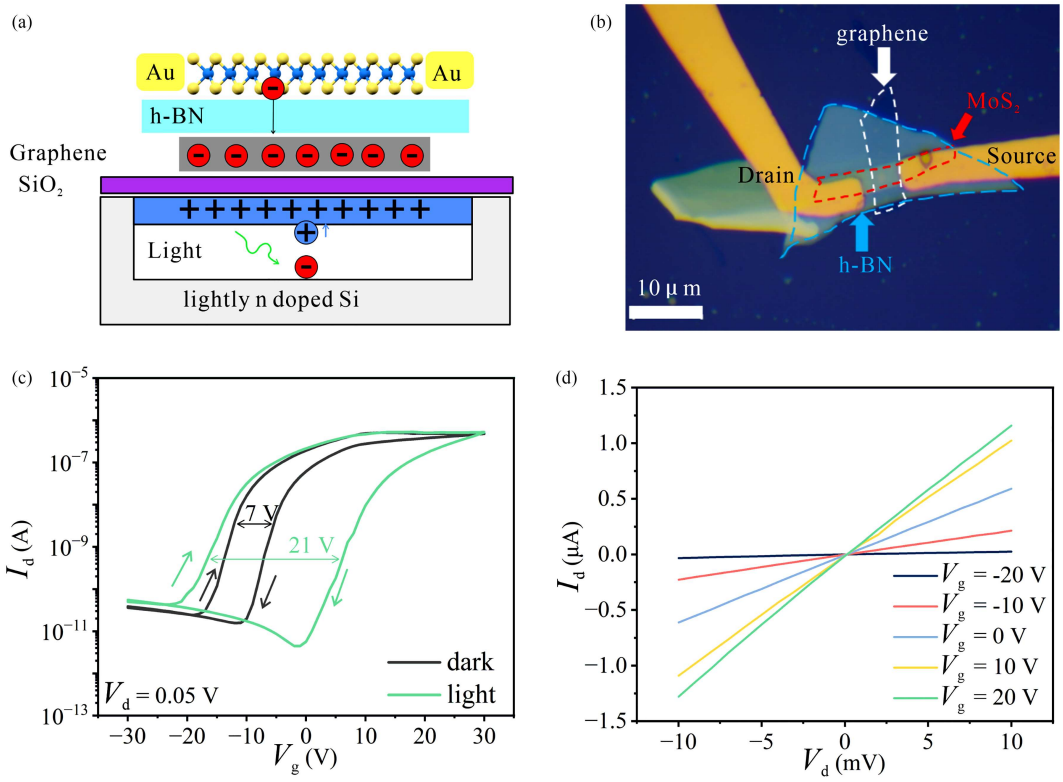

Figure 1 (Color online) Charge-coupled floating gate device. (a) Schematic illustration of the cross-sectional structure of the optical memory device; (b) optical microscopic image of the optical memory device; (c) transfer curve of the optical memory device at $V_{\rm d}$ = 0.05 V under dark (black line) conditions and 532 nm light (green line, power density 37 μW · mm^{-2}); (d) output characteristic of optical memory device under dark conditions.

The memory window under dark conditions is only 7 V, while the memory window greatly increases to 21 V under 532 nm light irradiation. We performed a control experiment by fabricating the device (graphene/100 nm SiO_2/lightly doped silicon) without the floating gate and tunnel barrier. The device displays negligible hysteresis in the transfer curve (Appendix A). We can conclude that the presence of a large memory window can be attributed to the existence of the graphene floating gate, and the size of the memory window demonstrates the electric field across the tunnel barrier and the storage capability. Under dark conditions, the deep-depleted Si withstands a large proportion of electric potential drop, leading to a small memory window and low storage capability. Under light irradiation, the deep depletion region is filled with photo-generated carriers, and the voltage drop at Si greatly decreases. It results in increased voltage drop across the floating memory region, a large memory window, and high storage capability. The corresponding charge density stored in the graphene floating gate can be estimated by $(\Delta V \times C)/q$ [32], where q is the electron charge of 1.6×10^{-19} C and C is the dielectric capacitance between the Si gate and the graphene floating gate (100 nm SiO_2) of 3.45 $\times10^{-8}$ F cm^{-2}, resulting in a value of 4.5 $\times$ 10^{12} cm^{-2}. The optically controlled memory window preliminarily proves the integrated sensing/storage function in our optical memory devices. It is worth noting that the off-state current under light irradiation is even lower than that under dark conditions. This is because, under light irradiation, the MoS_2 channel has been programmed to a high resistance state via the drive of electron tunneling into the graphene floating gate. The electric field from both the back gate and the floating gate depletes the MoS_2 channels. Furthermore, under light irradiation conditions, the transfer curve undergoes a subtle leftward shift. This phenomenon arises from the photogating effect of the MoS_2 channel. Also, it can be observed that the photocurrent in the MoS_2 layer has negligible influence on the device memory window. The output characteristic curves under dark conditions (Figure 1(d)) indicate the formation of high-quality semiconductor/metal contact in our optical memory devices.

To better understand the device mechanism, we present band structure diagrams of our optical memory device under dark and illuminated conditions in Figures 2(a) and (b), respectively. In a dark environment, a voltage on the lightly doped silicon creates a deep depletion potential well on the silicon and silicon

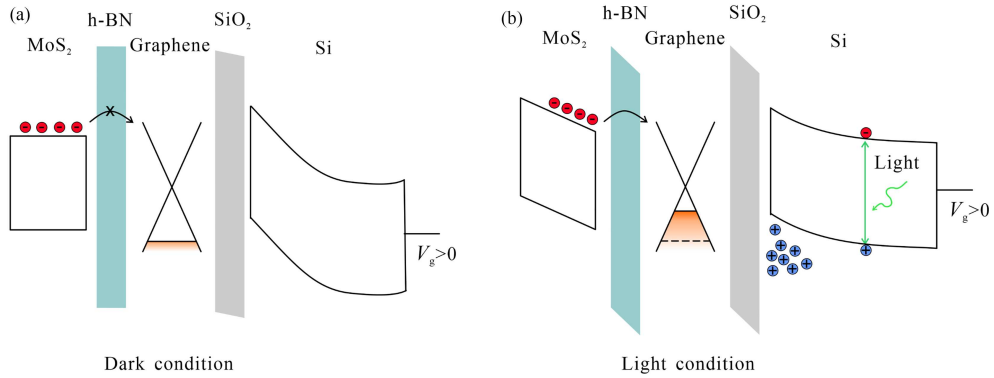

Figure 2 (Color online) Band diagram of the optical memory device. The working mechanism under (a) dark conditions and (b) light conditions.

dioxide interface. As the silicon is lightly doped, no carriers can be filled in the potential well except for those from the thermal carrier generation. The slow thermal generation rate in Si maintains the state of deep depletion for a long time. As a result, the voltage drop occurs primarily on the lightly doped silicon, which has been depicted as a large energy drop at the Si/SiO_2 interface. The electric field across the h-BN tunnel barrier is not strong enough (small energy drops in the band diagram) to induce the electrons to tunnel from the MoS_2 channel to the graphene floating gate, thus impeding non-volatile storage. Under visible light irradiation, the photogenerated electron-hole pairs separate within the Si, and the holes rapidly fill the deep depletion potential wells at the Si/SiO_2 interface. With increased light intensity or increased light exposure time, the accumulated holes inside the potential well gradually increase until the potential well is filled completely. During the filling of the potential well, the electric field across the h-BN tunnel barrier gradually increases to a threshold value (large energy drops in the band diagram) and electrons in MoS_2 start to tunnel through the h-BN layer to the graphene floating gate because of the Fowler-Nordheim (FN) tunneling effect [33]. Also, the photogenerated electron-hole pairs increase the MoS_2 carrier density and enhance the carrier tunneling. The graphene floating gate stores electrons and modulates the channel conductance. By measuring the channel conductance in dark conditions, the optical information stored in the floating gate can be read out.

In our optical memory device, the Si gate bias is an important parameter for determining the performance of the device. Figures 3(a) and (b) display the transfer curves by varying the V_g sweeping range under dark and irradiant conditions, respectively. In a dark environment (Figure 3(a)), a negligible memory window can be observed under a V_g sweeping range of ±5 and ±10 V. When the V_g sweeping range increases to ±20 V, a memory window appears. Although the deep depletion potential well withstands a large portion of potential drop, the large gate voltage bias (±20 V) induces a high electric field, which surpasses the threshold electric field across the h-BN tunnel barrier to drive the FN tunneling. Under light illumination (Figure 3(b)), an obvious memory window appears from the V_g sweeping range of ±10 V, which is consistent with the traditional 2D floating gate memory device. The V_g sweeping range is smaller than that under dark conditions to induce the memory window. Figures 3(c) and (d) depict the time-dependent channel current under 10 and -10 V gate voltage pulses under dark and irradiant conditions, respectively. Under dark conditions, 10 and -10 V gate voltage pulses (pulse width 500 ms) cannot change the conductance of the channel layer, and the channel current remains at 1.18×10^{-8} A at V_d of 0.05 V (Figure 3(c)). Under light irradiation, when 10 V gate voltage pulses are applied, the MoS_2 channel is driven to a low-conductance state. This state can be erased by applying a negative gate voltage pulse to recover the high conductance of the MoS_2 channel. The extinction ratio between the high- and low-conductance states is almost 10^2. It indicates that light information can be detected by the Si deep depletion region and stored in the floating gate under positive and negative 10 V gate voltage pulses. We further increase the gate voltage pulses to ±20 V. Figures 3(e) and (f) show the time-dependent channel current under 20 and -20 V gate voltage pulses under dark and irradiant conditions, respectively. Notably, in both dark and illuminated environments, the MoS_2 channel conductance can be switched between a high-conductance state and a low-conductance state. It shows that the gate voltage of ±20 V imparts a sufficiently large electric field across the h-BN tunnel barrier even under dark conditions, rendering light incapable of altering the stored information in the floating gate. Therefore, by varying the voltage applied to the Si gate, our device can be switched between an optical sensing-

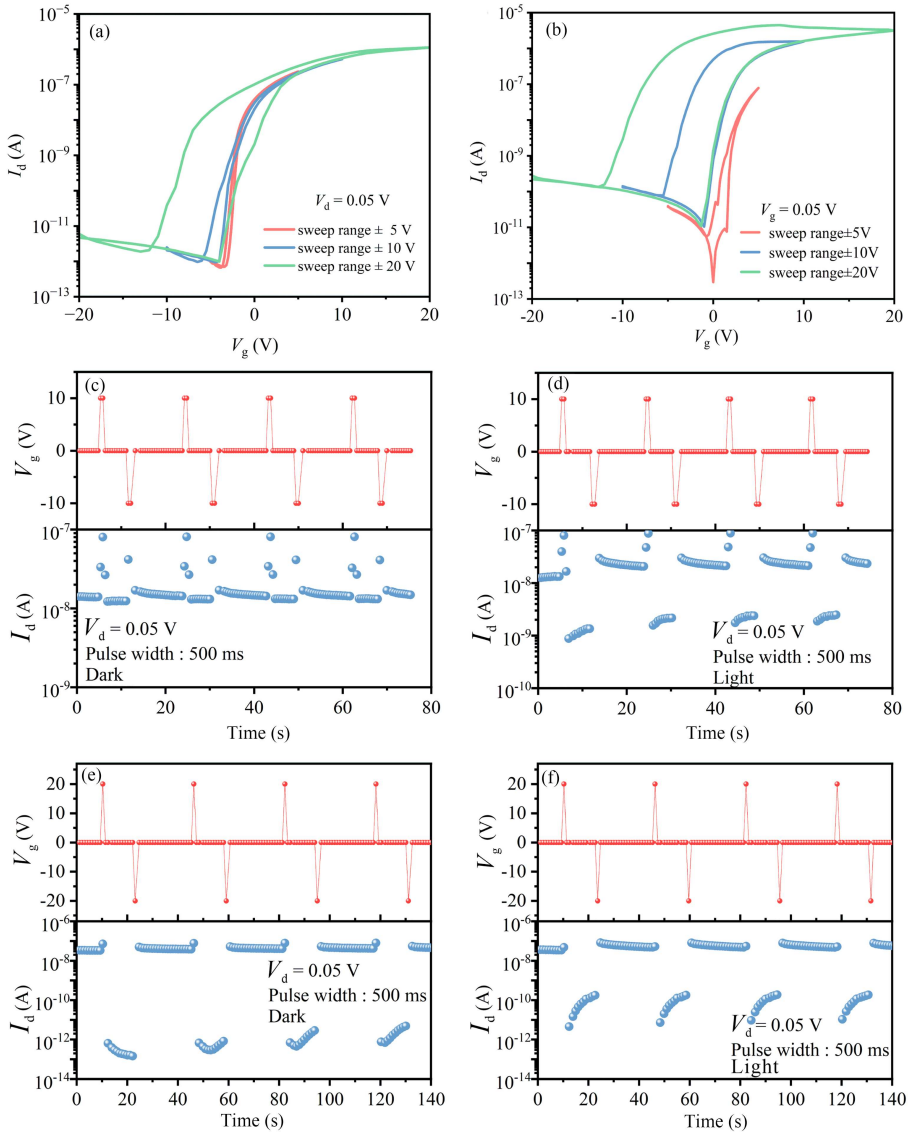

Figure 3 (Color online) Memory characteristics with varied gate voltage pulses. (a) Typical dual-sweep transfer curves of an optical memory device in (a) dark and (b) 532 nm light (power density 37 $\mu W \cdot mm^{-2}$). The plots of the drain current with time by applying gate voltage pulses of ±10 V under (c) dark and (d) light conditions (532 nm, 7 $\mu W \cdot mm^{-2}$) and by applying gate voltage pulses of ±20 V under (e) dark and (f) light conditions (532 nm, 7 $\mu W \cdot mm^{-2}$).

memory mode and an electrically driven storage mode. In the control device (Appendix A), the Si gate voltage can only change the depth of the deep depletion region; it cannot modulate the working mode of the device. By applying a gate voltage larger than +4 V, the current of the graphene channel under illumination gradually becomes smaller than that under dark conditions, indicating the formation of the deep depletion region. We can conclude that the formation of deep depletion at the Si/SiO_2 interface starts from a +4 V gate voltage bias.

Figure 4(a) illustrates the transfer characteristics of the device under different light intensities. During the sweep of gate voltage, light exposure will fill the deep depletion potential well and increase the memory window. Under dark conditions, the memory window is 7.6 V. With an increase of light intensity from 0.2 to 10 $\mu W \cdot mm^{-2}$, the memory window increases from 8 to 12 V. Figure 4(b) extracts the current ratio between the high-conductance state and the low-conductance state under different light power densities by applying a 10 V gate voltage pulse. It reveals that, under low light intensity (0.2 to 10 $\mu W \cdot mm^{-2}$), the current ratio is small, displaying negligible memory behavior. When the light intensity passes the threshold (20 $\mu W \cdot mm^{-2}$), the current ratio is proportional to the light intensity, demonstrating optically controlled memory characteristics. Figure 4(c) displays the time-dependent channel current under ±10 V

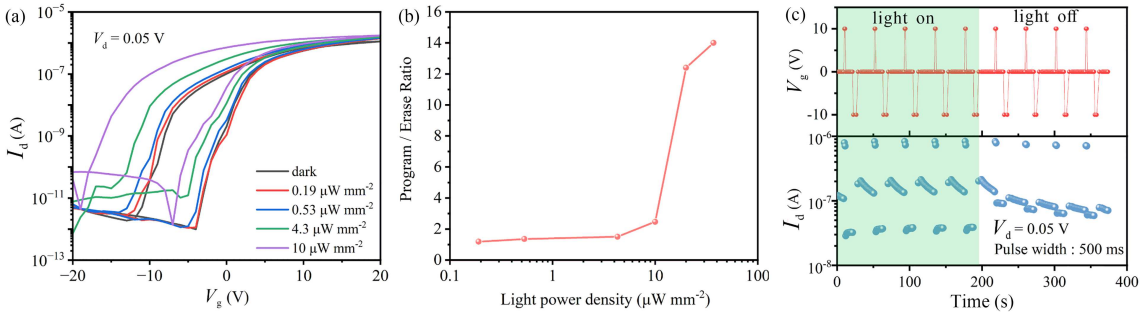

Figure 4 (Color online) Memory characteristics with varied light power density. (a) Transfer curves of the optical memory device with different light power densities; (b) Program/Erase ratio under different light power densities, which is defined as $I_{\text{erase}}/I_{\text{program}}$; (c) the plot of the drain current with time at V_{d} = 0.05 V by applying gate voltage pulses of ±10 V under light (highlighted by light green, 532 nm, 37 μW · mm^{-2} laser) and dark conditions.

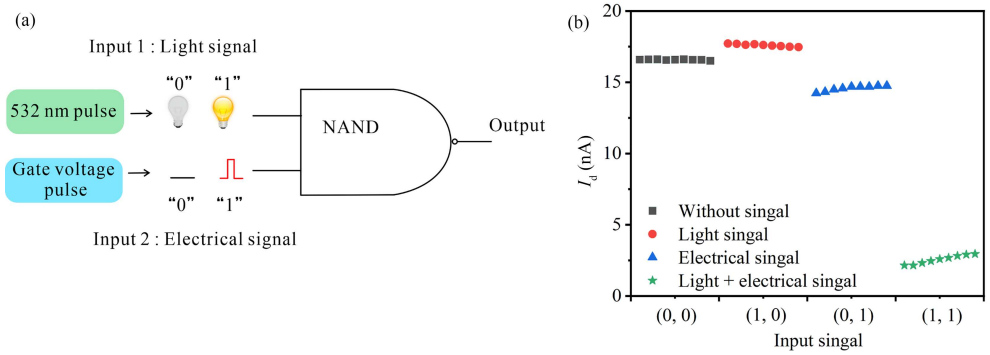

Figure 5 (Color online) Logic function of the optical memory device. (a) Schematic diagram of NAND logic gate. (b) NAND logic operation achieved by the optical memory device. Light and gate voltage pulses represent input terminal 1 and input terminal 2, respectively. The absence of both light and electrical gate pulses can be denoted by input signal "0". The introduction of light pulses, electrical pulses or both signals can be denoted by input signal "1". The high and low channel currents can be denoted by outputs "1" and "0".

gate voltage pulses with varied light conditions. When the device is exposed to light, and the Si gate is applied with a positive voltage pulse, the channel can be programmed into a low-conductance state. When the device is under dark conditions, the conduction state cannot be modulated.

Based on the device characteristics, we can achieve NAND logic functions in our device by applying input optical and electrical signals. We consider light signals and gate voltage pulses to be two independent input signals. We define the absence of light and positive electrical pulses as input signal "0" and the presence of light and electrical pulse signals as input "1". The high and low channel currents are denoted by outputs "1" and "0", as illustrated in Figure 5(a). Initially, by applying a negative gate voltage pulse, the device can restore the channel conductance to its initial value. Figure 5(b) illustrates the realization of NAND logic functionality in our device. Under dark conditions and a gate voltage of 0 V, the few-layer MoS_2 is in an accumulated state because of the intrinsic n-type doping, resulting in high conductance and an output signal "1". When only light signals or gate voltage pulse signals are applied, the device cannot be programmed to a low-conductance state, maintaining the output "1". When both light signals and gate voltage pulses are simultaneously applied, the floating gate initiates the programming process, reducing the channel current, and the output changes to "0". For large-scale fabrication, it is possible to replace graphene and h-BN with Au nanoparticles and Al_2O_3 as the floating gate and the tunneling layer, respectively. Also, the wafer-scale chemical vapor deposition (CVD) MoS_2 is the ideal channel material because of its outstanding integration ability and heterogeneous electrical characteristics.

4 Conclusion

In this work, we successfully demonstrate an optical memory by heterogeneous integration of Si-based CCD and 2D floating gate heterostructures. By systematically analyzing the working mechanism, the device exhibits gate voltage-dependent operation modes, including an integrated optical sensing-memory

mode and an electrically driven storage mode. Under moderate gate voltage, the device can simultaneously detect and store optical information, displaying optically controlled memory characteristics. Furthermore, the use of light and electrical pulses as dual input signals can realize NAND logic gates. Our work displays a novel optical memory device through Si-2D heterogeneous integration and demonstrates its potential application in artificial vision systems.

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Appendix A

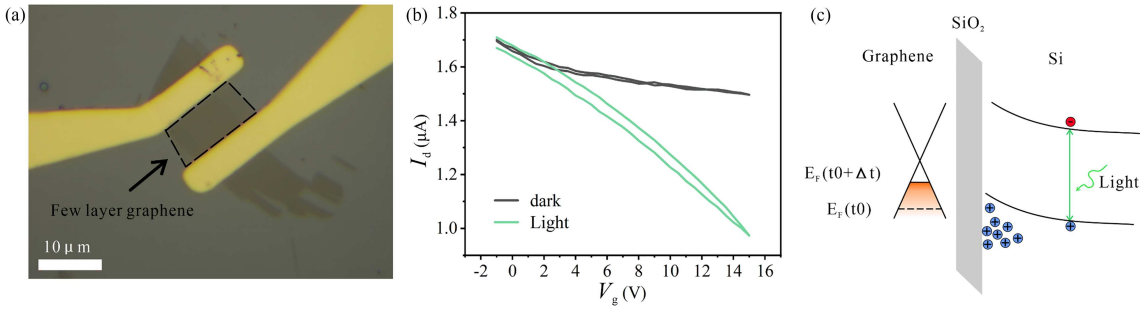

Figure A1 (Color online) (a) Optical image of the control device (graphene/SiO_2/lightly doped Si); (b) transfer curve of the control device in dark (black line) and light (green line, 532 nm, 37 μW · mm^{-2}) environments; (c) band diagram of the control device.