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• RESEARCH PAPER •
Special Topic: Silicon-compatible 2D Materials Technologies

Contact engineering for temperature stability improvement of Bi-contacted MoS_2 field effect transistors

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Abstract Semimetallic bismuth (Bi) is one of the most effective strategies for reducing the contact resistance of two-dimensional transition metal dichalcogenide field effect transistors (FETs). However, the low melting point of Bi contact (271.5°C) limits its reliable applications. In this study, we demonstrated that the temperature stability of Bi-contacted electrodes could be improved by inserting a high-melting point semimetallic antimony (Sb) between the Bi contacting layer and the gold (Au) capping layer. The proposed Bi/Sb/Au contact electrodes tended to form a metal mixture with a continuous surface during the heating process (Voids appeared on the surface of the Bi/Au contact electrodes after heating at 120°C). Because of the improved contacting layer formed by the semimetal Bi/Sb alloy, the fabricated Bi/Sb/Au-contacted molybdenum sulfide (MoS_2) FETs with different gate lengths demonstrated higher on-state current stability after heating treatment than the Bi/Au contact. Because of the Bi/Sb/Au contact and poly (methyl methacrylate) package, the MoS_2 FETs demonstrated time stability of at least two months from the almost unchanged transfer characteristics. The electrical stability indicates that the insertion of semimetallic Sb is a promising technology for reliable Bi-based contact.

Keywords temperature stability, semimetallic bismuth contact, semimetallic antimony contact, MoS_2 FETs, time stability

1 Introduction

The next generation of high-performance and low-power FETs requires that channel length and thickness be minimized while maintaining high driving current and low leakage current [1, 2][1)]. Because of the appropriate band gap and atomic-scale ultrathin thickness, two-dimensional (2D) transition metal dichalcogenides (TMDs), represented by molybdenum sulfide (MoS_2), are considered potential channel materials to avoid the short channel effect in advanced process nodes [3–6]. However, the contact resistance (R_C) at a metal-semiconductor interface remains an obstacle to the use of 2D TMD channel materials in ultimate scaling [7–9].

The high R_C of n-type transistors is mainly caused by two reasons: (1) mismatched contact metal work functions with the electronic affinity of 2D TMDs and (2) Fermi-level pinning caused by interfacial disorder and metal-semiconductor interactions [4,7,10–12]. Recently, semimetallic bismuth (Bi) and antimony (Sb) have been reported to weaken Fermi-level pinning and reduce R_C because of low-temperature deposition, suitable work functions, and near-zero density of states at the Fermi-level to suppress metal-induced gap states [4, 9, 13–16]. To minimize R_C, Bi contact is better than Sb contact for a lower work function of 4.1 eV (Sb of 4.4 eV, (0001) crystal orientation) embedded in the conduction band of MoS_2, as shown in Figure 1(a) [4]. However, the low melting point of 271.5°C of the semimetallic Bi contact severely restricts its reliable application.

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† Liu Z Z and Zhang Q have the same contribution to this work.
1) International Roadmap for Devices and Systems. https://irds.ieee.org/.

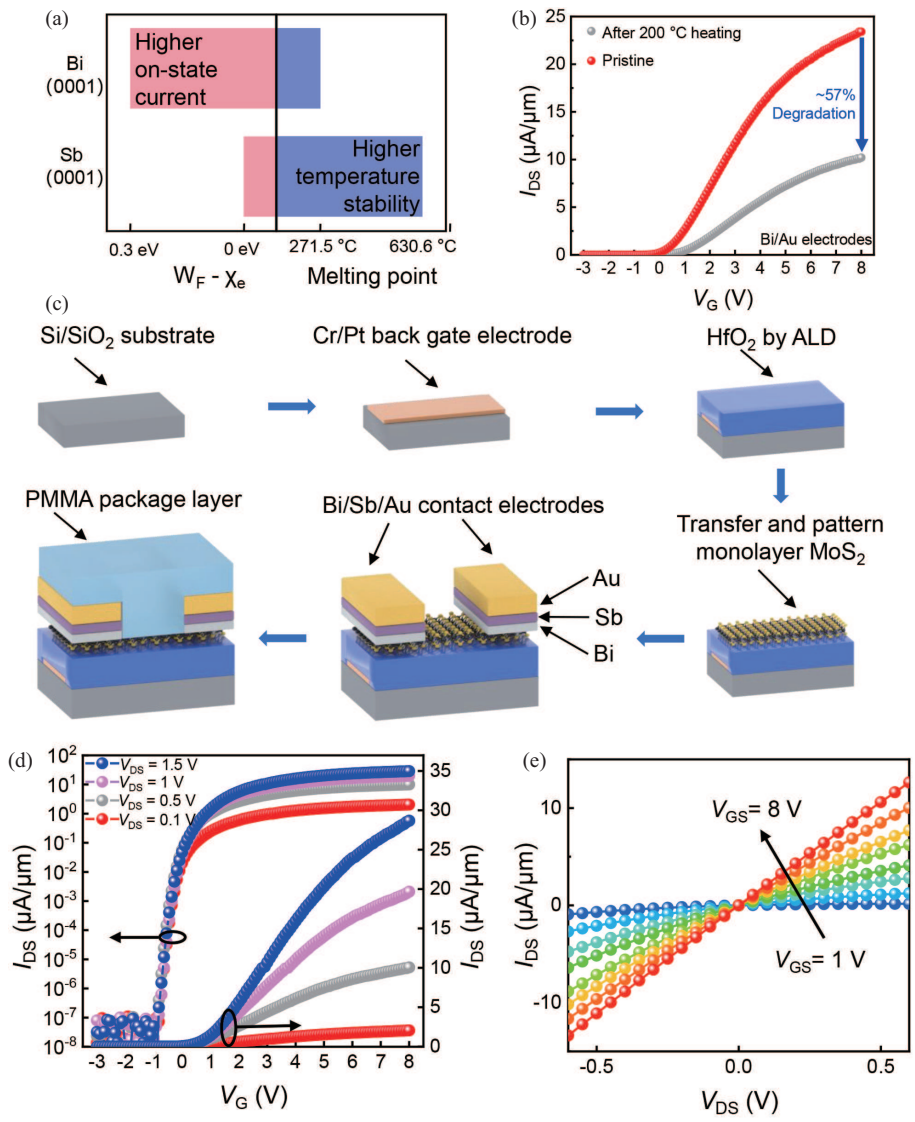

Figure 1 (Color online) (a) Schematic of comparison between Bi and Sb contacts in terms of (left) differences in the electron affinity of MoS_2 and metal work functions and (right) melting points [4,15]. (b) Transfer characteristics of a representative Bi/Au-contacted MoS_2 FET with $L_{channel}$ = 5 μm, L_{width} = 5 μm, and V_{DS} = 1 V before (red data) and after (gray data) heating at 200°C for 2 h. (c) Simplified schematic of the process flow and structure of MoS_2 FETs with Bi/Sb/Au contact electrodes. (d) Transfer characteristics of a representative Bi/Sb/Au-contacted MoS_2 FET with $L_{channel}$ = 5 μm at various V_{DS}. From top to bottom, V_{DS} = 1.5, 1, 0.5, and 0.1 V. The left axis is the logarithmic axis, and the right axis is the linear axis. (e) Output characteristics of the same MoS_2 FET in (d), where V_{GS} varies from 1 to 8 V with a step of 1 V, at room temperature.

As shown in Figure 1(b), after 200°C heating treatment for 2 h, significant degradation of approximately 57% occurred on the on-state current of the monolayer MoS_2 transistor with Bi/gold (Au) contact electrodes (the fabrication method is mentioned in the materials and methods section). The heat generated during high driving current working, multiple voltage sweeps, and long voltage bias time leads to obvious degradation of the performance of Bi-contacted MoS_2 FETs [17–19]. In addition, low-melting point contacts cannot be used practically in the silicon-based compatible back end of the line because of thermal instability. Semimetallic Sb (0001) has a higher melting point of 630.6°C but lower on-state current performance than Bi under the same external voltage bias conditions. Although a semimetallic Sb $(01\bar{1}2)$ contact has been proposed to approach R_C lower than that obtained using a semimetallic Bi (0001) contact, special electron beam evaporation (EBE) equipment with a holder heating module is required, and crystal orientation stability above 125°C has not been confirmed [9]. Therefore, improving the stability of the semimetallic Bi contact remains one of the main issues confronting MoS_2 FETs in practical applications.

In this study, we inserted semimetallic Sb between the semimetallic Bi contacting layer and Au cap-

ping layer to improve the temperature and time stability of the semimetallic Bi contact. According to the results of scanning electron microscopy (SEM), 20/20/10-nm-thick Bi/Sb/Au electrode films exhibited higher continuity after the heating process than 20/30-nm-thick Bi/Au electrode films. In addition, Bi/Sb/Au electrodes tended to form metal alloys. Cross-sectional transmission electron microscopy (TEM) images and energy-dispersive X-ray spectroscopy (EDS) element mappings revealed that the contact metal after heating was a Bi/Sb mixture. There was negligible 3.5% degeneration in the on-state currents of the MoS_2 FETs with Bi/Sb/Au contact electrodes even after heating at 200°C for 7 h, proving the higher stability of Bi/Sb/Au contact electrodes than Bi/Au contact electrodes. Furthermore, the undegraded transfer characteristics after two months demonstrated the time stability of the Bi/Sb/Au contact. This work provides a technical path for improving semimetallic contact temperature stability and application reliability without increasing process complexity and specific equipment requirements.

2 Materials and methods

Device fabrication: Figure 1(c) illustrates the main device fabrication process. First, a silicon substrate with a 300-nm SiO_2 thermal oxide film was thoroughly cleaned. A 5/15-nm-thick Cr/Pt film stack was used as a localized back gate metal by electron beam lithography (EBL) pattern/EBE/lift-off. Thermal atomic layer deposition of 20-nm HfO_2 was then performed as a dielectric by reacting tetrakis(ethylmethylamino)hafnium with water at 150°C. Subsequently, a prefabricated Au/(polyvinylpyrrolidone) (PVP)/poly (methyl methacrylate) (PMMA)/thermal release tape (TRT) stamp with a fresh and ultraflat Au surface was used to mechanically exfoliate millimeter-scale single crystal monolayer MoS_2 and transfer it onto HfO_2 [20–22]. After removing the organic and Au layers, a channel width of 5 μm was defined by EBL and O_2 plasma etching. A 20/20/30-nm-thick Bi/Sb/Au film stack was used as contact electrodes by EBL pattern/EBE/lift-off. The metal was deposited at a well-controlled deposition rate of 0.5 Å·s^{-1} at ∼10^{-7} torr. (A 20/30-nm-thick Bi/Au film stack was used to fabricate Bi/Au-contacted MoS_2 FET). Finally, a PMMA layer was spin-coated and baked at 200°C to form the package layer, which prevents device oxidation by water vapor in air [23–25]. Electrical characterization was performed at room temperature (except heating process) under ambient conditions in a probe station. The heating process was performed in a nitrogen atmosphere.

MoS_2 exfoliation and transfer: EBE 60-nm-thick Au on a silicon oxide substrate. Spin coating the PVP and PMMA solutions in sequence, and bake at 150°C for 5 min and 170°C for 3 min and 30 s, respectively. Gently apply TRT to the stack. The TRT is lifted to obtain Au/PVP/PMMA/TRT layers, and the Au surface is quickly attached to the freshly mechanically cleaved flat MoS_2 single crystal bulk material. Gently press and lift to obtain a single layer of MoS_2 on Au, which is further transferred onto the desired substrate. TRT is removed after heating at 110°C. PVP/PMMA/Au was then removed using deionized water, acetone, and gold etchant.

3 Results and discussion

Figure 1(d) shows the transfer characteristics (drain-to-source current, I_{DS}, versus gate-to-source voltage, V_{GS}) of a MoS_2 FET with a 5-μm channel length at room temperature. The device exhibits an on/off ratio exceeding 10^8 with V_{DS} over 0.5 V, a subthreshold swing of 74 mV/dec at V_{DS} = 1 V, and negligible drain-induced barrier lowering with V_{DS} ranging from 0.1 to 1.5 V. This is facilitated by the semimetallic Bi/Sb contact and the high-quality channel material of mechanically exfoliated single crystal monolayer MoS_2. The nearly linear output characteristics (drain-to-source current, I_{DS}, versus drain-to-source voltage, V_{DS}) indicate the like-Ohmic contact nature and the nearly negligible Schottky barrier height of the Bi-MoS_2 interface, as shown in Figure 1(e).

The SEM images of the metal surface morphology after heating at different temperatures were investigated to shed light on the physics mechanism of the improved stability of the Bi/Sb/Au contact electrodes. After the heating process, the surface of the Bi/Au electrodes is broken (Figures 2(a)–(d)). As the heating temperature increases, the holes become denser, which indicates the fragile temperature stability of the Bi/Au electrodes. The Bi/Au electrode surface tends to form a mixture of Bi and Au. The reduced electrode surface continuity and metal mixing due to heating inhibit the performance of the as-fabricated transistors in two aspects: (1) the conductivity of the electrode decreases, and the density

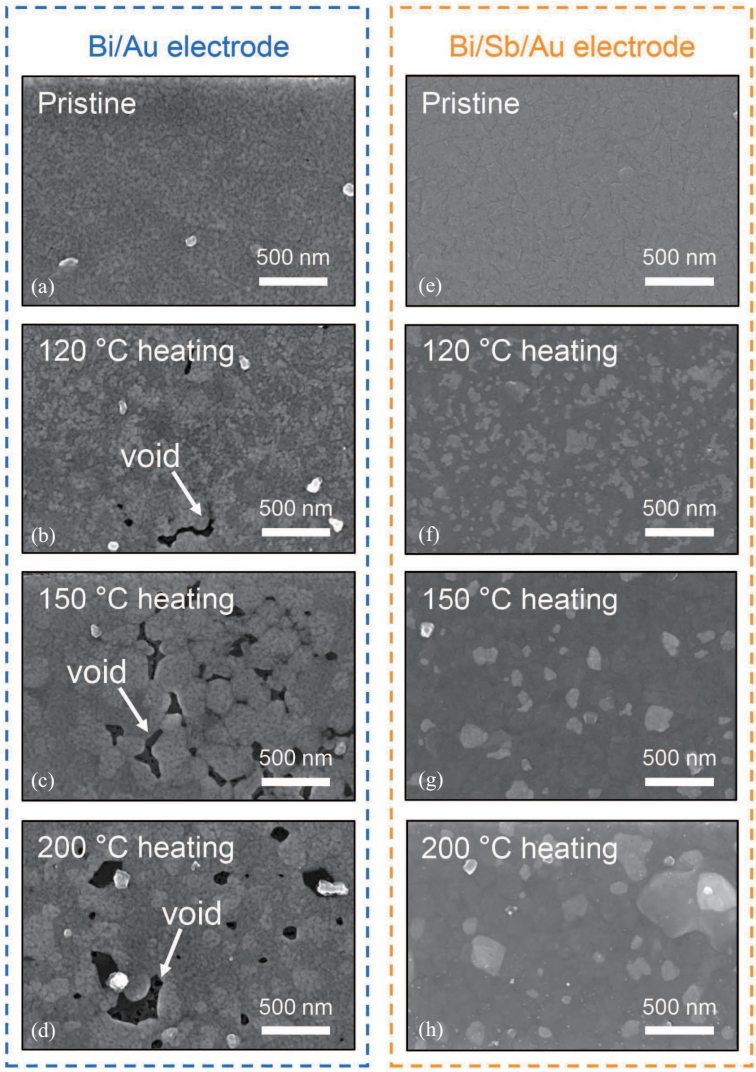

Figure 2 (Color online) Top-view SEM images of (a) pristine Bi/Au electrode and Bi/Au electrodes after heating at (b) 120°C, (c) 150°C, and (d) 200°C for 1 h. Top-view SEM images of (e) pristine Bi/Sb/Au electrode and Bi/Sb/Au electrodes after heating at (f) 120°C, (g) 150°C, and (h) 200°C for 1 h. All scale bars are 500 nm. Bi/Au electrodes are sequentially deposited with 20-nm-thick Bi and 30-nm-thick Au. Bi/Sb/Au electrodes are sequentially deposited with 20-nm-thick Bi, 20-nm-thick Sb, and 10-nm-thick Au.

of the voids on the electrode surface and the area of a single void increase with increasing heating temperature. As the conductive area of the electrode decreases, the conductivity of the Bi/Au electrodes also decreases. (2) The contact metal at the metal-MoS_2 interface: the heating process causes the actual contacting layer to change to a mixture of Bi and Au contacts, and the transfer length no longer depends only on the Bi-metal contact but on the Bi and Au mixture.

The Bi/Sb/Au electrodes exhibited good film continuity after the heating process (Figures 2(e)–(h)). Note that the change in contrast of the SEM images of the Bi/Sb/Au electrode is due to the change in the atomic number of the electrode surface atoms while heating and forming the alloy, rather than electrode damage.

The metal-MoS_2 interfacial properties determine the effective work function. Cross-sectional TEM and EDS element mappings of the Bi/Sb/Au contact regions of the MoS_2 FETs after heating at 200°C (PMMA capping layer baking temperature) are shown in Figure 3. First, the Pt of the back gate electrode does not diffuse to the HfO_2 dielectric (Figures 3(b) and (c)), which is consistent with the stability of the gate control capability of the transistors shown in Figure 4. Second, there is a mixture of Bi and Sb at the metal-MoS_2 interfacial, indicating that the effective work function depends on Bi and Sb but not on Au (Figures 3(d) and (g)). In addition, the Bi/Sb alloy has a higher melting point than Bi [26]. The lower content of Sb than the thickness set may be due to the resublimation of Sb during Au layer

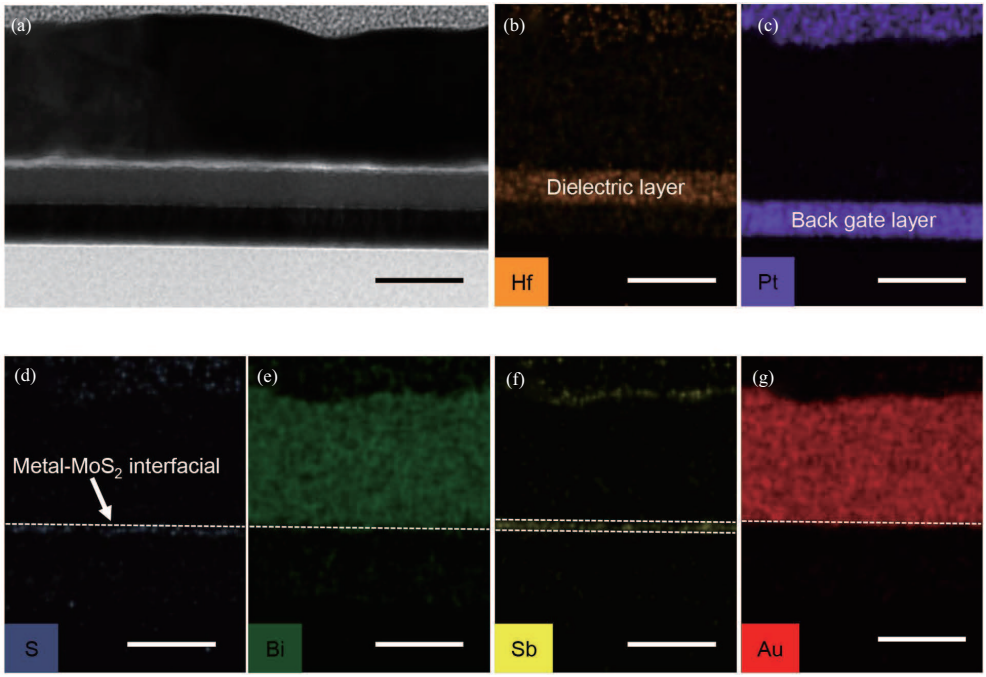

Figure 3 (Color online) (a) High-resolution cross-sectional TEM images of the contact region of a typical Bi/Sb/Au-contacted MoS_2 transistor after thermal annealing at 200°C. EDS mapping of the distribution of (b) Hf, (c) Pt, (d) S, (e) Bi, (f) Sb, and (g) Au. All scale bars are 40 nm. Note: S is observed underneath Bi and Sb, suggesting that Bi/Sb alloy contacts MoS_2. Sb is mainly distributed on the surface and bottom layer of the electrode. The middle layer of the electrode is mainly a uniform mixture of Bi and Au.

deposition. The bulk of the electrode is mainly composed of Bi and Au alloys. Sb is also observed on the upper surface of the electrode.

Based on the metal temperature stability characteristics, we evaluated the stability of MoS_2 FETs with Bi/Sb/Au contact electrodes. To fully determine the potential of the Bi/Sb/Au contact electrodes, we fabricated a MoS_2 FET with Lchannel from 5-μm scaling to 500 nm. Figure 4(a) shows the false-colored SEM image of the fabricated transistors. Figure 4(b) shows a typical atomic force microscopy (AFM) image of the high-quality Au-assisted mechanically exfoliated monolayer MoS_2 surface after removing the organic and Au layers. The fabricated transistors were heated according to the series heating process of as-fabricated (H_0), 200°C for 40 min (H_1), 125°C for 12 h (H_2), and 200°C for 7 h (H_3) in sequence, as shown in Figure 4(c). Next, the superimposed heating steps are illustrated. The transfer characteristic curves of the MoS_2 FETs with Bi/Sb/Au contact electrodes of $L_{\text{channel}} = 1$ μm after series heating are displayed in Figure 4(d). The threshold voltage of the MoS_2 FET has negligible changes, and the on-state currents also fluctuate within a small range. Both phenomena indicate that the temperature stability of the Bi/Sb/Au-contacted MoS_2 FET was improved compared with that of the Bi/Au-contacted MoS_2 FET. After H_1, the on-state current increases, which can be explained by the high-temperature removal of absorbed water vapor during the device manufacturing process through the heating process, which reduces interface scattering and improves contact quality. To clarify the improvement in stability, we performed statistical analysis and compared the on-state currents of four groups of MoS_2 FETs with different channel lengths after series heating. Figures 4(e) and (f) show the statistical results of the MoS_2 FETs with Bi/Sb/Au contact electrodes. There is no distinct degeneration in the aspect of on-state currents after heating at 200°C for 40 min and 125°C for 12 h with Lchannel ranging from 1 to 5 μm. Because of the limitations of exposure equipment, MoS_2 FETs with an L_{channel} of 500 nm are prone to heating degradation because the residual photoresist in the exposure area accelerates contact degradation.

In addition to temperature stability, the time stability of the proposed Bi/Sb/Au contact electrode was characterized, as shown in Figure 5. The transfer characteristics of the as-fabricated MoS_2 FETs are almost identical to those of the device tested two months later. There are two reasons for this: (1) the contact with good temperature stability experiences little change in performance after multiple tests; (2) the PMMA package prevents external water vapor from adsorbing in the channel region and leads to oxidation of the contact electrodes.

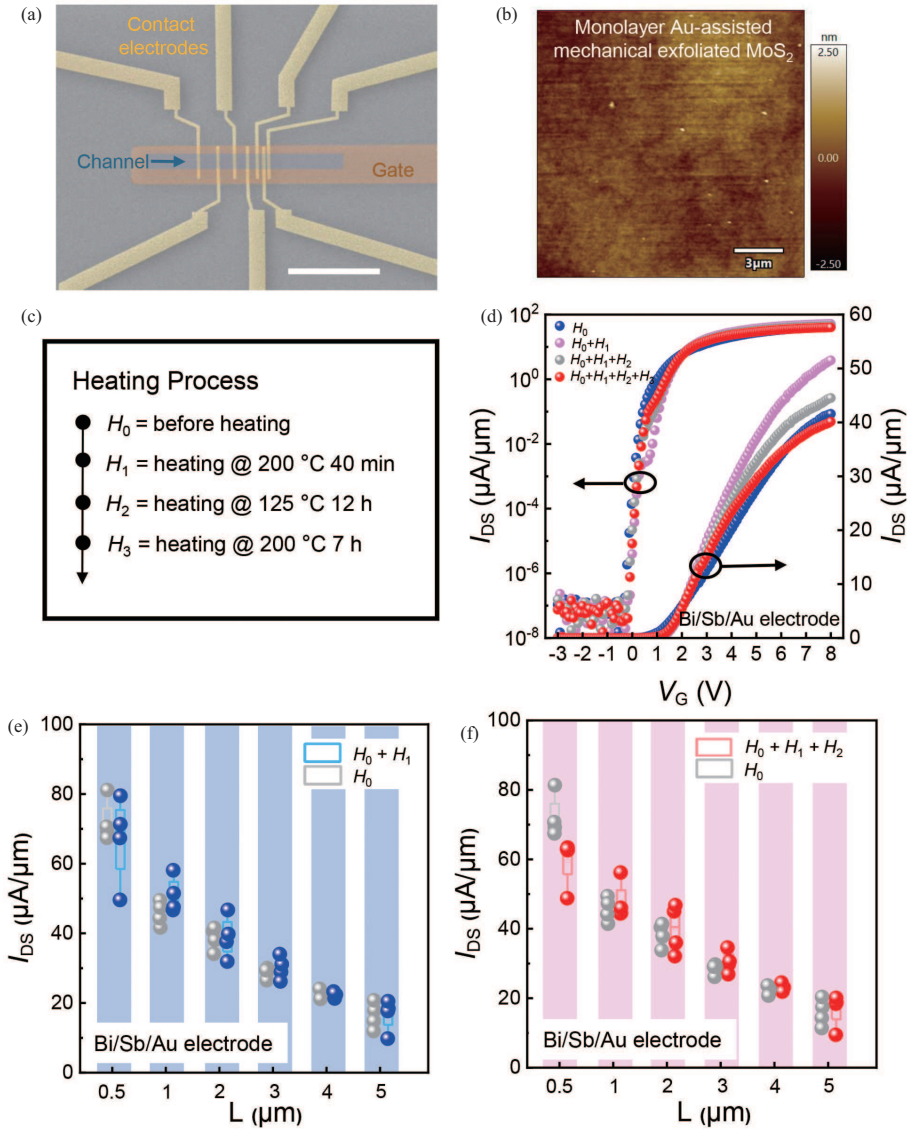

Figure 4 (Color online) (a) False-color SEM image of partially fabricated MoS_2 FETs with Bi/Sb/Au contact electrodes. The scale bar is 30 μm. (b) AFM topography shows the high quality of Au-assisted mechanically exfoliated monolayer MoS_2 after removing organic and Au layers. (c) The flow of the heating process was applied to the fabricated MoS_2 FETs with Bi/Sb/Au contact electrodes. (d) Transfer characteristics of a typical MoS_2 FET with Bi/Sb/Au contact electrodes with $L_{\text{channel}} = 1$ μm after different heating conditions. H_0, H_1, H_2, and H_3 correspond to the heating process in (c). The left axis is logarithmic, and the right axis is linear. (e) and (f) Boxplots comparison of the on-state currents of MoS_2 FETs with Bi/Sb/Au contact electrodes after different heating processes, including lower quartile (25%), median (50%), upper quartile (75%), and interquartile range (25%–75%). $L_{\text{width}} = 5$ μm for the fabricated transistors shown in (d), (e), and (f).

4 Conclusion

In conclusion, we presented a strategy for improving the temperature stability of potential semimetallic Bi contact by inserting semimetallic Sb on top of the Bi layer without additional complexity in device manufacturing. Through the surface SEM morphology and cross-sectional TEM characterization of the metal electrodes, we found that the temperature stability of the Bi/Sb/Au contact electrodes was significantly improved compared with that of the Bi/Au contact electrodes for higher surface continuity and Bi/Sb alloy contacting layer. The temperature stability of the Bi/Sb/Au-contacted MoS_2 FETs at 125°C and 200°C was verified through the nondegenerate transfer characteristics after heating. In addition, the fabricated device exhibits good time stability, benefiting from the Bi/Sb/Au contact electrodes and PMMA package. This study provides a new technical path for reliable semimetallic contact schemes

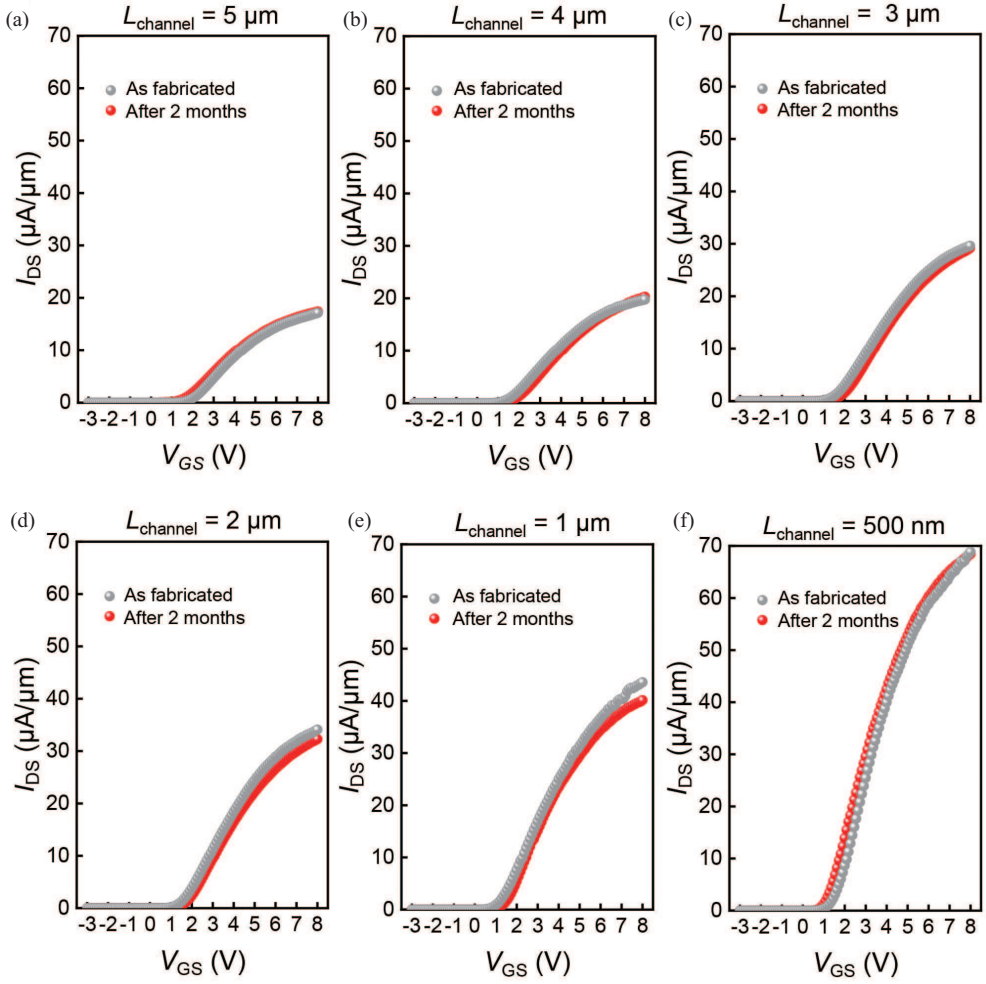

Figure 5 (Color online) Transfer characteristics of MoS_2 FETs with Bi/Sb/Au contact electrodes with different $L_{channel}$ as fabricated and after two months, including (a) $L_{channel}$ = 5 μm, (b) 4 μm, (c) 3 μm, (d) 2 μm, (e) 1 μm, and (f) 500 nm.

necessary for the practical application of 2D TMD FETs at the beyond silicon node [27,28].

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