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• REVIEW •
Special Topic: Silicon-Compatible 2D Materials Technologies

Progress on the program of Si-compatible two-dimensional semiconductor materials and devices

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Abstract Two-dimensional (2D) materials are at the forefront of innovation, heralding a new era for next-generation electronics and optoelectronics. These materials are distinguished by their unique structural characteristics: they have no hanging bonds on their surface, exhibit weakened electrostatic shielding in the Z-direction, and boast atomic thickness in their monolayers. These features have led to groundbreaking discoveries in electrical, optical, and magnetic properties, paving the way for advancements in low-power electronics, valleytronics, infrared detectors, and memory devices. Despite these promising developments, Si-based technologies continue to dominate the landscape of next-generation electronics and optoelectronics, as well as heterogeneous integration. In response to this ongoing evolution, the National Natural Science Foundation of China (NSFC) initiated a major program in 2021 dubbed "Si-compatible two-dimensional semiconductor materials and devices". This study reviews the progress made under the NSFC Program, spotlighting its main achievements and outlining key future research directions. Additionally, it sheds light on the challenges that researchers in the 2D domain face, particularly in developing Si-compatible 2D technologies.

Keywords two-dimensional materials, Si-based CMOS technologies, electronics and optoelectronics, heterogeneous integration, low-power

1 Introduction

Two-dimensional (2D) layered materials represent a fascinating class of materials characterized by their unique atomic structure. These materials are held together by strong covalent or ionic bonds within layers, while the bonds between layers are much weaker van der Waals forces. This unique configuration results in a 2D atomic structure with no dangling bongs on the surface, exhibiting weakened electrostatic shielding in the Z-direction and maintaining an atomic thickness in its monolayers [1]. Such a reduced dimensionality has unlocked new discoveries in electrical, optical, and magnetic properties, paving the way for innovative technologies, including low-power electronics, valleytronics, broadband responsive photodetectors, and neuromorphic devices [2].

In the midst of rapid advancements in broadband, big data, cloud computing, the Internet of Things, the Internet of Everything, artificial intelligence (AI), and other emerging information industries, there is a growing demand for enhanced signal processing, transmission, storage, and computing capabilities. Traditional device paradigms, such as graphics processing units and tensor processing units used in parallel computing processors, are increasingly constrained by limitations in heat dissipation and energy consumption, thereby posing new requirements for semiconductor integrated circuits (ICs). At present, as Si-based complementary metal oxide semiconductor (CMOS) transistors have shrunk to sub-10-nm scales, they face significant challenges, such as high power consumption and high costs. In addition, to mitigate short-channel effects, scaling rules require a reduction in channel thickness commensurate with gate length reduction to ensure sufficient electrostatic control. Despite these challenges, Si-based technologies are poised to remain the cornerstone for the development of next-generation electronics,

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optoelectronics, and heterogeneous integration. However, to overcome the inherent shortcomings of the Si material, 2D materials emerge as promising candidates. When integrated with Si CMOS, these 2D materials offer the potential to revolutionize future chip technologies. This integration could enhance not only computing and memory functions but also introduce sensing and brain-like intelligence functions [3].

In an effort to align with the nation's major strategic needs and push the boundaries of scientific exploration, the Information Science Division of the National Natural Science Foundation of China (NSFC) initiated a major program in 2021 entitled "Si-compatible two-dimensional semiconductor materials and devices (Si-2DMD)". This major program stands out among the various initiatives funded by the NSFC. The Si-2DMD program encompasses five key areas: controllable synthesis of 2D semiconductor materials and their modification, memory devices, logic devices, integrated devices with sensing-memory-computing functions, and the monolithic integration system of electronics and optoelectronics. The collaborative effort behind this program brings together researchers from prestigious institutions across China, including Zhejiang University, Fudan University, Xidian University, Peking University, and Hunan University. This collaboration stimulates a spirit of innovation, encouraging exploration and propelling the field toward new frontiers of knowledge and technological advancements. This article aims to review the main progress made by the Si-2DMD program, spotlighting its main achievements and key future research directions. Furthermore, it addresses the challenges faced in developing Si-compatible 2D technologies, both from the perspective of this program and the broader 2D material domain.

2 Synthesis and basic properties

For the development of optoelectronic devices, achieving wafer-scale spatial uniformity in 2D films is crucial. This uniformity ensures consistent optical and electronic properties essential for device and circuit operations while facilitating cost effectiveness. Si technologies have thrived owing in part to the easy production of the Si material, which boasts well-controlled crystalline structures, high purity, and tailored doping. However, in the field of 2D materials and devices, the controllable synthesis of 2D materials on various substrates, not limited to Si-based substrates, remains a significant challenge. This limitation hinders their practical electronic and optoelectronic applications despite their excellent performance exhibited by individual devices. Recent discussions have highlighted chemical vapor deposition (CVD) as one of the most promising methods for synthesizing 2D materials. One of its key advantages is that its growth temperature, normally no higher than 550°C or even 450°C for 2 h [4], fits within the back end of the line thermal budget [2]. Furthermore, the direct preparation of 2D layers on Si-CMOS is highly desirable. However, the film crystalline quality of 2D materials synthesized on silicon-based substrates such as Si and SiO_2/Si currently falls short of expectations. As a result, alternative crystalline substrates such as sapphire are considered for the synthesis of transition metal dichalcogenides (TMDs), especially for applications requiring high-mobility transport.

2.1 2D CrS_2 and its basic properties

Since the groundbreaking reports in 2017 [5, 6], the exploration of 2D materials for magnets has garnered significant interest owing to discoveries of magnetism at the atomic layer thickness. The effort to understand the intrinsic magnetic mechanisms within novel 2D layered materials has been extensively investigated by both theoretical and experimental studies, aiming to exploit these properties for spintronics and other applications [7].

In a landmark development in 2019, our team reported the successful synthesis of 2D layered CrS_2 materials. However, the initial synthesis on various substrates, including Si resulted in CrS_2 layers composed of mixed phases: 2H, 1T, and 1T′ phases [8]. Notably, these monolayer CrS_2 sheets exhibit markedly different electronic band structures depending on their phase. Specifically, the 2H phase of CrS_2 is a direct bandgap p-type semiconductor, while the 1T and 1T′ phases display metallic and semi-metallic characteristics, respectively. Furthermore, while 2H-CrS_2 is a nonmagnetic semiconductor, the 1T and 1T′ phases of CrS_2 exhibit magnetic behavior. Leveraging a Te-assisted CVD process, we synthesized 2D CrS_2 layers at 800°C, a technique that notably reduces the synthesis temperature. Through careful optimization of the synthesis parameters, we successfully obtained pure 1T-CrS_2 flakes on mica and SiO_2/Si substrates [9]. Our observations revealed oriented growth of CrS_2 domains on the mica surface (Figure 1). Inspired by the theoretical findings [8], we investigated the basic properties of the 1T-CrS_2 layer. Consistent with theoretical results, the field-effect transistor (FET) built using 1T-CrS_2 as the

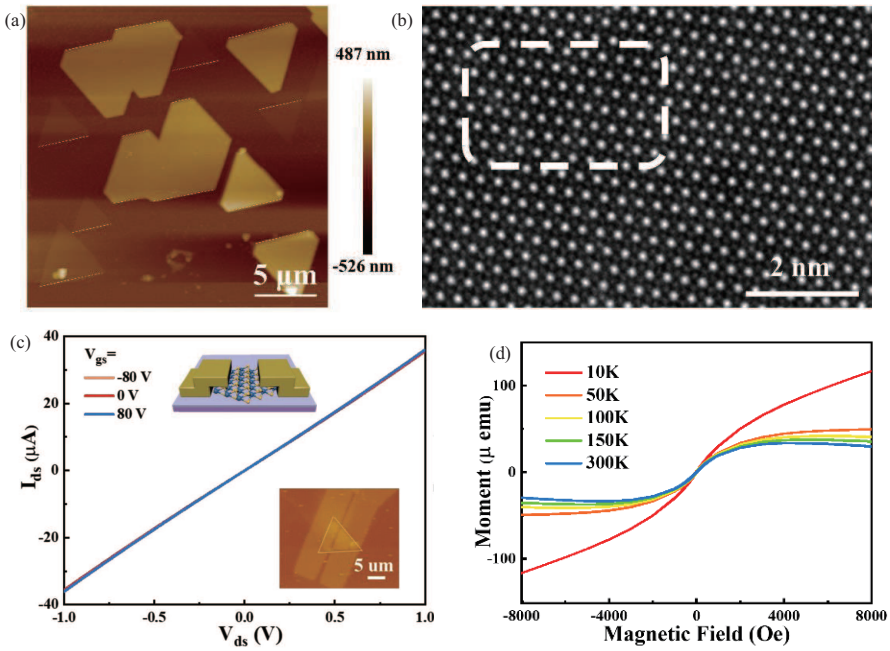


Figure 1 (Color online) (a) Atomic force microscopy (AFM) image of as-grown CrS_2 domains showing nearly identical orientation; (b) high-angle annular dark-field (HAADF) scanning transmission electron microscope (STEM) image of a CrS_2 crystal after transfer onto a Cu grid; (c) typical output characteristics of a CrS_2-based FET. The bottom-right and top-left insets show the schematic graph of a CrS_2-based FET on 300 nm-SiO_2/Si substrate and an AFM image of the fabricated device, respectively; (d) M-H curves measured at different temperatures for an as-grown CrS_2 sample [9]. Copyright 2022 Wiley-VCH GmbH.

channel material did not exhibit gate modulation behavior, indicating its metallic nature. Further investigations into the in-plane magnetic properties of the as-grown 1T-CrS_2 nanoflakes were conducted using a superconducting quantum interference device magnetometer across varying magnetic fields (M-H). The M-H measurements at 300 K revealed a hysteresis loop, signifying the room-temperature ferromagnetic behavior of the CrS_2 nanoflakes, with a coercivity of 28.7 Oe [9]. It is worth noting that the CrS_2 material is air-stable and although many 2D magnets have been reported, only a few, such as VS_2, MnS_2, and Fe_5GeTe_2, exhibit room-temperature magnetic orders [7, 10].

2.2 Wafer scale synthesis of 2D $PtSe_2$ film

Recent studies have highlighted the remarkable properties of 2D platinum diselenide ($PtSe_2$) crystals, which are known for their high carrier mobility. A particularly intriguing feature of this 2D material is its tunable bandgap, ranging approximately from 0 to 1.2 eV depending on the number of layers [11]. Furthermore, 2D $PtSe_2$ is very stable and environmentally friendly, and its low synthesis temperature is compatible with silicon-based technologies. These features position the material as a promising candidate for integration with Si-based technologies. The ability to adjust the electronic bandgap structures of $PtSe_2$ films by varying their thickness opens up possibilities for broadband photodetection across near-infrared (NIR) to mid-infrared (MIR) bands [12].

We exploited the thermally assisted conversion (TAC) technique to synthesize wafer-scale $PtSe_2$ films with different thicknesses. This process began with the deposition of a platinum (Pt) layer onto a SiO_2/Si substrate using a magnetron sputtering system. Following this, the Pt-deposited sample was loaded in the downstream side of a CVD furnace, while selenium (Se) powder was placed at the upstream side. The temperature for evaporating the Se powder was set at 222°C, and the Se vapor was then carried to the Pt/SiO_2/Si sample under a controlled Ar/H_2 flow. The selenization of the Pt layer occurred at a temperature of 400°C [13]. Using the TAC method allowed us to synthesize wafer-scale uniform polycrystalline $PtSe_2$ films with thicknesses of up to about 35 nm [14] thanks to the diffusion of Se into the pre-deposited Pt layer. We evaluated the uniformity of the $PtSe_2$ films, ranging from nanoscale analysis (using AFM) to device-level performance (in photodetector applications) [13], suggesting a high degree of homogeneity across the $PtSe_2$ substrates. As discussed later, the exceptional performance and reproducibility demonstrated by the fabricated 9 × 9 photodetector (PD) array further underscore the

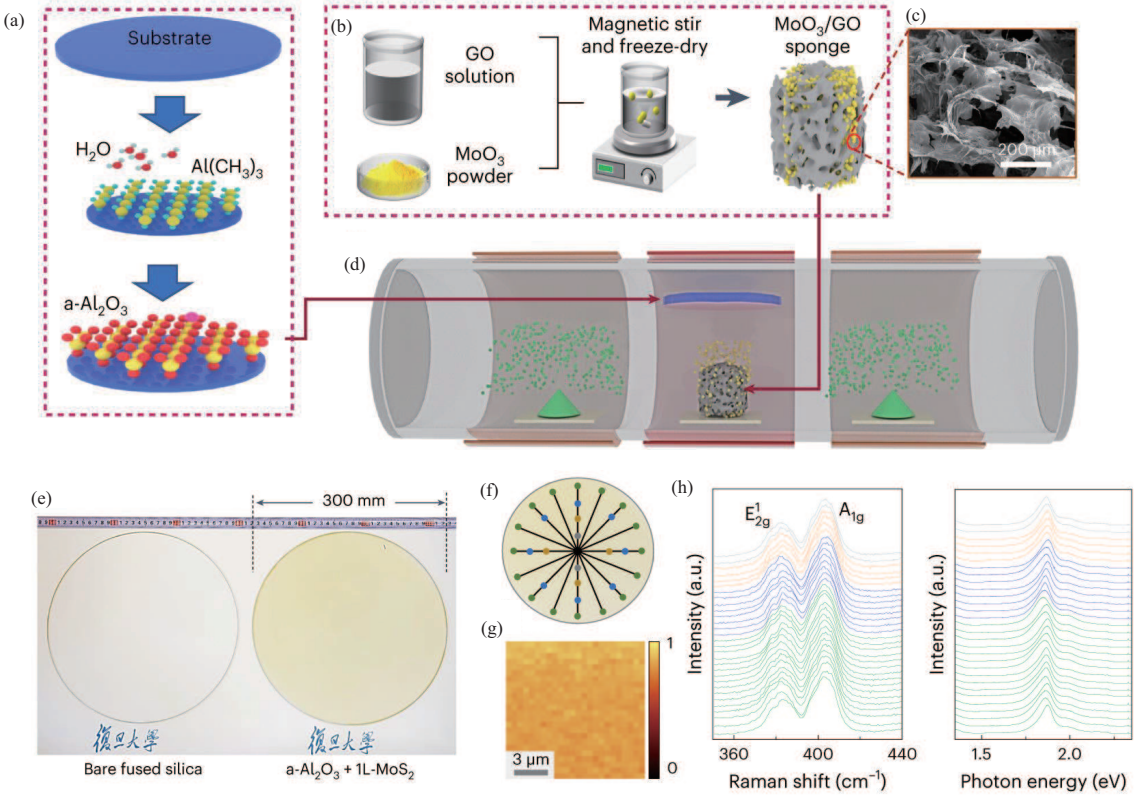


Figure 2 (Color online) (a) Schematic diagram of MoS_2 synthesis on an Al_2O_3 surface by ALD; (b) preparation of MoO_3/GO sponge precursors by magnetic stirring and freeze-drying; (c) SEM image of a MoO_3/GO sponge; (d) a schematic CVD system for MoS_2 synthesis; (e) photograph of a 12-inch wafer before and after the growth of MoS_2 monolayer; (f) uniformly scattered sampling spots over a 12-inch MoS_2 film for Raman and photoluminescence (PL) spectra measurements; (g) spatial intensity mapping of the A_{1g} Raman mode (406 cm^{-1}) acquired at the center spot. The color bar represents the Raman peak intensity (a.u.); (h) Raman and PL spectra acquired from 30 sampling spots [17]. Copyright 2023 Springer Nature.

readiness of 2D $PtSe_2$ films for the construction of high-performance $PtSe_2$/Si heterostructure PDs [13,14].

2.3 12-inch growth of uniform MoS_2 monolayer

To date, various strategies have been reported for synthesizing inch-scale 2D TMD films, especially molybdenum disulfide (MoS_2). These methods include substrate engineering [15] and careful precursor selection [16].

Zhou et al. [17] reported the controlled synthesis of a 12-inch polycrystalline MoS_2 monolayer, placing an emphasis on the balance between scale, cost and performance metrics to meet the requirements of electronic-grade IC manufacturing. First, to accurately control the release of metal precursors, they encapsulated MoO_3 by using a graphene oxide (GO) sponge as a reservoir. This was achieved by dispersing MoO_3 powder into a GO solution, thereby preparing a homogeneous MoO_3/GO mixture. To distribute sulfur vapor evenly, two containers filled with sulfur powder were symmetrically placed on either side of the MoO_3 source (Figure 2). Second, to optimize the crystalline structure of Al_2O_3 on substrates such as Si, the team treated the substrate with O_2 plasma prior to the Al_2O_3 deposition. The high-quality Al_2O_3 film was grown using trimethyl-aluminum (TMA) and H_2O as the aluminum and oxygen precursors, respectively, through atomic layer deposition (ALD). After the deposition, a 10-min thermal annealing at 120°C in a tube furnace under an O_2 atmosphere was implemented to further repair oxygen defects in the as-grown α-Al_2O_3, which resulted from the ambient atmosphere. It was found that the thickness of the α-Al_2O_3, ideally around 50 nm, significantly affected mobility. Furthermore, the Al_2O_3 layer served as an effective dielectric layer for FETs. The uniformity of the 12-inch MoS_2 was evaluated by Raman and FET property analyses. The evaluation of 37 top-gate FET arrays revealed an average mobility value of 40.65 $cm^2 \cdot V^{-1} \cdot s^{-1}$ in the range of approximately 12–70 $cm^2 \cdot V^{-1} \cdot s^{-1}$and an average I_{ON}/I_{OFF} value of 2.27×10^8, indicating relatively small device-to-device variations. The study also

found that the presence of grain boundaries did not significantly affect the performance of MoS_2 FETs with a long channel at room temperature.

2.4 Layer-controlled growth of TMDs and contact

To date, a significant portion of the research on 2D TMD FETs has focused on monolayer TMDs. This focus is primarily attributed to the challenges associated with achieving high-quality and uniform TMD layers with multiple layers [18]. A major issue encountered during device fabrication is the physical damage to the 2D monolayers caused by metal deposition, leading to substantial contact resistance (R_c). This issue is a critical bottleneck in device performance, particularly for short-channel devices. Furthermore, monolayer TMDs such as MoS_2 are known to have a relatively low density of states and are more susceptible to interface scattering, which can adversely affect device operation [19, 20]. On the other hand, multilayered TMDs, such as trilayer MoS_2, possess a higher density of states and improved mobility.

Wu et al. [21] successfully demonstrated the synthesis of trilayer MoS_2 crystals on soda-lime glass substrates, which enabled the creation of high-performance FETs with short-channel lengths. Unlike common synthesis methods that employ solid substrates such as SiO_2/Si and sapphire, the use of soda-lime glass, a liquid substrate, provided several advantages. These include uniform nucleation and lateral growth of the domains owing to the smooth and inert surface of the glass. Furthermore, the hydrophilic nature of glass facilitates the rapid transfer of grown 2D materials onto various substrates with minimal degradation. As a result of these factors, which contribute to fewer defects and negligible physical damage induced by metal deposition, the FETs constructed from 40-nm channel trilayer MoS_2 achieved remarkable performance. At a drain-source voltage $V_{ds} = 1$ V, the maximum drain current reached 589 $\mu A \cdot \mu m^{-1}$ at 300 K and 1162 $\mu A \cdot \mu m^{-1}$ at 4.3 K. Additionally, these FETs exhibited high saturation velocities of up to 4.2×10^6 $cm \cdot s^{-1}$ at room temperature and 6.7×10^6 $cm \cdot s^{-1}$ at 4.3 K, record-breaking values reported in the field.

Most 2H-TMDs exhibit n-type transport characteristics. 2D WSe_2 shows a bipolar transport feature. However, the device performance of 2D pFETs has not yet matched that of their n-type counterparts (nFETs), which currently stands as a significant hurdle in the realization of 2D CMOS logic circuits. Wu et al. [22] synthesized bilayer WSe_2 on SiO_2/Si substrates by using molten-salt-assisted low-pressure CVD at 890°C in an Ar/H_2 atmosphere. They investigated the scaling of the equivalent oxide thickness (EOT) with varying SiO_2 thickness, from 100 nm down to 6 nm, and also investigated a 2-nm-thick SiO_2/10-nm-thick HfLaO dielectric (EOT < 5 nm) by directly growing the bilayer WSe_2 on SiO_2 surfaces. This transfer-free mitigates the potential introduction of unfavorable doping and defects. The mobility of the bilayer WSe_2 pFETs remained consistent across different SiO_2 thicknesses, indicating that the substrate thickness had minimal impact on the growth of the bilayer WSe_2. The enhanced gate electrostatic control, achieved through reduced EOT, led to a drain-induced barrier lowering of approximately about 0.25 V/V on the 2-nm-thick SiO_2, marking the lowest value reported to date. The bilayer WSe_2 pFET, with a channel length of 120 nm, exhibited a record I_{ds} of 425 $\mu A/\mu m$ and G_m of 80 $\mu S/\mu m$ on the 6-nm SiO_2. The excellent device performance, partially attributed to the significantly low contact resistance of 650 $\Omega \cdot \mu m$ between the bilayer WSe_2 and the Pt metal, underscores the potential for fabricating high-performance WSe_2 pFETs on thinner EOT substrates without a transfer process, advancing the development of 2D CMOS devices.

The nature and quality of the 2D TMD/electrode contact is crucial to device performance. Achieving low contact resistance or Ohmic contact is vital to fully leverage the intrinsic transport properties of TMDs [23]. However, forming a low resistance contact remains a significant challenge owing to the easy formation of a tunnel barrier at a TMD/metallic contact interface, caused by the van der Waals (vdW) gap, which impedes carrier injection. Additionally, a finite Schottky barrier (SB) at the electrode-TMD interface reduces carrier injection efficiency [24]. Therefore, identifying suitable contacts capable of forming low-resistance connections is crucial. To avoid damage to 2D materials during metal contact deposition, a transfer method for metal electrode preparation has been developed [25]. Notably, most 1T-TMDs are metallic and thus can form better interfaces with 2H-TMDs. Pan et al. [26] used the CVD-grown MoO_2 flakes as contact buffer layers to fabricate MoS_2 FETs, achieving a carrier mobility of 33.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature and a low SB height of 36 meV. To establish ultra-clean metal contacts to 2D TMDs, Wang and Chhowalla [23] provided several valuable recommendations, including the use of high-quality TMD materials, avoiding highly reactive metals such as Ti, Cr, Ir, and Sc,

minimizing interface strain, and reducing the size of the vdW gap.

2.5 Ferroelectric (FE) materials for negative capacitance FETs

The relentless advancements of CMOS technology are increasingly challenged by issues related to power consumption and self-heating. These challenges have spurred researchers to explore scalable and energy-efficient architectures, such as tunnel FETs and ferroelectric negative-capacitance field-effect transistors (NCFETs) [27]. Unlike conventional MOSFETs, the structure of a Fe-NCFET incorporates a thin layer of ferroelectric material, marking a distinct functional departure from ferroelectric FETs [27]. Thus, the key to developing effective 2D Fe-NCFETs lies in identifying a reliable ferroelectric insulator capable of exhibiting negative capacitance. Recently, HfO_2-based ferroelectric films have emerged as promising candidates for negative-capacitance elements owing to their exceptional properties [28, 29].

Liu et al. [30] fabricated a ferroelectric capacitor using an HfO_2-ZrO_2 superlattice (SL). The superlattice-ferroelectric capacitor exhibited an endurance of 5×10^{12} cycles, a figure three orders of magnitude higher than that of traditional $HfZrO_x$ (HZO) [31], along with higher fatigue recovery capability. FETs incorporating amorphous ferroelectric-like dielectrics such as ZrO_2, Al_2O_3, and La_2O_3 have shown promising results, including higher endurance and lower operation voltage. The performance of these amorphous films depends on the accumulation and dispersion of mobile ions [32, 33], which play a crucial role in the manifestation of ferroelectric-like behaviors in the FETs [34]. Compared to the HfO_2-based ferroelectric films, the amorphous ferroelectric-like dielectrics of ZrO_2 and Al_2O_3 offer simpler fabrication processes, typically around 400°C for 2D ferroelectric NCFETs.

2.6 Growth of heterostructures and interlayer exciton properties

The innovative technique of vertically stacking 2D materials, each possessing distinct electronic, optical, and polarization characteristics, has paved the way for the creation of a large variety of vdW heterostructures [1, 35]. Unlike traditional bonded heterostructures, which are built using other dimensional materials, vdW heterostructures offer a flexible integration approach. This method allows for the combination of diverse materials without the constraint of lattice matching, thereby unlocking unprecedented opportunities to explore various material combinations and devices featuring multiple and customizable functions. Both top-down assembly and bottom-up synthesis are used to construct vdW heterostructures. The top-down assembly method, however, presents challenges in terms of consistency across samples, as the quality of stacks can significantly vary. This variability largely depends on the assembler's skill, rendering the top-down process nearly uncontrollable at present. Conversely, bottom-up methods require each material to be independently grown, often necessitating an appropriately catalytic underlayer.

Pan et al. [36] prepared vertical $GaSe/MoS_2$ p-n heterojunction on SiO_2/Si via liquid gallium (Ga)-assisted CVD method. The MoS_2 was synthesized on SiO_2/Si via a typical CVD process. To deposit GaSe onto the MoS_2, they utilized a ceramic boat filled with Ga_2Se_3 powder mixed with Ga. Their findings revealed that by adjusting the quantity of Fa, it was possible to precisely control the vertical and lateral growth modes of the material. Employing a similar two-step CVD growth technique, they also prepared $GaTe/MoS_2$ [37] and In_2Se_3/WSe_2 heterostructures [38]. This two-step approach, involving separate growth processes for the first and second layers, proves more suitable for the controllable synthesis of 2D heterostructures [39]. Crucially, the edges of the first layer, characterized by dangling bonds, serve as the preferred sites for the nucleation of the subsequent vapor reactants. The fabrication of high-quality vdW heterostructures hinges on the ability to form subsequent layers effectively, given that the growth of high-quality TMDs normally requires a catalytic surface.

The construction of vdW heterostructures through the stacking of two monolayer semiconductors, such as different TMDs, can introduce lattice mismatch or rotational misalignment. This often results in the formation of an in-plane moiré superlattice. Such moiré superlattices play a pivotal role in regulating the electronic band characteristics of vdW heterostructures, leading to unique electronic and optical phenomena. These phenomena include unusual superconductivity, interlayer exciton resonances, and distinctive patterns of light emission [40, 41]. For instance, Pan et al. [42] observed moiré intralayer excitons in a WSe_2/WSe_2 twisted homobilayer with a small twist angle by measuring the PL spectrum. Notably, they identified multiple split peaks within the energy range of 1.55–1.73 eV. The splitting differed significantly from the exciton peaks of monolayer WSe_2 and was attributed to the trapping of intralayer excitons by the moiré potential. Further investigation revealed that the depth of the moiré potential, and

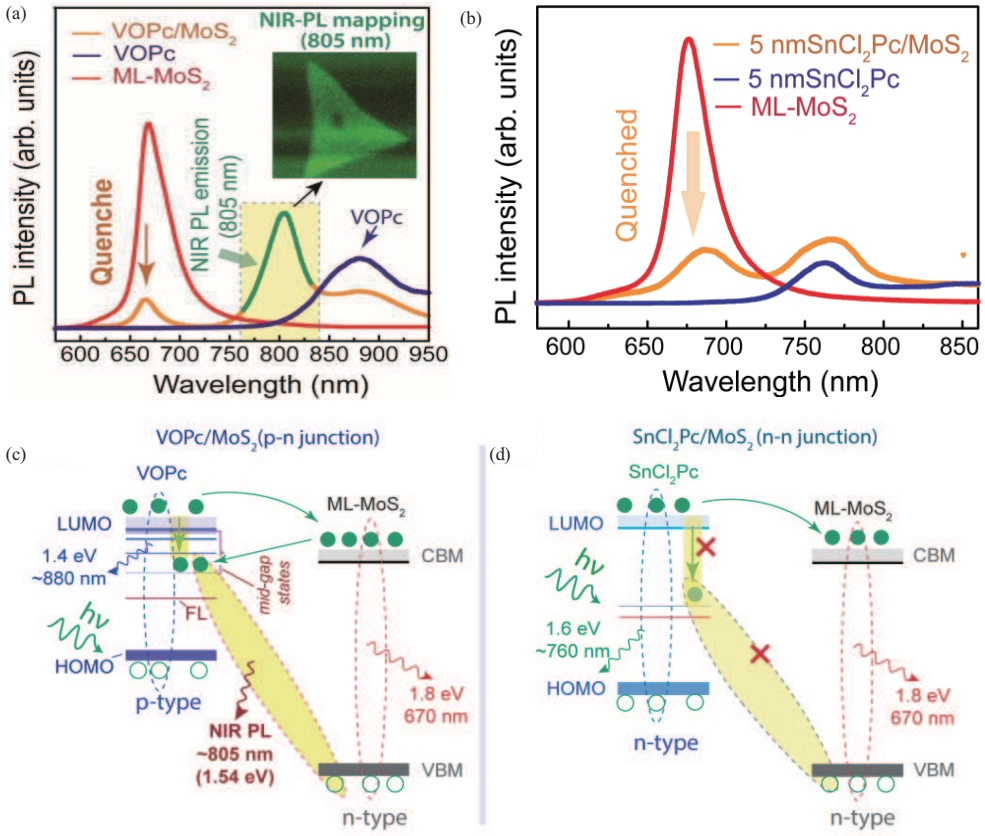


Figure 3 (Color online) (a) Typical PL spectra of the VOPc/MoS_2 heterostructure; the orange, blue, and red curves were measured from the VOPc/MoS_2, VOPc, and MoS_2 monolayers, respectively. PL quenching in the VOPc/MoS_2 heterostructure is indicated by a downward yellow arrow. A noticeable feature is the PL peak appearing around 805 nm (1.54 eV) as marked in the yellow-shaded box and shown in the inset PL mapping. (b) PL spectra of the $SnCl_2Pc/MoS_2$ heterostructure; the orange, blue, and red curves were measured from $SnCl_2Pc/MoS_2$, $SnCl_2Pc$, and ML MoS_2, respectively. PL quenching in the heterostructure is indicated by a downward bold arrow. (c), (d) Schematic representation of the energy band alignment of (c) VOPc/MoS_2 and (d) $SnCl_2Pc/MoS_2$ heterostructures. The shaded areas indicate the possible formation of interlayer excitons in the VOPc/MoS_2 heterostructure via mid-gap states, which is not possible for the $SnCl_2Pc/MoS_2$ heterostructure. The arrows illustrate the charge transfer processes that result in the formation of interlayer excitons [50]. Copyright 2022 Royal Society of Chemistry.

thus the behavior of these trapped excitons, was influenced by the interfacial coupling in the CVD-grown WSe_2/WSe_2twisted homobilayer [43].

Moreover, Pan et al. [44] explored the manipulation of interlayer excitons trapped at separate moiré locales within WS_2/WSe_2 heterobilayers. These moiré-locale excitons exhibited opposite circular polarizations, a characteristic traced back to their different local stacking registries, with an energy separation of around 60 meV. Two momentum-indirect moiré-locale excitons were observed as the measurement temperature increased. This suggests that the heterointerface, with its varying different phonon scattering properties, could influence the emission of these moiré-locale excitons. Furthermore, it was demonstrated that their emission energy could be fine-tuned by strain engineering.

Forming vdW heterojunctions by stacking individual TMD layers with precise control over the twist angle remains a major challenge. This precise arrangement is crucial to harnessing the pronounced effects that these structures can offer. Both monolayer TMDs and organic semiconductors exhibit larger exciton binding energies than those observed on conventional semiconductors. This results in well-defined dispersive exciton bands within the Brillouin zone, resulting in either the formation of moiré exciton minibands [45] or an ordered arrangement of energy traps [46]. These configurations significantly influence the propagation or confinement of excitons. Therefore, heterostructures consisting of 2D materials and organic semiconductors provide a novel platform for exploring fundamental physics and designing functional devices, leveraging the benefits of both 2D materials and organic semiconductors [47–49].

In our study, we identified a new emission peak at around 1.54 eV (~805 nm) within a heterostructure that combines pyramidal VOPc (p-type) and monolayer MoS_2 (VOPc/MoS_2), possibly originating from interlayer excitons (Figure 3) [50]. This observation contrasts with the PL quenching noted in the

$SnCl_2Pc/MoS_2$ heterostructure, despite both being type-II heterostructures. We tentatively attribute this emission to carrier transitions between the generated interface mid-gap states of VOPc, as predicted by density functional theory calculations and the ground state of MoS_2 in the heterostructure. The energy of this emission sits between the individual VOPc and MoS_2 bandgaps, which is strikingly different from previously reported interlayer exciton emissions that exhibited energy levels below the bandgaps of the constituent semiconductors [51]. The observation also diverges from the PL enhancement observed in the PTCDA/MoS_2 heterostructure [47, 48]. Although the origin of this new emission requires further investigation, these studies underscore the importance of not just the interface energy level alignment but also the intrinsic properties of the organic/TMD interface, in affecting charge transfer and transport mechanisms.

3 2D functional electronic devices

In this section, we concentrate on the Program's progress on 2D devices, with an emphasis on functions such as memory and computing. These are fundamental components for multifunctional devices.

3.1 Vertically stacked layer FETs

As silicon transistor technology continues to scale down, the quest for performance improvement in planar transistors is increasingly challenged by quantum confinement effects. To address this limitation and further boost the density of ICs, vertical stacking integration of complementary transistors is an effective approach. This technique, involving the stacking of p-n type FETs in a 3D integrated form, greatly reduces the IC footprint. Moreover, it allows for a significant reduction in the spacing between p-n transistors compared to planar devices. This reduction not only diminishes parasitic effects and interconnect overhead in ICs but also contributes to a decrease in power consumption. The vertical complementary FET (CFET) is viewed as a potential successor to the FinFET in the evolution of device structures. In a CFET, nFET and pFET are fabricated on top of each other, transitioning the p-n spacing from horizontal to vertical and unlocking considerable scaling potential. However, the realization of CFETs in Si-based devices requires rigorous integration process conditions, including high-temperature treatment processes, which pose significant challenges. To overcome the difficulties associated with fabricating vertical 3D fin-like FETs, aimed at enhancing gate-control capabilities and reducing power consumption, innovations such as the multibridge channel (MBC) structure and CFET (stacked nanosheets) are being introduced. These technologies, leveraging gate-all-around technology and aggressive cell height scaling, promise further gains in performance, power efficiency, and area utilization. The MBC FET, in particular, features nanosheet channels that are horizontally stacked and surrounded by a gate on all sides. This configuration significantly improves gate-control ability. Additionally, the design of MBC FETs offers flexibility in determining the width and vertical stack levels of nanosheet channels. Consequently, vertical stacking of multilevel nanosheet channels can significantly enhance the drive current per footprint.

Zhou et al. [52] reported a two-level-stacked MBC FET utilizing trilayer MoS_2 as the channel material (Figure 4). This innovative design achieved a high drive current of 23.11 μA per channel alongside a low leakage current of 55 fA per level, surpassing the performance metrics of the latest seven-level-stacked Si-based MBC FET. The fabricated MBC FET showed an on-off current ratio of 4×10^8 with a subthreshold swing (SS) value of 60 mV/dec at room temperature.

Building on the advancements in CVD-grown 2D material channels, Wu et al. [53] introduced a monolithic 3D stacking CFET aimed at developing low-power ICs. Their approach involved a post-metal annealing process at 200°C under an Ar atmosphere and the optimization of Ni/Pt/Au (1/10/30 nm) contacts. This methodology significantly enhanced the performance of the top-gate p-channel bilayer WSe_2 transistor, which featured a 12-nm HfO_2 dielectric layer. The device achieved a record-high I_{on} of around 594 μA/μm and G_m of around 244 μS/μm at V_d of −2 V with a channel length of 135 nm, setting a new benchmark in the field. Furthermore, the symmetry in threshold voltages between the WSe_2 pFETs and MoS_2 nFETs enabled the creation of full-output-swing inverters with rail-to-rail operations while consuming less than a nanowatt of power. Leveraging the CFET design, Wu et al. [53] successfully demonstrated for the first time the implementation of a 4T static random-access memory (SRAM) and 16T half-adder circuit units. Compared to traditional planar CMOS technology, these 3D ICs exhibited an approximate 8% performance improvement, a 6% reduction in dynamic power consumption, and a 44%

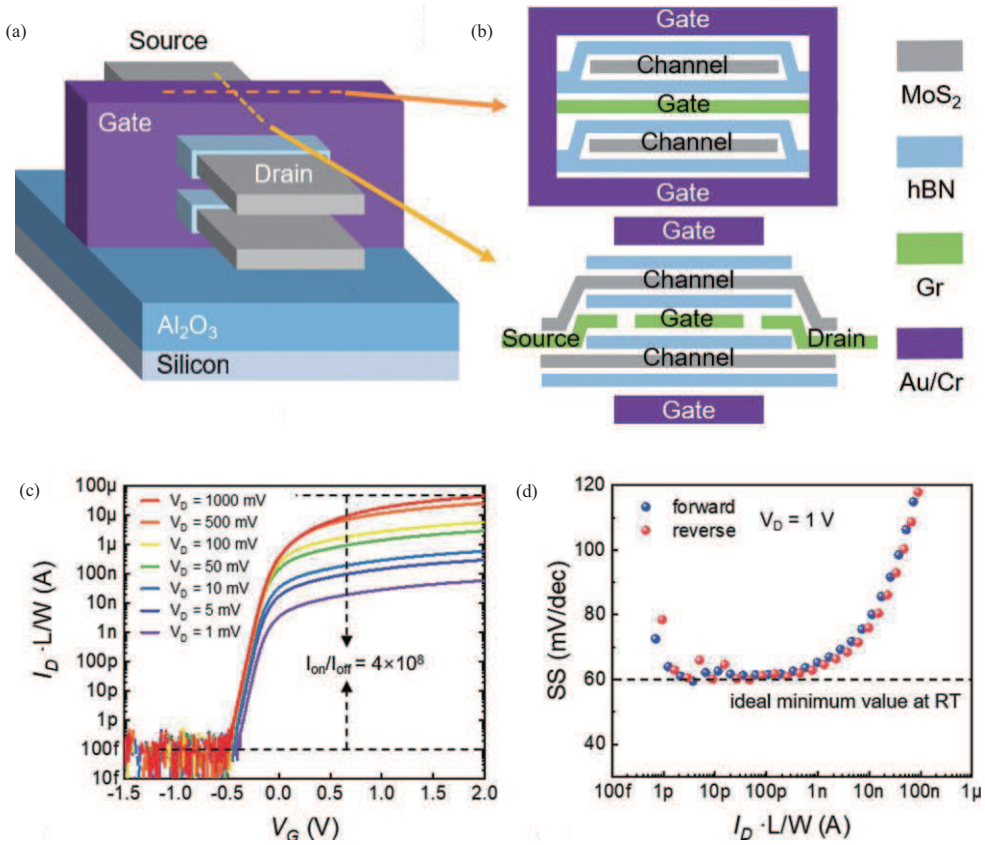


Figure 4 (Color online) (a) Schematic structure of a two-level-stacked channel MBC FET. The two channels cross the gate and connect together on the source and drain. (b) Schematic cross-sectional views along gate (upper inset) and source/drain (lower inset) directions. (c) Transfer characteristics of the MBC FET at the source-drain voltage from 1 to 1000 mV. The threshold voltages are identical and the on-off ratio can be 4×10^8. (d) SS data extracted from transfer characteristics at $V_D = 1$ V. There are three orders of magnitude as the I_D approaches the theoretical minimum at room temperature [52]. Copyright 2021 Wiley-VCH GmbH.

reduction in area. These results underscore the superior performance, power efficiency, and compactness offered by the CFET approach.

The two-surface-channel (TSC) working mechanism [54] introduces a novel approach whereby logic computing can be executed within a single dual-gated transistor. Utilizing the voltage-modulated barrier effect, Zhou et al. [55] successfully implemented a pixel processing unit by using only one TSC WSe_2 transistor. This innovation allows for the AND and XNOR logic functions within the pixel processing unit to be switched only by adjusting the drain voltage, which modulates the carrier injection barrier. This adjustment suggests that a single device can effectively serve as the core of a pixel processing unit. Through the integration of such pixel processing units, a low transistor-consumption image processing array (3×3) was realized. This array demonstrated its capability by performing both image intersection and image comparison tasks efficiently. Remarkably, the transistor consumption in this innovative image processing unit was less than 16% of that required by traditional circuits, despite offering comparable image processing power. Consequently, this low transistor-consumption scheme presents a potential solution to the issue of circuit redundancy often encountered in parallel computing systems.

3.2 In-memory computing

The quest for efficient data-intensive computation in the post-Moore era has led to the exploration of in-memory computing as a promising new paradigm. In modern computers, there is a physical separation between computing and memory components. This separation requires extensive communication between the two, resulting in increased power consumption and reduced efficiency, ca dilemma known as the von Neumann bottleneck. Overcoming this challenge requires innovative solutions, as the device architecture based on traditional Si-CMOS technology tends to be complex and demonstrates a large footprint. In

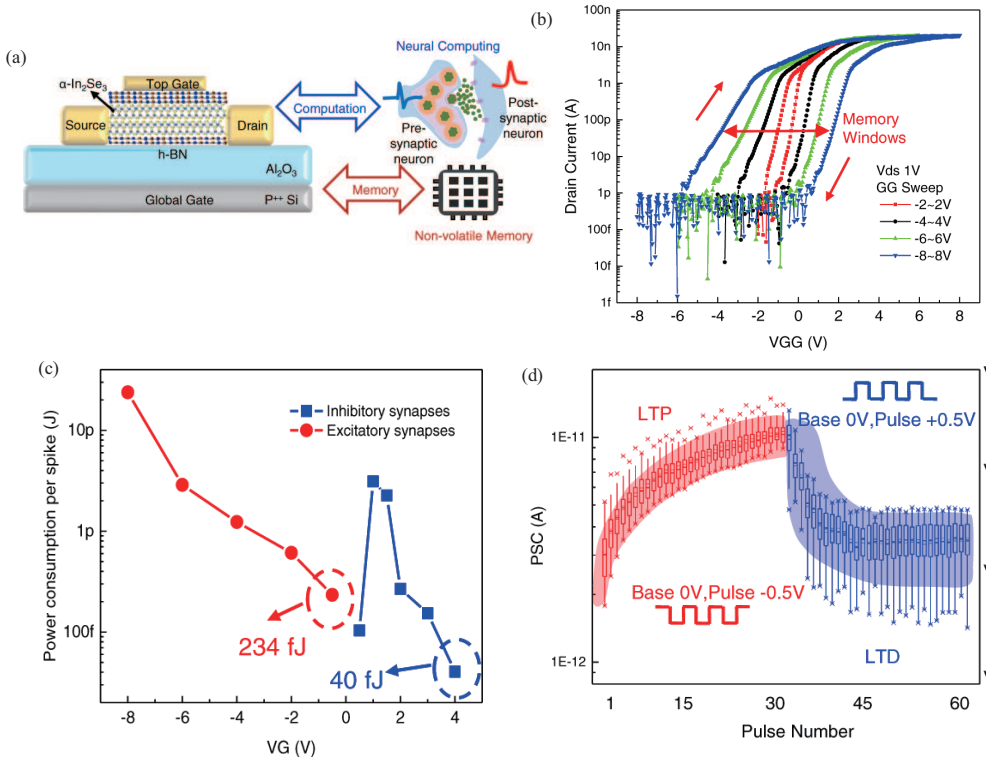


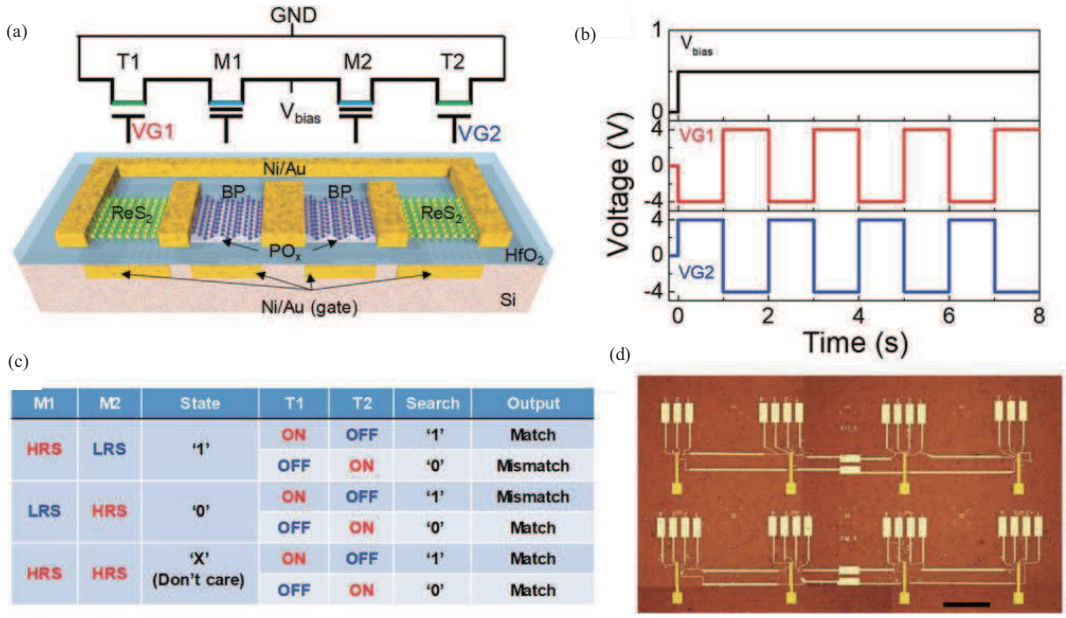
Figure 5 (Color online) (a) 2D FeCTs structure features memory and computing functions, with the channel layer composed of α-In_2Se_3 ferroelectrics. The global and top dielectric layers are Al_2O_3 and hBN, respectively. Nonvolatile memory operations are carried out by GG, and neural computing is implemented through the combined use of TG. (b) Transfer characteristics of 2D FeCTs NVM, demonstrating that the clockwise hysteresis windows expand with the increase in VGG, showing cumulative channel polarization. (c) Calculated single-event energy consumption of FeCTs in sumulating excitatory and inhibitory synapses under varying VG stimuli. 2D FeCTs exhibit ultra-low power consumption. (d) Progressive excitatory and inhibitory PSC modulation is achieved by using spike voltages ($\pm$0.5 V, 30 ms), corresponding to the LTP and LTD simulations [56]. Copyright 2021 Springer Nature.

this context, 2D vdW heterostructures have distinctive advantages that can be harnessed to construct versatile logic functions with simplified device structures.

Zhou et al. [56] exploited 2D ferroelectric semiconductor α-In_2Se_3 as the channel material in developing a compact and scalable device. This device not only serves as nonvolatile memory (NVM) but also supports neural computing functions (Figure 5). The In_2Se_3 ferroelectric channel transistors showed outstanding performance characteristics. These include improved endurance enabled by the internal electric field and the ability to flexibly adjust neural plasticity. Furthermore, the device boasts remarkable operational metrics: a write speed of 40 ns, energy consumption rates of 234/40 fJ per event for excitation/inhibition, and 94.74% accuracy in simulated iris recognition classification tasks.

Leveraging the charge-trapping mechanism between a black phosphorus (BP) channel and a phosphorus oxide (PO_x) layer, a high voltage gain was realized in a nonvolatile CMOS logic circuit incorporating BP and rhenium disulfide (ReS_2) (Figure 6) [57]. This innovative approach enables the realization of a Schmidt-like flip-flop function by using only two transistors, a significant reduction from the six transistors required by conventional S-based circuits. Furthermore, Wu et al. [57] demonstrated parallel data search by using only four-transistor (4T) nonvolatile ternary content-addressable memory (nvTCAM) cells, which exhibited high resistance ratios of 10^3 between the match and mismatch states alongside the advantage of zero standby power, thanks to the nonvolatility of the BP transistors.

In a different vein, Zhou et al. [58] have explored the potential of a compact architecture using two MoS_2 FETs and one metal-insulator-metal capacitor in a 2_transistors-1_capacitor (2T-1C) configuration. This design is tailored for multiply-accumulate (MAC) operations, which are fundamental to AI computations. The 1T-1C portion of the architecture acted as a dynamic random-access memory cell, capable of storing a voltage with 8-level (3 bits) quantization for more than 10 s, thereby facilitating additional complex operations. The stored voltage is then applied to the gate of the second MoS_2 transistor, enabling an



M1	M2	State	T1	T2	Search	Output
HRS	LRS	'1'	ON	OFF	'1'	Match
			OFF	ON	'0'	Mismatch
LRS	HRS	'0'	ON	OFF	'1'	Mismatch
			OFF	ON	'0'	Match
HRS	HRS	'X' (Don't care)	ON	OFF	'1'	Match
			OFF	ON	'0'	Match

Figure 6 (Color online) (a) Schematic diagrams of TCAM cell based on BP/ReS_2 and its equivalent circuit. (b) Measurement set-up of the 4T-nvTCAM cell. The opposite gate voltage is applied to the 2 ReS_2 FETs (V_{G1} and V_{G2}) to implement search operations. (c) States of the four transistors in the 4T-nvTCAM cell for ternary storage and search operations. The two BP FETs (M1 and M2) and the two ReS_2 FETs are used for ternary storage and for data search, respectively. The output is always matched as the state is bit "X". (d) Optical picture of the TCAM devices connecting with 2 ReS_2 FETs and 2 BP FETs. The scale bar is 500 μm [57]. Copyright 2022 Wiley-VCH GmbH.

analog multiplication operation through the modulation of the drain current I_d. In addition, the current in multiple 2T-1C rows was converged to perform additional operations.

In a sophisticated demonstration of vdW heterostructure engineering, Pan et al. [59] introduced a partial floating-gate FET (PFGFET) based on the heterostructures consisting of graphene, h-BN and WSe_2. The PFGFET could operate in an FET mode or an NVM mode via independent control of the charge polarity of the WSe_2 channel by a control gate (CG) and a top gate (TG). When operating as an FET, the device showcased remarkable electrical properties, including the ability to switch between p- and n-type conductive modes, a steep SS of 64 mV/dec, and a high on/off current ratio of about 10^8. While working as an NVM, the PFGFET was varied between p- and n-type memory, achieving a high erase/program ratio of about 10^8 and a retention time exceeding 10^5 s. Building on these devices, the team successfully developed nonvolatile CMOS circuits showcasing a gain of 197 and noise margins of 0.44 and 0.47 V at V_{DD} of 1 V, as well as linear logic gates with integrated storage capabilities. Furthermore, nonlinear (XNOR and XOR) logic gates and a half-adder were demonstrated by using WSe_2- and MoS_2-based PFGFETs.

Liu et al. [60] explored the potential of double-ferroelectric-coupling effects and the reconfigurable polarity of the 2D TMD channels. They crafted a unique double-gate 2D FeFET aimed at facilitating in-memory computing across both digital and analog spaces. Unlike the single-gate 2D FeFET, this device concept with the dual-ferroelectric gates could carry out multiple functional operations, such as nonvolatile logic gates and synaptic transistors. By utilizing independent polarizations of the top and bottom ferroelectric layers (specifically P(VDF-TrFE)) acting as two logic inputs, the dual-gate 2D FeFETs accomplished two-input Boolean logic-in-memory operations. The linear (AND, OR) and nonlinear (XNOR) logic functions were realized in the unipolar MoS_2 and ambipolar $MoTe_2$ dual-gate FeFETs, respectively. By integrating MoS_2 and $MoTe_2$ FeFETs, the researchers successfully fabricated a crucial computational circuit, a half-adder, using an area-efficient two-transistor structure. Furthermore, using the same device structure as a conventional three-terminal FeFET, the single-gate memristive operations emulating the synaptic plasticity were demonstrated in the double-gate 2D FeFETs by fixing the polarization state in one of the ferroelectric layers.

These studies highlight the significant potential of 2D materials and their vdW heterostructures in the development of low-power, high-area-efficient, and multifunctional in-memory computing hardware, opening up avenues for both digital and analog computations.

4 2D functional optoelectronic devices

In this section, we review the Program's progress on 2D devices with an emphasis on their applications in lighting and sensing.

Unlike graphene, which is characterized by its zero bandgap, 2H-TMDs feature a bandgap in the NIR to the visible region. At the monolayer limit, these materials possess direct bandgaps, making them highly suitable for use in photonics and optoelectronics applications. 2D semiconductive TMDs have two distinctive aspects [61]. The first is the presence of strong excitonic effects, which arise from the inherently 2D nature of these materials and the consequent reduction in dielectric screening of Coulomb interactions among charge carriers. This significantly influences the strength of light-matter interactions, the radiative recombination lifetime of electron-hole (e-h) pairs, and the optoelectronic response of the materials. The strong excitonic effects also pave the way for the development of excitonic devices capable of operating at room temperature. The second feature is their valley- and spin-dependent properties. These stem from the unique electronic band structure of 2D materials, leading to valley- and spin-dependent optical and electrical characteristics. Such attributes hold considerable promise for future information technologies.

4.1 Lighting

Light sources are fundamental and indispensable elements in photonic ICs and other applications. The quantum confinement effects and direct bandgap feature of monolayer 2H phase TMDs, together with diversified heterostructures, facilitate the engineering of bright excitonic emission across a wide optical spectral region.

Pan et al. [62] reported a room-temperature waveguide-integrated light-emitting heterojunction diode. This diode comprises a p-type monolayer WSe_2 and n-type cadmium sulfide (CdS) nanoribbon (NR) on a SiO_2/Si substrate. In this configuration, the WSe_2 serves as the emitter, while the CdS NR, which has a transparency window in the red spectral range, functions as a low-loss dielectric waveguide. This design effectively guides both PL and electroluminescence (EL) emission along its longitudinal axis. By controlling the CdS NR waveguides, the EL from WSe_2 is efficiently coupled and directed, showcasing potential for optical interconnection. The hybrid LED demonstrates clear rectification under forward bias, generating intense EL at 1.65 eV from the exciton resonances in monolayer WSe_2, in which carrier injection is facilitated via intervalley scattering. Additionally, fluorescence blinking behavior was observed in monolayer MoS_2 within a heterostructure consisting of CdSe/ZnS core-shell quantum dots (QDs) and MoS_2 atomic layers, potentially attributed to an energy transfer from the QDs to MoS_2 [63].

The emission characteristics of TMDs are often influenced by defects, impurities, and other factors, such as plasmonic effects. For instance, it has been revealed that the PL enhancement in monolayer WS_2 arose from the oxygen adsorption-induced p-doping. Thus, it is possible to tune the PL brightening rate by adjusting the oxygen dopant concentration and temperature [64–66]. Furthermore, by combining a few-layer InSe with an Ag nanoprism array, the optical response of the 2D InSe layer in linear and nonlinear regimes was enhanced [67]. The improved response was attributed to the local surface plasmon resonance from the Ag nanoprism, which intensifies the coupling of InSe with incident light. Additionally, the distinct bending structure increases the out-of-plane polarization component of the incident light, leading to improved light absorption and scattering by the out-of-plane excitons at the InSe band edge.

4.2 2D/3D heterostructure photodetectors

2D materials exhibit strong light-matter interactions and can be seamlessly integrated with 3D semiconductors such as Si and Ge, making them compatible with the current CMOS production lines. Furthermore, the bandgap of 2H-TMDs can be easily adjusted by varying the number of layers and applying strain. PDs, devices that convert optical signals of various incident wavelengths into electrical signals, are crucial in both military and civilian applications, including environmental monitoring, medical diagnosis, and optical communication. Commercial PDs are made of different 3D semiconductor materials such as GaN, SiC, Si, Ge, HgCdTe, InSb, and InGaAs. These materials are often chosen for their specific response to different spectral wavelengths, a characteristic determined by their unique bandgaps. However, these devices normally suffer from complex manufacturing processes, high costs, environmental toxicity, and/or tough operation conditions. By contrast, 2D materials offer several advantages, such as tunable bandgap and excellent photoelectric properties, paving the way for the development of novel broadband PDs. Additionally, PDs based on 2D materials are emerging as promising solutions for machine vision.

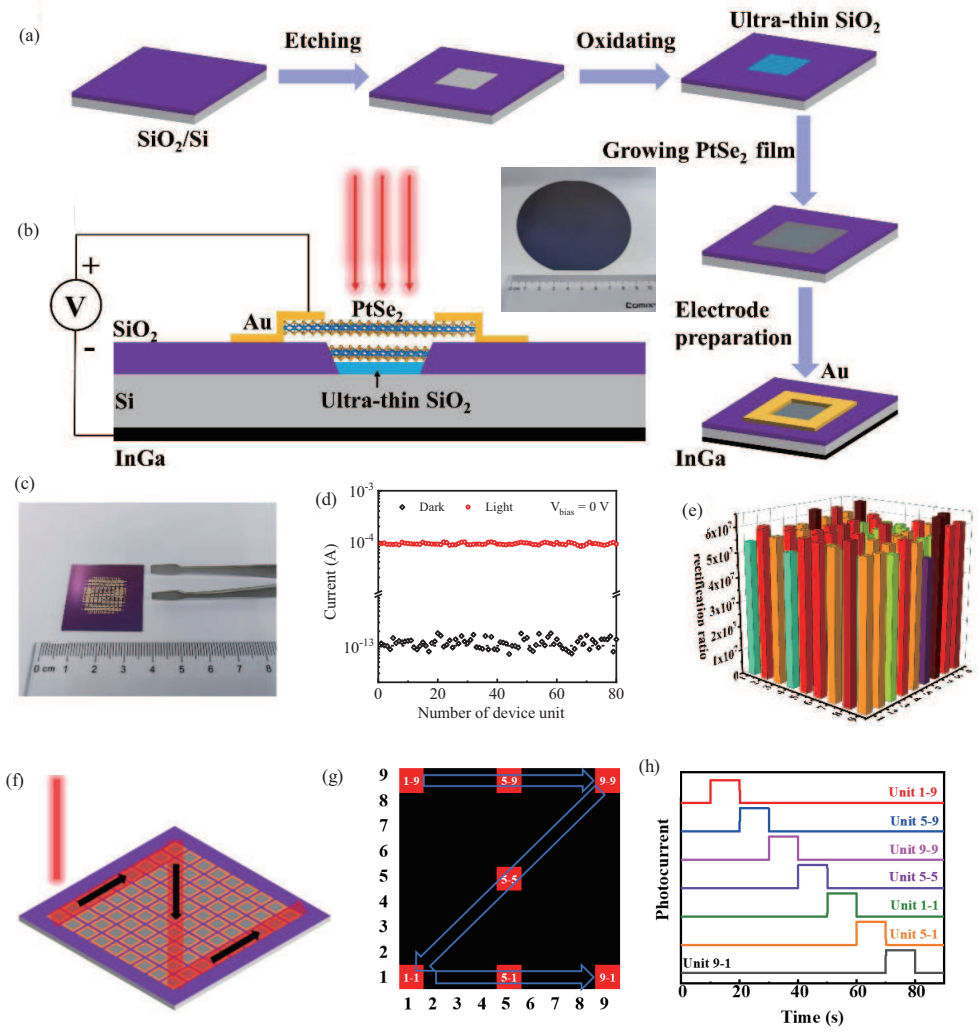


Figure 7 (Color online) (a) Fabrication flow of wafer-scale uniform 2D $PtSe_2$ film on SiO_2/Si; (b) schematic diagram of the cross-sectional view of the device; (c) optical picture of prepared array consisting of 9 × 9 devices based on the $PtSe_2$/ultrathin SiO_2/Si heterostructure; (d) currents of the 9 × 9 devices in the array in darkness and under 808 nm illumination. The dashed black and red lines denote the average values for the dark current and photocurrent, respectively; (e) 3D diagram of the rectification ratio for each device in the array within ±5 V; (f) and (g) schematic setup illustration for NIR 808 nm light tracing and (h) the corresponding currents [13]. Copyright 2023 Science China Press.

Utilizing our wafer-scale uniform 2D $PtSe_2$ films, we reported high-performance heterostructure PDs by combining with Si [13, 14, 68] and Ge [69]. These heterostructure PDs, characterized by their simple fabrication process, demonstrate superior performance across key parameters, with the notable exception of response speed, when compared to their commercial counterparts.

We designed a heterostructure comprising a $PtSe_2$ layer atop an ultrathin SiO_2/Si structure. This structure effectively utilizes the photogenerated carriers from both the Si substrate and the 2D $PtSe_2$ films (Figure 7) [13]. By integrating an ultrathin SiO_2 as the dielectric layer, we not only increased the barrier height at the $PtSe_2$-Si interface but also achieved passivation of the Si surface without hindering the bipolar carrier transport. The device demonstrated a dark current (I_{dark}) at zero bias of 0.12 pA, a rectification ratio within ±5 V of 5.7 × 10^7, and an ideality factor (n) of 1.015. Upon exposure to 808-nm NIR illumination at zero bias, the heterostructure PD exhibited an I_{light}/I_{dark} ratio of around 1.29 × 10^9, a responsivity (R) of 8.06 A·W^{-1}, a specific detectivity (D^*) of 4.78 × 10^{13} Jones, and a response speed of 14.1/15.4 μs. The PD showed impressive performance under different illumination wavelengths, with D^* values exceeding 3.85 × 10^9 Jones and responsivities of 2.12 A·W^{-1} (UV, 375 nm), 5.56 A·W^{-1} under visible (Vis, 532 nm), and 0.65 mA·W^{-1} under and NIR (1550 nm) illumination. We demonstrated the potential for UV-Vis-NIR illumination imaging and tracing applications by fabricating a 9 × 9 device array. The devices in the array demonstrated high homogeneity and reproducibility,

affirming their compatibility with Si-CMOS technologies. Characteristics such as unprecedented high performance, air stability, self-driven operation, and broadband response at room temperature make the $PtSe_2$/ultrathin SiO_2/Si heterojunction PDs stand out. Furthermore, our experiments revealed that a thicker $PtSe_2$ layer (35 nm) led to enhanced device performance compared to thinner layers (10 and 20 nm) [14]. Furthermore, we discovered that the photoresponse can be modulated by applying a gate bias [68].

We observed that PDs based on the combination of $PtSe_2$ and Si respond poorly to the 1550-nm illumination, which is attributed to the weak absorbance of both materials in this spectral band, the thin $PtSe_2$, with its bandgap of 0.4 eV, and Si, which as a larger inherent bandgap of about 1.12 eV. The latter corresponds to an absorption cut-off at wavelengths around 1100 nm, making it challenging to achieve excellent photoresponse characteristics to the infrared light spectrum. Therefore, we turned our attention to Ge for the development of $PtSe_2$/ultrathin Al_2O_3/Ge PDs [69]. The introduction of an ultrathin Al_2O_3 layer serves a dual purpose: it passivates the surface of Ge, reducing surface defect states, and it creates a barrier that prevents any reaction between Ge and Se. The resulting PD, measuring 50 μm × 50 μm, a responsivity of 4.09 $A{\cdot}W^{-1}$, a specific detectivity of 1.42×10^9 Jones, and a response speed of 32.6/18.9 μs under 1550 nm illumination (0.31 $mW{\cdot}cm^{-2}$) at zero bias. It was also found that the device size affected the response speed. The PD demonstrated a broad band response; R and D^* values of 0.31 $A{\cdot}W^{-1}$ and 3.23×10^8 Jones, 1.36 $A{\cdot}W^{-1}$ and 1.43×10^9 Jones, 1.80 $A{\cdot}W^{-1}$ and 1.90×10^9 Jones, were achieved by the $PtSe_2/Al_2O_3$/Ge photodetector for 375, 532, and 940 nm illumination, respectively. Notably, the device exhibited superior photosensitive characteristics in response to NIR light, largely owing to the inherent absorption properties of Ge.

Charge-coupled devices (CCDs) are renowned for their high-quality and low-noise imaging capabilities. They are highly sensitive to even weak light conditions, providing better image quality with lower noise as compared to CMOS image sensors. However, their performance has been limited by high operation power requirements, slow response times, and limited charge integration capabilities. We have recently introduced an electric-dipole-gated phototransistor. This novel device, which can operate without external gate bias, leverages a high-k HfO_2 dielectric material to replace conventional SiO_2 in graphene and Si-based devices [70]. By employing a thin, 10-nm layer of HfO_2 layer, we have successfully facilitated electrostatic coupling between charges photogenerated in the Si and the graphene channel. The device exhibited outstanding performance in the broadband spectrum, ranging from 266 to 1342 nm at very low drain bias voltage (∼0.5 V) without gate bias. The device has a high responsivity of 3.7×10^3 $A{\cdot}W^{-1}$, external quantum efficiency of 0.72×10^4, and detectivity of 6.20×10^{13} $cm{\cdot}Hz^{\frac{1}{2}}{\cdot}W^{-1}$at an 800-nm wavelength and 3.3×10^3 $A{\cdot}W^{-1}$, 1.31×10^4, and 5.61×10^{13} $cm{\cdot}Hz^{\frac{1}{2}}{\cdot}W^{-1}$at a 400-nm wavelength. The underlying mechanism of our two-terminal phototransistor, which operates without a gate electrode, relies on the integral combination of photovoltaic effects, high-k dielectric properties, and Dirac materials. This discovery has the potential to eliminate the need for a gate terminal from commercial CCD devices.

4.3 Spike-based neuromorphic sensing

Drawing inspiration from the brain's hierarchical organization and neuro-synaptic architecture, neuromorphic computing offers a promising solution to the von Neumann bottleneck in circuit design thanks to its capacity for highly parallel computation and minimal energy dissipation. Central to this approach are synaptic devices, which play a critical role in artificial neural networks by emulating the behavior of biological synapses through the manipulation of synaptic weights. Optoelectronic synaptic devices, combining light-sensing capabilities with synaptic plasticity, have shown potential for energy-efficient visual processing. While synapses based on conventional CMOS circuits are compatible with existing fabrication processes, they typically require many transistors with complex interconnections and high energy consumption to emulate a single synapse. Thanks to their flexible energy band design, unique optoelectronic properties, and ultrathin body, 2D materials and their vdW heterostructures have recently garnered significant attention. Their attributes make them highly suitable for mimicking synaptic plasticity, offering a potential pathway for advancements in neuromorphic computing [71,72]. Under electric and/or optical stimuli, various device architectures have been demonstrated to emulate biological synaptic functions.

Liu et al. [73] developed a floating-gate optoelectronic transistor. This device, sitting atop a SiO_2/Si substrate (Figure 8), comprises vdW heterostructures of mechanically exfoliated MoS_2, hBN, and graphene. In this configuration, the MoS_2 acts as the semiconductor channel, hBN serves as the tunnel barrier, graphene functions as the floating gate, SiO_2 acts as the gate dielectric, and Si acts as the CG. The opto-

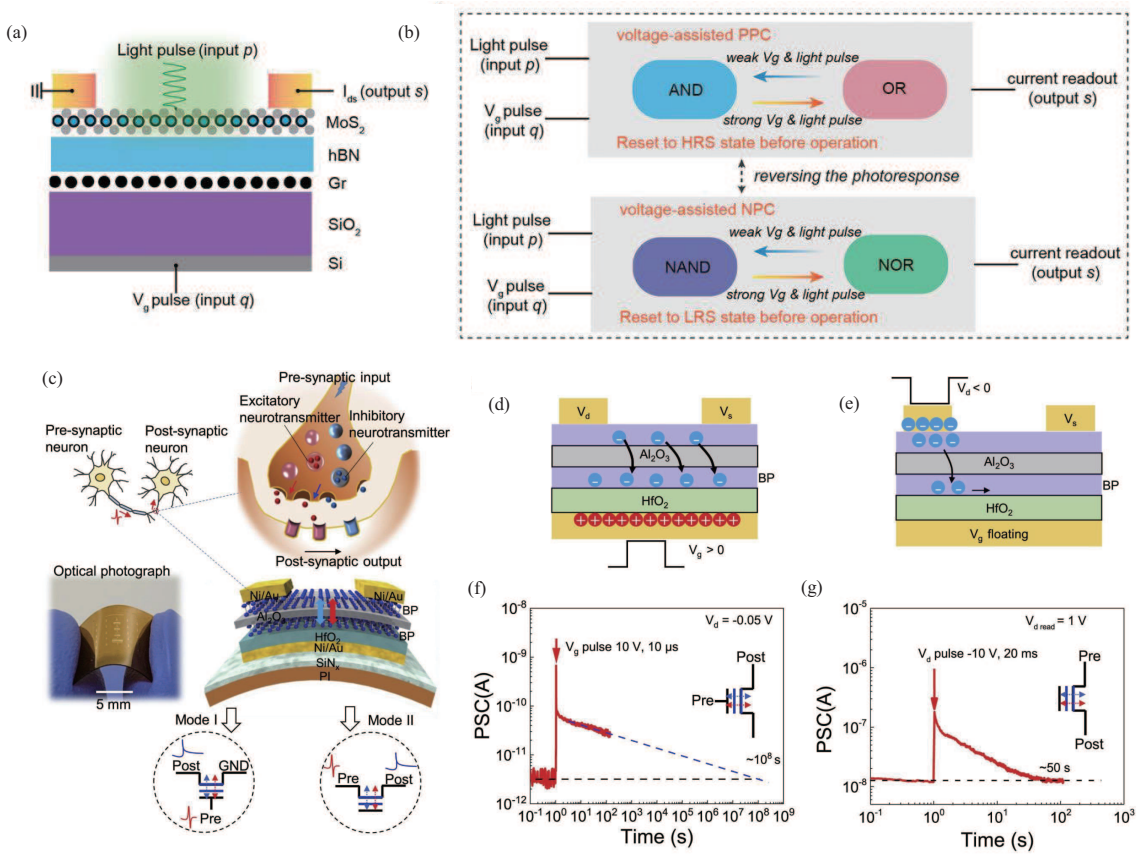


Figure 8 (Color online) (a) Schematic diagram of a logic gate. The logic inputs (p, q) are controlled by light and gate voltage pulses, and the logic output (s) is the drain-source current; (b) operation demonstration of the reconfigurable nonvolatile optoelectronic logic gates [73]. Copyright 2022 Wiley-VCH GmbH. (c) Conceptual illustration of BP-based floating-gate synaptic devices on a flexible polyimide (PI) substrate, serving as synapses between neurons with two working modes; diagram showing the operating mode for the three-terminal synapses (d) and the two-terminal synapses (e); excitatory postsynaptic current triggered by one presynaptic spike by V_g (f) and V_d (g) versus time, showcasing long-term and quasi-long-term memory effects [74]. Copyright 2022 Elsevier B.V.

electronic transistor can simultaneously sense, memorize, and process optical information. By leveraging the physical attributes of the 2D materials and vdW heterostructure, the devices implement both reconfigurable Boolean logic operations ("AND", "OR", "NAND", and "NOR") and synaptic functions within a logic-in-sensor unit. The device exhibits optically triggered volatile and nonvolatile types of conductance switching, showcasing typical memristive characteristics that can be controlled by the strength and width of light pulses. The ability to switch between conductance states aligns with biological phenomena of short- and long-term plasticity, effectively emulating memorization and learning processes. The conductance state of the device, representing the level of memorization, is tailored by the light pulsing frequency.

Wu et al. [74] developed an innovative approach to synaptic devices by employing a floating-gate structure in BP transistors. Utilizing a mechanically exfoliated BP film as a charge-trapping layer, these devices were fabricated on a flexible polyimide (PI) substrate with pre-patterned local gates, showcasing dual-mode operation (Figure 8). The local gate, composed of 20/50 nm Ni/Au, was patterned onto the Si_3N_4/PI. A blocking oxide of HfO_2, measuring 20 nm in thickness, was situated between the local gate and the BP layer, while a 7-nm Al_2O_3 served as the charge tunneling layer. Atop this, another BP film was transferred to function as the channel layer. This configuration resulted in a significant current hysteresis, a critical feature for synaptic operation, attributed to the charge-trapping capacity of the BP floating gate. In contrast to the abrupt switching observed in traditional RRAM devices, the postsynaptic current (PSC) in these synaptic devices could be gradually depressed or potentiated by continuous pulse stimulation. This control facilitated the realization of two distinct modes corresponding to nonvolatile and quasi-NVM effects, achieved via three-terminal and two-terminal operations of the device, respectively. Both modes showed excellent mechanical durability up to 5000 bending cycles without compromising

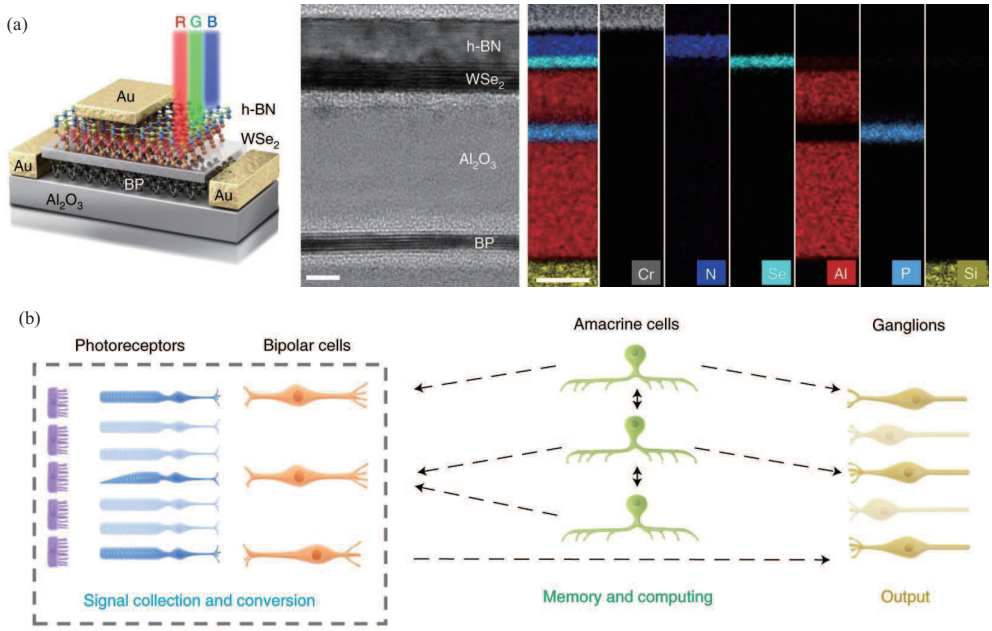


Figure 9 (Color online) (a) Schematic diagram of the device and cross-section STEM image with corresponding energy-dispersive X-ray spectroscopy mappings. The left and right scales are 5 and 20 nm, respectively; (b) schematic of the human retina implementation of MDR, with dashed arrows showing the modulation effect of amacrine cells [78]. Copyright 2022 Springer Nature.

transfer characteristics, leakage current, and long-term excitatory weight change. Notably, in the three-terminal mode, the devices operated with a low energy consumption, requiring less than a fJ/spike when utilizing approximately 10 ns pulse voltage.

Pan et al. [75] reported on a BP/CdS heterostructure-based photonic synapse, which exhibited an average power consumption of 4.78 fJ per training process. In this device, the CdS flakes and 2D BP were used as the photosensitive layer and channel layer, respectively. Zhao et al. [76] highlighted how choosing an appropriate PSC readout layer could decrease the static power. They demonstrated a double-stimuli-responsive synapse based on 2D vdW heterostructures consisting of a responsive layer (WSe_2), a weight-control layer (h-BN), and a readout layer (graphene or MoS_2). All the 2D materials were mechanically exfoliated. The devices, responding to both electrical and optical stimuli, exhibited a response time of 3 μs and optical responsivity of 10^5 A/W, emulating synaptic functionality and optical-sensing capability in an ultracompact device. Further, by leveraging a multiterminal configuration that connects two synapses, it successfully mimics light-modulated dendritic integration.

Exploring the bipolar carrier transport feature of 2D WSe_2, Pan et al. [77] introduced an artificial synaptic device. This device, constructed from a WSe_2/h-BN/$MoTe_2$ floating-gate transistor, exhibited reconfigurable excitation and inhibition of synaptic functions. The fabrication process involved the meticulous exfoliation and sequential transfer of 2D sheets onto a SiO_2 (300 nm)/Si substrate employing a dry transfer technique. Within this structure, WSe_2 functioned as the channel layer, h-BN as the tunneling layer, and $MoTe_2$ as the floating-gate layer. Remarkably, the device demonstrated the ability to modulate multistorage in both n-type and p-type memories through bidirectional voltage amplitudes, achieving an endurance of more than 2000 cycles and an on/off ratio of 3×10^8. Owing to the independent p- and n-memory behaviors, the ambipolar floating-gate device exhibited reconfigurable excitation and inhibition of synaptic functions, enabling the fulfillment of dynamically tailorable synaptic plasticity.

Inspired by the human retina, Zhou et al. [78] proposed a retinomorphic hardware device that leverages the photoconductive characteristics of 2D materials. This device, consisting of a BP/Al_2O_3/WSe_2/h-BN heterostructure, displayed nonvolatile positive and negative photoconductive properties, enabling efficient motion detection and recognition (MDR) (Figure 9). This single device integrates perception, memory, and computing capabilities. The 2D retinomorphic device is sensitive to optical stimuli, mirroring the signal collection and conversion of the photoreceptors in the human eye. The 2D layers of the heterostructure were also prepared by mechanical exfoliation. Nonvolatile positive photocurrents (PPCs) and negative photocurrents (NPCs) could be controlled by programmable electrical and optical pulses, which correspond to the "on" and "off" photoconductive states and emulate the antagonistic shunt and

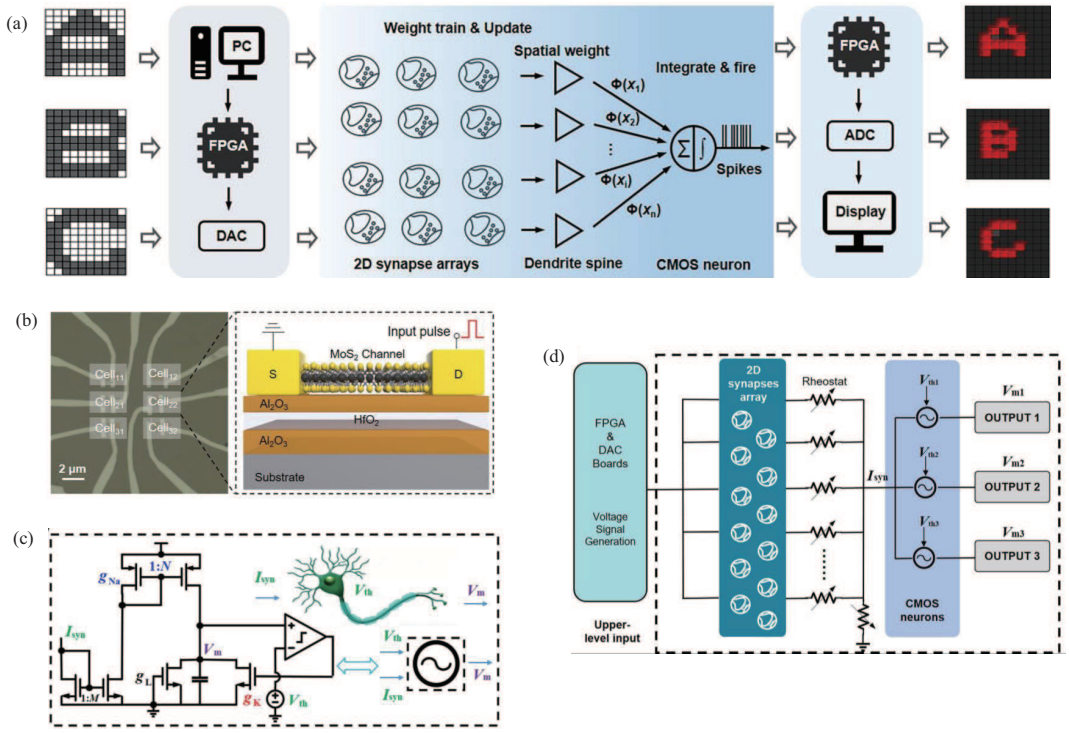


Figure 10 (Color online) (a) Schematic diagram showing the functionality of the hybrid neuromorphic hardware. This includes input signals generated by an FPGA-controlled DAC board, the implementation of spike sequences with various frequencies by a core printed circuit board (PCB) that integrates with 2D synaptic arrays with CMOS neurons, detection and recognition processes managed by an FPGA-controlled analog-to-digital converter (ADC) board, and the display of the target characters on a monitor screen. (b) Schematic diagram of 2 × 3 synaptic array and its two-terminal device, scale bar: 2 μm. For measurements, a voltage bias is applied to the drain, and the source is grounded. (c) Designed circuit for a CMOS neuron, which includes a current mirror, integrating capacitor, leakage transistor, and threshold comparator. $I_{\rm syn}$ is the synaptic array output current acting as neuronal input, $V_{\rm th}$ is the comparator threshold voltage, and V_m is the neuronal output voltage. (d) Detailed system architecture for generating variable-frequency spike sequence outputs. The voltage output from the upper-level FPGA (i.e., DAC output signal) is passed as the input to the 2D synaptic array to adjust the device conductance (weight). A rheostat connected in series with each synapse introduces spatial weights, emulating dendritic spines and compensating for weak synaptic weights. The output current of the 2D synaptic array, $I_{\rm syn}$, is then fed as an input to the CMOS neuronal circuit, and the modulation of $I_{\rm syn}$ influences the charging/discharging of integrating capacitors, ultimately causing the neuron to fire voltage spike sequences with variable frequencies [80]. Copyright 2023 Science China Press.

memory functions observed in bipolar cells within the retina. The device is capable of mimicking multi-signal regulations akin to those in amacrine and ganglion cells by combining "on" and "off" states under various modulations of laser intensity, pulse number, and width. Furthermore, Zhou et al. [78] achieved a 100% separation detection rate of moving trichromatic trolleys without ghosting, utilizing interframe differential computations based on the nonvolatile positive and negative optical conductivity. The detected images were then accurately recognized by a neural network that mapped the device conductance.

The development of arrayed devices is essential for the practical implementation of retina-like and brain-like synapses. To this end, Pan et al. [79] crafted a 5 × 6-pixel array designed to emulate the processes of learning, forgetting, and associative memorization characteristic of the human brain. This was achieved using a monolayer MoS_2 array positioned on a SiO_2/Si substrate, which was developed through an Au nanorod-guided CVD method. The study delved into how varying the wavelength and power of light stimulation could influence the photocurrent's low resistance states, thereby enabling synaptic functions. The array showed the ability to reconstruct ambiguous and incomplete memories by utilizing associated images, thus mimicking the intricate intelligent behaviors of associative memory and logical reasoning found in humans.

Zhou et al. [80] introduced a hybrid neuromorphic hardware system by transferring the CVD-grown by transferring the CVD-grown MoS_2 onto a stacked dielectric layer composed of $Al_2O_3/HfO_2/Al_2O_3$ deposited on a heavily doped Si substrate. This complex structure, consisting of two MoS_2 arrays with twelve synaptic devices and three CMOS neural circuits (Figure 10), was integrated into a field-programmable gate array (FPGA) controlled digital-to-analog converter (DAC) board. The inclusion of peripheral DAC boards enhanced the system functionality, enabling it to recognize user-defined alphabetic and numeric

inputs. This was made possible through a synergy of hybrid integration, frequency coding, and feature extraction techniques. In this device, the 2D MoS_2 served as the channel, while the $Al_2O_3/HfO_2/Al_2O_3$ stack (measuring 7/3/30 nm in thickness) acted as the charge tunneling and trapping layer. This setup facilitated the storage of carriers injected through the drain, which in turn modulated the channel conductance. The synaptic device employed a two-terminal type architecture without a gate terminal, allowing electrical pulses to serve as the presynaptic stimulus and the reading of channel current to act as the postsynaptic response (synaptic weight) directly at the drain electrode.

5 Conclusion

The ongoing Program has reached several significant milestones, adhering to its proposed research agenda. We have achieved controllable growth in terms of phase, layer number, and uniformity for various TMDs, including magnetic 1T-CrS_2, bipolar transport WSe_2, high-mobility $PtSe_2$, and typical MoS_2. The vdW heterostructures, combining different TMDs and organic semiconductors, have been successfully developed. Their interlayer exciton behaviors have been investigated in detail [81]. Novel in-memory computing and logic devices have been designed, showcasing excellent properties in terms of size, energy consumption, switching speed, endurance, and multifunctionality. These fabricated neuromorphic devices exhibit brain-like functions [82]. Moreover, the development of 2D/3D PDs, which are easily fabricated and compatible with Si-CMOS technologies [83], has resulted in superior performance, making them suitable for practical applications that do not require extremely rapid response speeds.

Since the discovery of graphene in 2004, the need for a commercial electronic or optoelectronic product based on 2D materials, beyond mere prototype demonstrations, has become increasingly apparent to further the development of the 2D materials field [84–89]. The main challenge lies in achieving the manufacturing readiness levels required for Si-compatible 2D electronics and optoelectronics, which vary depending on the targeted applications [90]. The catalytic growth nature of 2D materials complicates the direct synthesis of a high-quality 2D layer on an underlying substrate. Consequently, patterned transfer and etching techniques that preserve the properties of 2D materials are essential for fabricating complex heterostructures to achieve varied functions. Property or function modification of 2D materials through doping and defect engineering remains challenging, especially for atomically thin materials. Ultimately, the success of integrating 2D materials into Si technology lines depends on the availability of 2D materials with the desired qualities and properties, as well as the integration process itself.

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