SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

May 2024, Vol. 67, Iss. 5, 152403:1–152403:7
https://doi.org/10.1007/s11432-023-3902-6

Mitigating set-stuck failure in 3D phase change memory: substituting square pulses with surge pulses

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Received 19 September 2023/Revised 18 October 2023/Accepted 17 November 2023/Published online 19 April 2024

Abstract In the devices that integrate phase change memory (PCM) and ovonic threshold switching (OTS), the OTS threshold voltage often surpasses the RESET operation voltage of PCM. The conventional application of square pulses hinders the successful completion of the SET operation in these integrated devices. To address this challenge, a novel pulse called the surge pulse is introduced, which comprises a high amplitude pulse for OTS activation and a low amplitude pulse for PCM operation. By employing COMSOL simulation, the operational effectiveness of both square pulses and surge pulses is validated. Test results reveal that using a square pulse to operate the integrated device accelerates the occurrence of SET-stuck failure (SSF). In contrast, the surge pulse enables the integrated device to operate for at least 1000 cycles while preserving the essential cyclic characteristics. Additionally, an investigation into the overshoot component of the surge pulse is conducted, revealing that an increase in overshoot amplitude and pulse width also accelerates the emergence of SSF. By applying the theory of ion migration induced by the electric field, the root cause of SSF in integrated devices is explained, and the accuracy of the theory is validated through the application of a reverse pulse. In summary, this study elucidates the rationality of replacing the square pulse with a surge pulse, presenting a superior approach for operating PCM and OTS integrated devices.

Keywords surge pulse, phase change memory (PCM), integration, SET-stuck failure (SSF), square pulse

1 Introduction

Presently, phase change memory (PCM) exhibits tremendous potential across various applications owing to its non-volatile nature, high speed, simple structure, and multi-level storage capabilities [1–3]. However, PCM arrays often encounter significant leakage current [4], thereby necessitating the connection of gated devices in series to address this concern [5, 6]. Moreover, as the reduction in size presents challenges for further advancements in storage density [7], the emergence of three-dimensional PCM technology serves as an effective solution to enhance storage density [8, 9]. Ovonic threshold switching (OTS) technology [10], known for its elevated open current density, minimal leakage current, and expeditious opening speed [11–14], utilizes chalcogenide materials and follows a similar preparation process as PCM [15, 16]. Furthermore, OTS holds the potential for continuous three-dimensional stacking, rendering it highly suitable for integration with PCM to create three-dimensional PCM architectures [17]. However, after the integration of PCM with OTS, it becomes imperative to adjust the operation of PCM to ensure compatibility with the integrated devices.

Currently, square pulses are predominantly utilized to operate integrated devices. By adjusting the amplitude, pulse width, and rising and falling edges of the square pulse to match the parameters of various integrated devices, both the SET and RESET operations can be achieved [18–21]. However, it is essential that the applied pulse amplitude for operating an integrated device meets the threshold voltage of OTS in order to activate it. Nevertheless, in practical scenarios, the threshold voltage of OTS may be higher, potentially surpassing the RESET operation voltage of PCM. When a square pulse with a short falling

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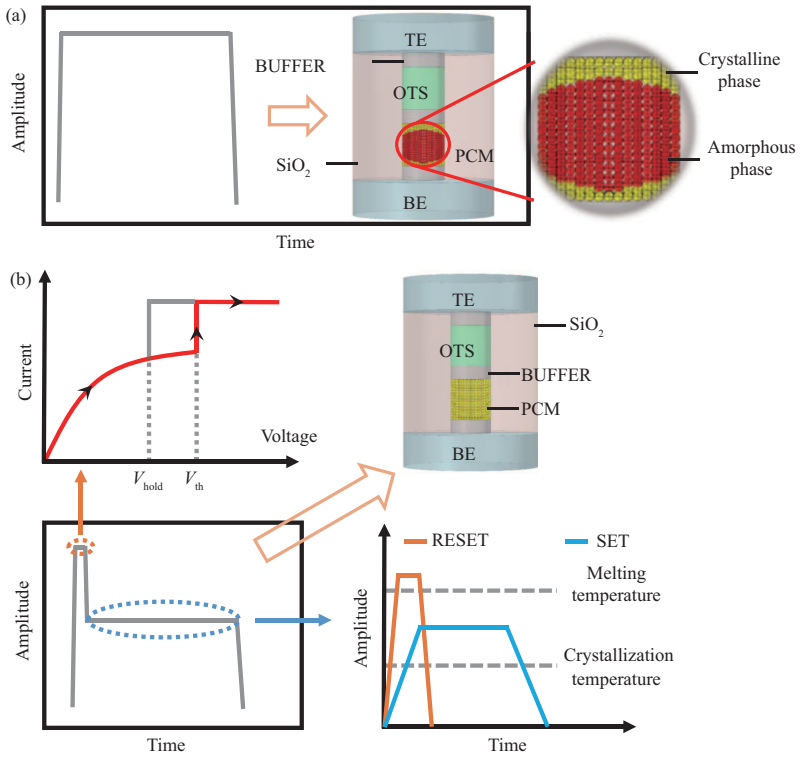

Figure 1 (Color online) (a) Traditional square pulse diagram, which fail to SET integrated devices with high threshold voltage in OTS, resulting in PCM remaining in an amorphous state; (b) surge pulse diagram, utilizing a high-amplitude pulse to activate OTS and a low-amplitude pulse to operate PCM, allowing for successful SET operation in integrated devices and transforming PCM into a crystalline state.

edge is applied to the integrated device, the temperature of PCM exceeds the melting point, inhibiting successful crystallization and completion of the SET operation, as shown in Figure 1(a). In terms of the RESET operation, utilizing a square pulse leads to unnecessary power consumption. To address these concerns, a newly developed pulse, referred to as the surge pulse, is proposed, as shown in Figure 1(b). The surge pulse exhibits a high pulse amplitude based on the threshold voltage of OTS and a pulse width determined by the OTS opening time, thus allowing for effective OTS activation. In addition, the surge pulse incorporates a low pulse amplitude based on the operation voltage of PCM, accompanied by a pulse width aligned with the operational pulse width of PCM. This low pulse is employed to effectively operate PCM.

In this manuscript, a pioneering operation pulse, namely the surge pulse, has been specifically devised to facilitate the efficient functioning of integrated devices with a high threshold voltage in OTS. Initial simulation validation using COMSOL Multiphysics was followed by a comprehensive experimental evaluation of the integrated device. Notably, it was observed that the utilization of a square pulse led to an accelerated onset of SET-stuck failure (SSF) [22]. Conversely, when the surge pulse was employed, the device exhibited a fundamental cyclic characteristic, thereby ensuring enhanced reliability. Moreover, a meticulous inquiry into the overshoot component of the surge pulse was undertaken to elucidate the underlying SSF mechanism, which was subsequently corroborated through experimentation.

2 Results and discussion

The COMSOL simulation model utilized a confined structure, encompassing W electrodes at both top and bottom, a surrounding layer of SiO2 as the medium, and C buffer layers placed between the PCM and OTS, as well as between the aforementioned layers and the electrodes [19, 23]. Furthermore, the viability of the surge pulse was examined through deliberate adjustment of the threshold voltage of OTS to a heightened level.

In the COMSOL simulation, a square pulse was initially applied. As shown in Figures 2(a) and (b), the majority of the PCM reached temperatures around 1150 K, indicating a state of melting. As a

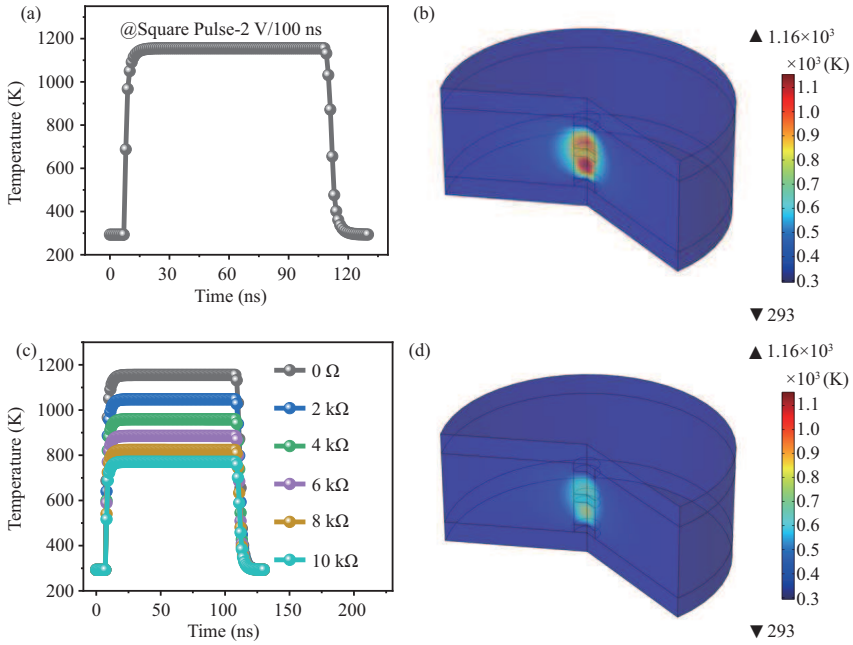

Figure 2 (Color online) (a) Temperature-time characteristic curve of PCM during the application of square pulse; (b) temperature distribution of the integrated device during the application of square pulse; (c) temperature-time characteristic curve of PCM with a gradual increase in series resistance from 0 to 10 kΩ; (d) the temperature distribution of the integrated device when the series resistance is set to 10 kΩ.

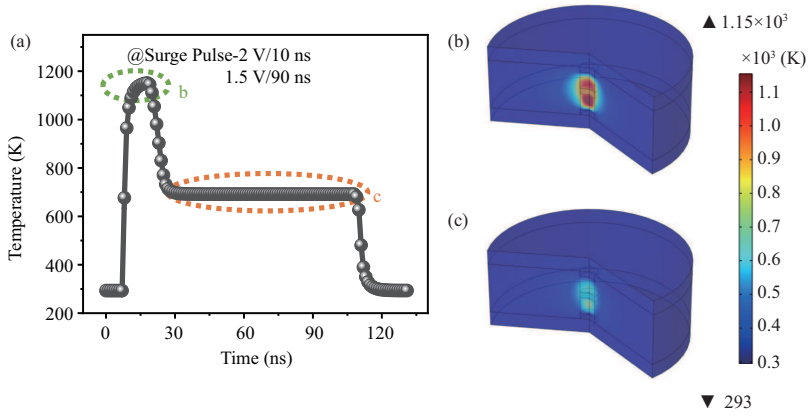

Figure 3 (Color online) (a) Temperature-time characteristic curve of PCM during the application of a surge pulse; (b) temperature distribution of the integrated device during the high amplitude pulse of the surge pulse; (c) temperature distribution of the integrated device during the low amplitude pulse of the surge pulse.

result, the utilization of a square pulse with a short falling edge failed to SET the integrated device. To address this predicament, the option of augmenting the series resistance is presently being investigated in order to lower the temperature of the PCM. The simulation outcomes, shown in Figures 2(c) and (d), exhibit a gradual increment in series resistance from 2 to 10 kΩ, ultimately resulting in a decrease in PCM temperature to approximately 750 K. Consequently, the SET operation of the integrated device can be effectively accomplished by applying a square pulse subsequent to the incorporation of the 10 kΩ resistance in series.

Continuing, the utilization of the surge pulse within the COMSOL simulation was executed. As shown in Figure 3, subsequent to a momentary interval of heightened temperatures during the high pulse, the PCM consistently upheld a temperature of approximately 700 K for a protracted duration throughout the low pulse. This protracted exposure to diminished temperatures facilitated the entirety of the PCM's crystallization process. Consequently, the surge pulse could be employed for the SET operation of integrated devices without necessitating a series resistance.

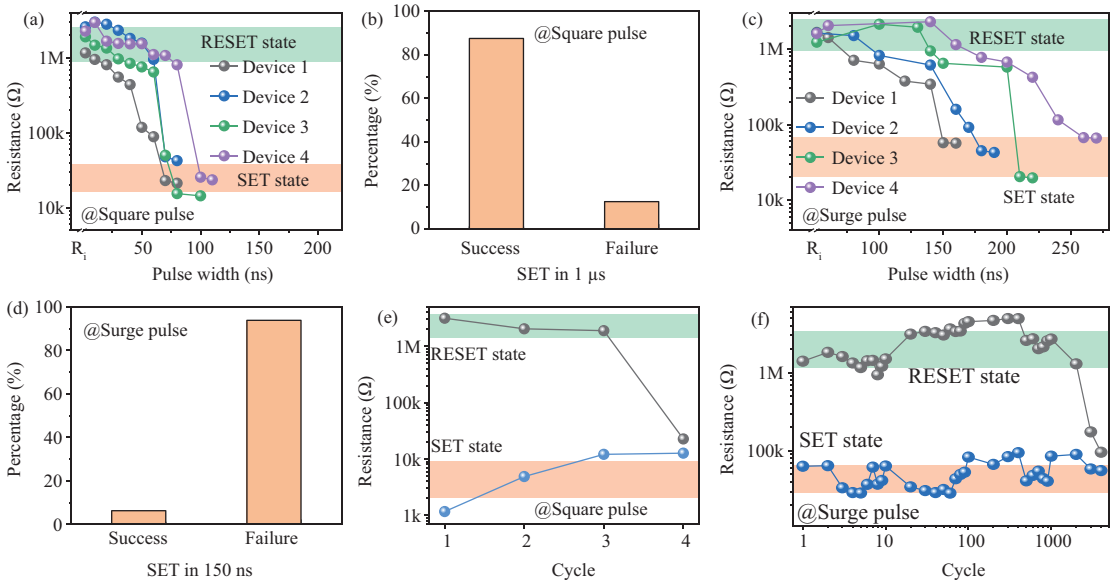

Figure 4 (Color online) (a) Curve depicting the variation in resistance of the integrated device with pulse width during square pulse application, where Ri represents the initial resistance state; (b) statistics indicating the success rate of completing SET operation within 1 μs during square pulse application; (c) curve depicting the variation in resistance of the integrated device with pulse width during surge pulse application; (d) statistics showing the success rate of completing SET operation within 150 ns during surge pulse application; (e) cyclic characteristic curve of the operating integrated device with a square pulse; (f) cyclic characteristic curve of the operating integrated device with a surge pulse.

The simulation outcomes reveal that solely employing a square pulse is insufficient to achieve the full SET operation of the device. Nevertheless, the SET operation can be effectively executed by utilizing a surge pulse, albeit resulting in a brief period of heightened temperatures during the process. This high temperature phase might potentially impact the crystallization speed of the PCM. To validate the simulation outcomes and evaluate the speed, a speed test was performed on both the square pulse and surge pulse. The test results during the application of the square pulse are presented in Figures 4(a) and (b). Merely 12.5% of the integrated devices conform to the simulation outcomes, unable to complete the SET operation within the designated timeframe of 1 μs. Surprisingly, for the remaining 87.5% of the integrated devices, they successfully accomplished the SET operation, contradicting the previous analysis. Additionally, Figure 4(c) illustrates the gradual transition of the PCM from high resistance (HRS) to low resistance (LRS) as the pulse width increases when the surge pulse is applied. In this scenario, the integrated device effectively achieves the SET operation. However, for individual PCM units operating under the same amplitude, the SET operation can be accomplished within a mere timeframe of 150 ns. Conversely, when the surge pulse is implemented on the integrated device, as shown in Figure 4(d), 93.75% of the devices necessitate a longer SET operation time than the 150 ns benchmark. As a result, the speed of the SET operation for integrated devices is diminished by the overshoot of the surge pulse.

While the completion of the SET operation is permissible through the application of a square pulse, it causes the temperature of the PCM beyond its melting point. It is widely accepted that this operation proves to be more detrimental to the device and showcases a low level of repeatability. Hence, a comparative cyclic test was carried out between the square pulse and the surge pulse. The results of this test are presented in Figures 4(e) and (f). Remarkably, the integrated device subjected to the square pulse experiences a significant decline in cyclic ability, leading to the occurrence of a failure referred to as SSF after a mere five cycles. On the contrary, the integrated device utilizing the surge pulse exhibits strong cyclic capacity, with a minimum cycle time of 1000. Therefore, while the square pulse can successfully accomplish the SET operation, it displays poor repeatability and hastens the onset of SSF.

In the previous test, the amplitude and pulse width of the surge pulse overshoot were intentionally set to the minimum standard. The amplitude of the overshoot portion was established utilizing the threshold voltage of the OTS, while the pulse width was determined by the opening duration of the OTS. To probe the extent of amplitude and pulse width within the overshoot portion, supplementary tests were executed with heightened values. The outcomes are shown in Figures 5(a) and (b), wherein the amplitude of the overshoot portion was increased by 0.5 and 1 V, respectively. With the gradual increase in amplitude,

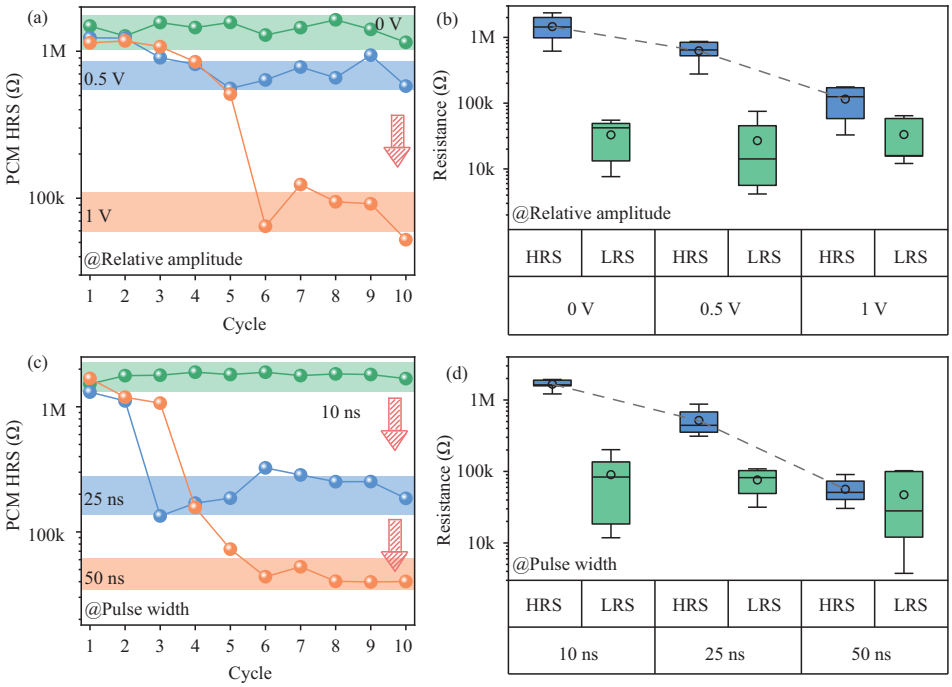

Figure 5 (Color online) (a) Variation of the HRS curve of the integrated device as a function of the number of cycles under different overshoot amplitudes during surge pulse application; (b) distribution of HRS and LRS in integrated devices subjected to surge pulse application with varying overshoot amplitudes; (c) variation of the HRS curve of the integrated device as a function of the number of cycles under different overshoot pulse widths during surge pulse application; (d) distribution of HRS and LRS in integrated devices subjected to surge pulse application with varying overshoot pulse widths.

the HRS of the integrated device progressively diminished, ultimately giving rise to SSF. Analogously, as shown in Figures 5(c) and (d), the pulse width of the overshoot portion was adjusted to 25 and 50 ns, respectively. The results were similar to those observed with the altered amplitude. The incremental pulse width led to a gradual reduction in the HRS of the integrated device, culminating in the occurrence of SSF. Therefore, it is advisable to keep the amplitude and pulse width of the surge pulse overshoot as minimal as possible, while ensuring adherence to the requirements of the OTS threshold voltage and OTS start time.

SSF has garnered attention in various domains, including the realm of storage [24] and the realm of neural morphology [25–27]. The theory of field-induced ion migration has been proposed to elucidate the emergence of SSF [24, 28]. Increasing the amplitude of the overshoot portion engenders an amplified field intensity, thereby hastening the rate of ion migration. Similarly, extending the pulse width of the overshoot part prolongs the duration of ion migration. Consequently, both factors contribute to the emergence of SSF. In the case of a square pulse, it not only furnishes the requisite amplitude to elevate the PCM temperature to its melting point but also features a lengthy pulse width. As a result, the employment of a square pulse expedites the onset of SSF.

In order to substantiate the theory of field-induced ion migration, the utilization of reverse pulse (RP) was employed to evaluate the recovery of the integrated device from the SSF state [24]. Initially, the amplitude of the surge pulse overshoot was increased to induce SSF. The test results are shown in Figures 6(a) and (b). Following the occurrence of SSF, the integrated device underwent retesting, wherein it was observed that the RESET voltage exceeded the RESET voltage under normal conditions by 0.3 V. Consequently, the previous voltage was deemed inadequate to complete the RESET operation. To address this matter, an RP was implemented on the integrated device based on the current RESET voltage, resulting in a recovery of the RESET voltage to 1.7 V. Subsequently, the device was subjected to normal cycling by utilizing the standard surge pulse. Furthermore, the pulse width of the surge pulse overshoot was increased to induce SSF. The obtained results corresponded with the earlier observations concerning the amplitude of the overshoot, as shown in Figures 6(c) and (d). Following the occurrence of SSF, the RESET voltage of the integrated device surpassed the RESET voltage under normal conditions by 0.4 V. The application of RP in this scenario also facilitated the recovery of the RESET voltage to 1.8 V. Normal operation was then achieved by utilizing the standard surge pulse. In summary, the successful

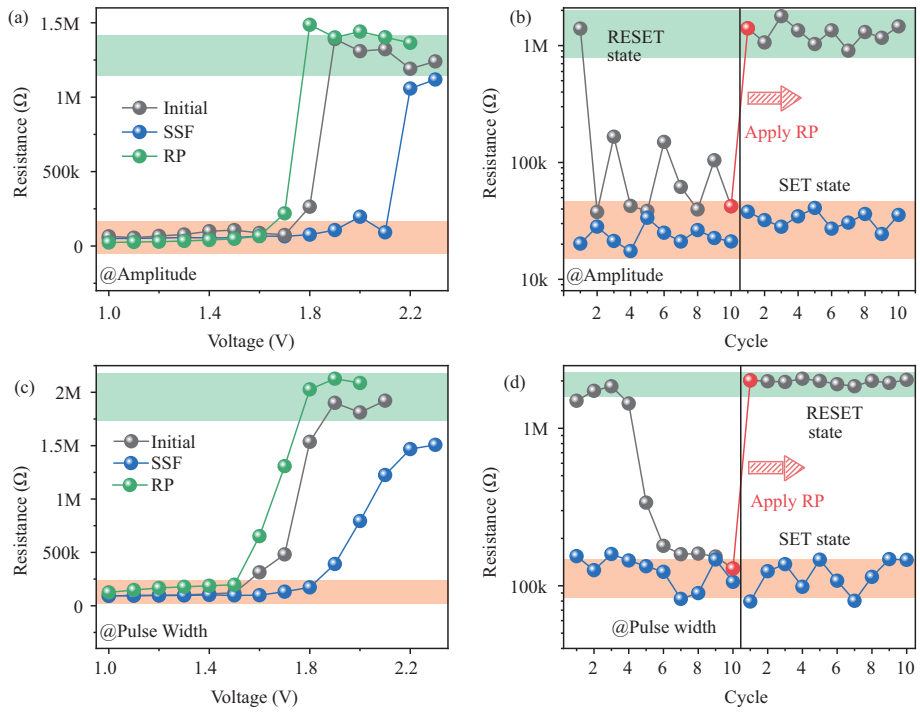

Figure 6 (Color online) (a) Comparison of the RESET operation threshold voltage of the integrated device in three states, where the SSF of the integrated device is induced by increasing the amplitude of the surge pulse overshoot; (b) a cyclic comparison before and after the application of RP, where the occurrence of SSF in the integrated device is due to an increase in the amplitude of the surge pulse overshoot; (c) comparison of the RESET operation threshold voltage of the integrated device in three states, where the SSF of the integrated device is induced by increasing the pulse width of the surge pulse overshoot; (d) a cyclic comparison before and after the application of RP, where the occurrence of SSF in the integrated device is due to an increase in the pulse width of the surge pulse overshoot.

recovery of the integrated device from the SSF state through the application of RP provides further evidence in support of the field-induced ion migration theory.

3 Conclusion

This paper introduces a unique and innovative pulse called the surge pulse, tailor-made for integrated devices characterized by high threshold voltage in OTS. The surge pulse comprises a pulse with a high amplitude for OTS activation, coupled with a pulse of lower amplitude for PCM operation. Through COMSOL simulation, the performance of square pulses in operating integrated devices has been greatly enhanced by augmenting the series resistance. Remarkably, the surge pulse itself attains the same desirable outcome. Experimental testing has revealed that the utilization of square pulse operation tends to hasten the occurrence of the SSF phenomenon. Conversely, the utilization of surge pulse operation helps preserve the fundamental cycling characteristic of the device. Furthermore, it has been observed that accelerating the onset of SSF is achieved by augmenting the amplitude and pulse width of the surge pulse overshoot portion. This phenomenon is elucidated by the principle of ion migration under field induction, which is further corroborated through the implementation of reverse RESET pulses. To sum up, a fresh approach to operating integrated devices comprising PCM and OTS is presented, providing valuable insights and a novel methodology for future research in this realm.

Acknowledgements This work was supported by National Key R&D Program of China (Grand No. 2021YFA1202804), National Natural Science Foundation of China (Grant No. 62174065), and Hubei Provincial Natural Science Foundation of China (Grant No. 2021CFA038). The authors acknowledge the support from Hubei Key Laboratory of Advanced Memories & Hubei Engineering Research Center on Microelectronics.

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