Appendixes A

1 Background

Gallium nitride (GaN), a state-of-the-art candidate for next-generation communication technology, has received much emphasis for decades owing to its outstanding material characteristics, such as high electron velocity, wide band gap and excellent Johnson's figure of merit (JFOM)[1-5]. GaN based High-Electron-Mobility-Transistors (HEMT) have been well investigated for its promising application for high frequency, high voltage, and high-power.

The theoretical material limit, however, sets obstacles for conventional single-heterostructure GaN HEMTs to keep up with rising power amplifying demand, despite numerous efforts including compensation-doping in buffer [6], high Al fraction barrier [7], surface treatment [8], and field plate design [9].

Meanwhile, GaN based double-channel HEMTs (DC-HEMTs) have attracted great deal of attention due to higher current drive and potential advantage of two channels in RF circuit design [10] and application in power switch [11]. Nevertheless, the gate access to the lower channel is typically ineffective for traditional AlGaN/GaN/AlGaN/GaN DC-HEMTs due to an extra AlGaN barrier between the two channels [12], which lead to poor off-state current and short-channel effect.

In this instance, a thinner AlN barrier was used to minimize the thickness of double channels and to improve gate control for the bottom channel while maintaining the benefit of high current drive. Optimised AlGaN/GaN/AlN/GaN or AlN/GaN/AlN/GaN double heterostructure has achieved promising gate control and large-signal characteristic at low drain voltage, according to published work [12-14] (less than 30V). However, AlN owns larger lattice mismatch with GaN, thereby the bottom AlN barrier has more negative influence on polarization of upper GaN channel. As a result, the carrier density is decreased in each channel [14]. High Al fraction in AlN, on the other hand, results in a greater inverse piezoelectric effect [15] and a worsened breakdown characteristic of the device, which prevents the use of DC-HEMT for high voltage. Aside from that, lag phenomenon at high voltage is not a negligible issue for GaN HEMT realizing high power [16].

A DC-HEMT with a graded bottom channel (DCGC-HEMT) was offered as a solution to the aforementioned issues. The $Al_{0.3}Ga_{0.7}N/GaN/Al_xGa_{1-x}N$ layer forms the foundation of the DC structure, x graded from 0.3 to 0, top down, and it is shown in Fig.1(a). The thickness of each layer is 20/10/10 nm. Several reported work on graded AlGaN has exhibited the its intrinsic advantages. Sanyam Bajaj et al. [17] reported a graded AlGaN channel transistor with shortened gate to channel distance, improved drain current and linearity. Ling Yang et al. [18] reported using graded AlGaN structure to improve breakdown characteristic. According to reference[19], 3DEG（3-dementional electron gas）can help suppress trap influence induced in the buffer by "shield effect" and graded AlGaN helps form 3DEG[17].

A reference DC-HEMT with an ultra-thin bottom AlN barrier (3-nm AlN, DCTB-HEMT) is offered for the rigor of the entire work in order to methodically investigate the benefits of DCGC-HEMT. According to Fig. 1(b), the reference device's heterostructure is $Al_{0.3}Ga_{0.7}N/GaN/AlN/GaN$.

Systematic evaluation revealed that the DCGC-HEMT performed better in terms of saturation current, breakdown voltage, and drain lag. The graded AlGaN bottom barrier, as can be shown, offers a great solution to realize good gate control and high saturation current. The power performance of the DCGC-HEMT outperformed the DCTB-HEMT at 3.6 GHz continuous wave

mode as well. With V_{DQ} = 60V, the maximum PAE (PAE_{max}) of DCGC-HEMT was increased from 56.98% of DCTB-HEMT to 64.98%, and the saturation output power (P_{sat}) of DCGC-HEMT increased from 10.44 W/mm of DCTB-HEMT to 11.76 W/mm. This work demonstrated an effective solution in minimizing power lag for double channel HEMT by taking advantage of the graded barrier's electrostatic shielding effect.

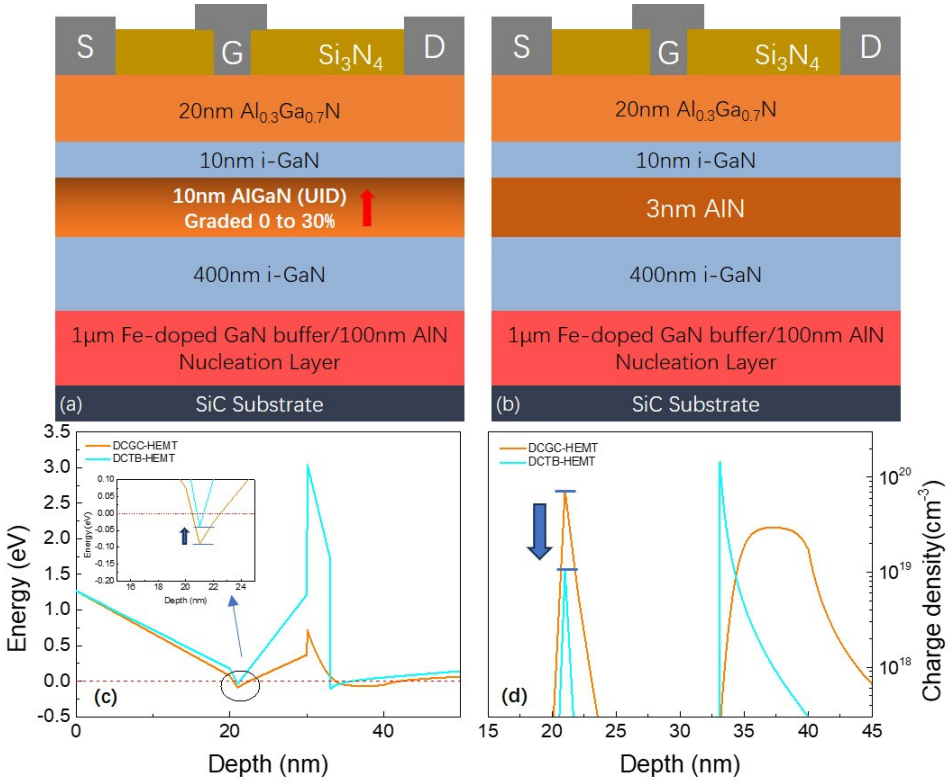

Figure 1 Schematic cross-section of (a) DCGC-HEMT and (b)DCTB-HEMT, (c)Band energy and (d) carrier concentration under gate of DCGC-HEMT (orange line) and DCTB-HEMT (blue line).

2 Growth epitaxy and device fabrication

The DCGC-HEMT and DCTB-HEMT heterostructures are grown via metal-organic chemical vapor deposition (MOCVD) on 3-inch SiC substrates. The schematic cross-section of two structures are shown in Fig. 1(a) and (b), respectively. The DCGC-HEMT consists of a 1-μm GaN intentionally doped with iron(concentration: 2.4×10^{19} cm^{-3}), a 400-nm unintentional-doping(UID) GaN, a 10-nm graded AlGaN bottom barrier, a 10-nm UID GaN top channel and a 20-nm $Al_{0.3}Ga_{0.7}N$ top barrier. Aside from bottom barrier: a 3-nm AlN barrier, the DCTB-HEMT owns same structure with DCGC-HEMT. The fabrication of devices started with ohmic contact. Metal stack Ti/Al/Ni/Au was evaporated on source/drain region and then a rapid temperature annealing (RTA) was performed at 830 °C for 50 s in an N_2 atmosphere. Via nitrogen vertical implantation technique, the devices achieved electrical isolation. The ohmic contact resistance (R_c) of DCGC structure and DCTB structure are recorded as 0.28 Ω·mm and 0.30 Ω·mm by the transmission-line method (TLM). Following that, a 120-nm Si_3N_4 passivation layer was deposited on the surface of the device via plasma-enhanced chemical vapor deposition (PECVD). After removing additional passivation located at gate region through CF_4 dry etching in a low power mode, the Ni/Au metal stack was evaporated for gate electrode. The devices have a gate length (L_g), a gate width (W_g), and a gate-drain spacing (L_{gd}) of 0.5 μm, 2×100 μm, and 3 μm, respectively.

3 Results and discussion in detail.

Fig.1 (c) and (d) are band energy and carrier concentration distribution with depth under gate region of DCGC-/DCTB-HEMT, respectively. It can be seen that, influenced by AlN barrier, the quantum well of top AlGaN/GaN heterostructure in DCTB-HEMT is shallower than that in DCGC-HEMT. As a. result, carrier concentration in top channel of DCTB-HEMT is less than that of DCGC-HEMT. Fig. 2(a)&(b) and (c)&(d) are TEM (Transmission electron microscope) cross-sectional image of DCGC-/DCTB-HEMT, respectively. Fig 2 (a) and (c) show different layers of two heterostructure in 10-nm scale. When the scale of cross-sectional image of two heterostructure is 2-nm, shown in fig 2 (b) and (d), the difference on microstructure of GaN, graded AlGaN and AlN get more obvious.

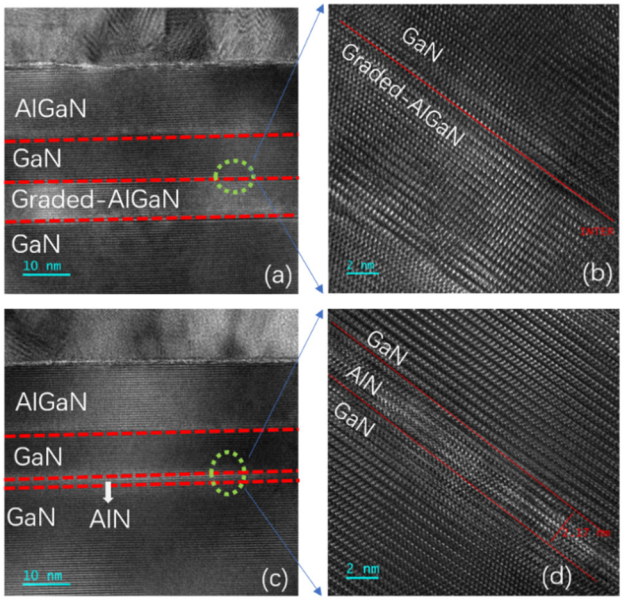

Figure 2 TEM (Transmission electron microscope) cross-sectional image of (a)&(b) DCGC- and (c)&(d) DCTB-HEMT.

Fig.2 (a) are the transfer curves of two devices. As is shown in the picture, double-hump profile is observed from transconductance (Gm). The two channels are both depleted with gate bias below pinch-off voltage. When gate voltage (V_g) positively shifts to the threshold voltage (V_{th}), the bottom channel turns on first. The upper channel subsequently turns on when gate voltage keeps positively shifting[20]. Thereby, the left and right humped profile of transconductance refer to the characteristic of bottom and upper channel, respectively. Considering the different gate access to bottom channel of two devices, the maximum transconductance ($G_{m,\,max}$) of bottom channel from DCTB-HEMT (209 mS/mm) is greater than that from GCGB-HEMT (189 mS/mm). Thinner bottom barrier strengthens gate control to bottom channel. Due to same structural upper heterostructure, the $G_{m,\,max}$ of upper channel form two devices are nearly same (226.8 mS/mm from DCTB-HEMT and 221.7 mS/mm from DCGC-HEMT). Aside from transconductance, DCGC-HEMT exhibited higher saturated drain current (I_d) and more negative threshold voltage. As is shown in Fig.2(a), the saturated drain current (gate voltage bias at 2V) of DCGC- and DCTB-HEMT are 1298.8 mA/mm and 1140.3 mA/mm, respectively. In addition to that, the V_{th} of DCGC-HEMT owning a 1.5V negative shift is observed in the picture (-5.9V of DCGC-HEMT and -4.4V of DCTB-HEMT). The DCGC-HEMT exhibits wider gate voltage range. Fig.3 (b) are breakdown characteristic of DCTB- and DCGC-HEMT. The measurement was operated on off-state at V_{GS}= -10 V, guaranteeing pinch-off for two devices. As shown in the picture, the breakdown voltage is increased from 124 V of DCTB-HEMT to 165 V of DCGC-HEMT, increased by 41 V. The simulation of electric field of two devices are shown in Fig. 3(c) and (d). According to reference[19], the graded AlGaN make electrons in channels redistribute, and reduce the peak value of electric field. Therefore, the breakdown characteristic is improved.

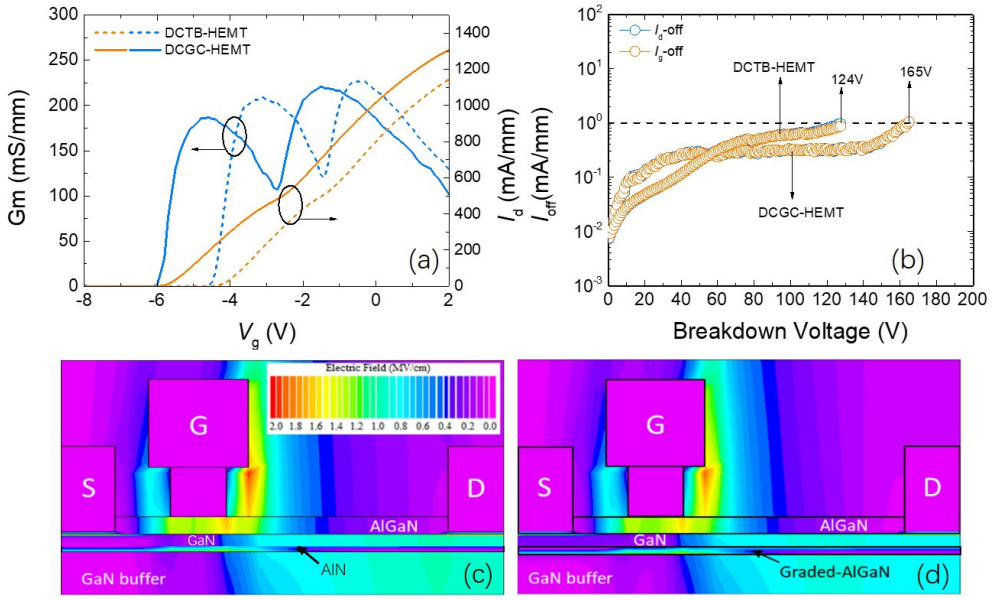

Figure 3 (a)Transfer curves of DCGC-HEMT (solid line) and DCTB-HEMT (dash line). (b)Breakdown characteristic of two devices. Electrical Field TCAD simulation of (c) DCGC-HEMT and (d) DCTB-HEMT.

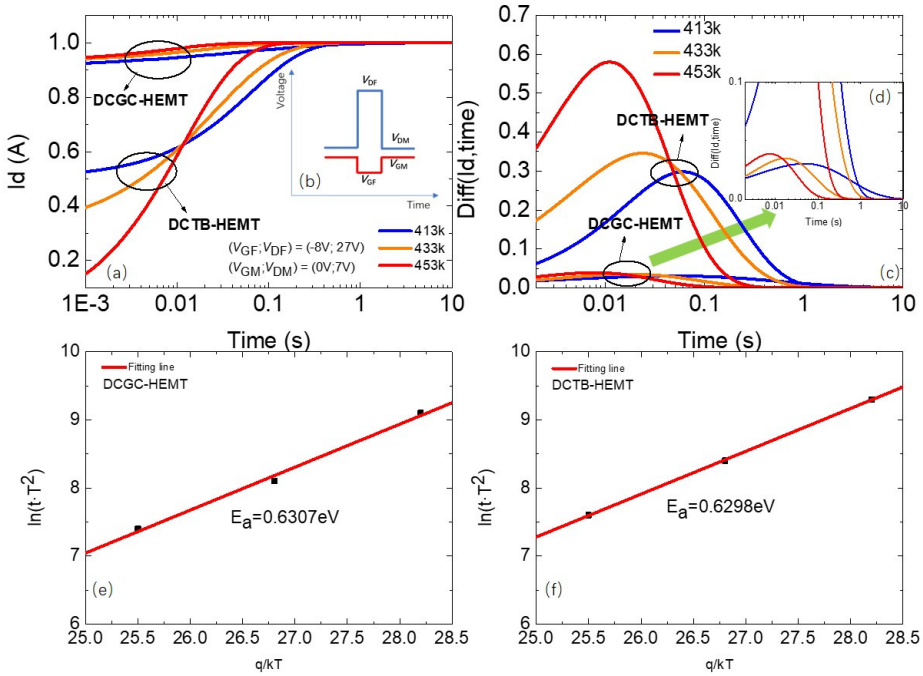

Figure 4 (a) drain transient current normalized to final of DCTB/DCGB-HEMT, (b) bias condition versus time,(c)&(d) related differential value of transient current of DCTB/DCGB-HEMT, (e)&(f) activation energies of DCTB/DCGB-HEMT extracted from Arrhenius plots.

Traps in devices has a significant impact on device RF characteristic, and it is essential to evaluate properties of traps. According to references[21], studying the current transient through multiexponential transient measurements is an accurate technique to describe trap properties. In this work, the transient current measurement was carried out by a 4200 semiconductor analyzer using two pulsed signals. In order to analyze traps characteristics under both gate region and gate-drain access region, the quiescent bias point was set with high negative V_{GS} and high positive V_{DS}: (V_{GF}; V_{DF}) = (-8V; 27V), promoting gate- and drain-dependent trapping. The measurement was carried out by analyzing the charge de-trapping with bias condition: (V_{GM}; V_{DM}) = (1V; 7V). Three measurement temperature 413k, 433k, and 453k were chosen to extrapolate the Arrhenius plots of the traps in terms of activation energies and capture cross-sections. Fig.4 (a) exhibits drain transient current normalized to final of DCTB/DCGB-HEMT at three temperatures and the insertion image (b) is bias condition versus time. According to the curve, the transient current of DCTB-HEMT has a more distinguished value between the start and the final. The current recovering process of DCTB-HEMT is much more rapid, which may be caused by more electrons being captured by traps. Fig.4 (c) and (d) shows related differential value of transient current from two device at different temperatures. According to the differential value, the DCTB-HEMT owns higher peak value at each temperature. As transient current is related to presence of density of defect state, DCTB-HEMT activates more density of defect state compared with DCGB-HEMT at same gate voltage. The graded barrier has a good shield-effect on traps. Fig. 4(e) and (f) summarize the activation energies from two devices, 0.6307eV and 0.6398eV, respectively. Two devices have quite similar activation energies. According to literature reports[21], it belongs to a common trap, ionized iron, in GaN buffer.

To investigate electrical characteristic influenced by high drain voltage, the drain lag analysis of two devices were extracted from measured transient drain current characteristics. Using Keysight 4200 DC analyzer, the gate voltage is fixed at 0 V, and a voltage pulsed from 0.1 V (V_{DS0}) to 20/40 V (V_{DS}) is applied to drain. The pulsed voltage is maintained at 20/40 V for 500 μs (pulse width = 0.5 ms), and after that, the drain voltage is back to 0.1 V until next period (pulse period = 10 ms). As is exhibited in Fig.5 (a), at the beginning of a pulse width, an initial drain current I_{D1} is detected and then a decreased drain current I_{D2} is detected in the end of a pulse width. All detected current is normalized to I_{D1} for convenient comparison. According to reference[22], the value I_{D2}/I_{D1} could be used to quantitatively define drain lag, called drain lag ratio (DLR). The normalized I_d at V_{DS} = 20/40 V and DLR of two devices with different V_{DS} is shown in Fig.5 (b) and (c), respectively. According to the image, the drain lag of both devices degrades with V_{DS}. Moreover, DLR characteristic of DCGC-HEMT is better than that of DCTB-HEMT at same drain bias condition. On one hand, DLR is heavily influenced by drain bias condition; on the other hand, two different bottom barriers have different suppression in drain lag.

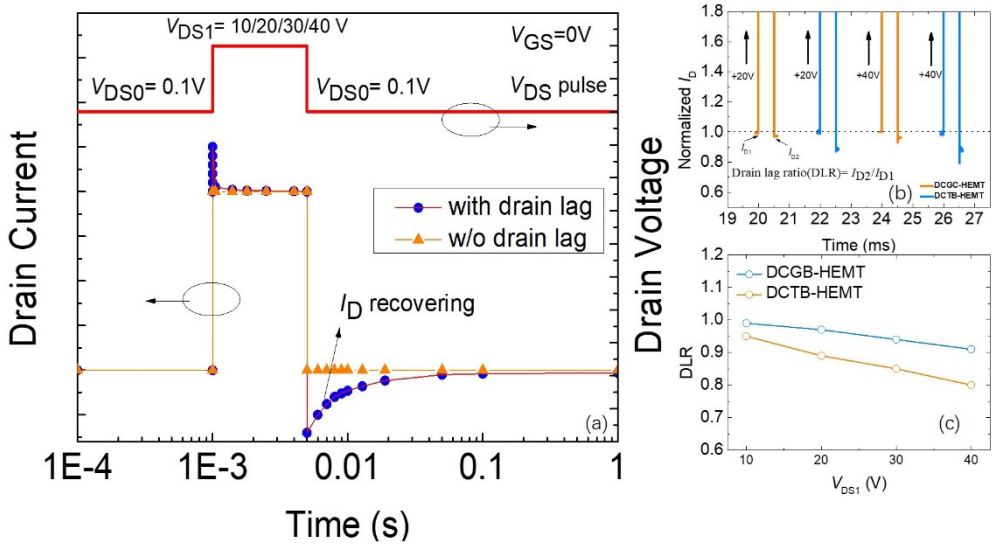

Figure 5 (a) Testing process, (b) –(c) Drain lag measurement of DCGC-/DCTB-HEMT at different drain voltage.

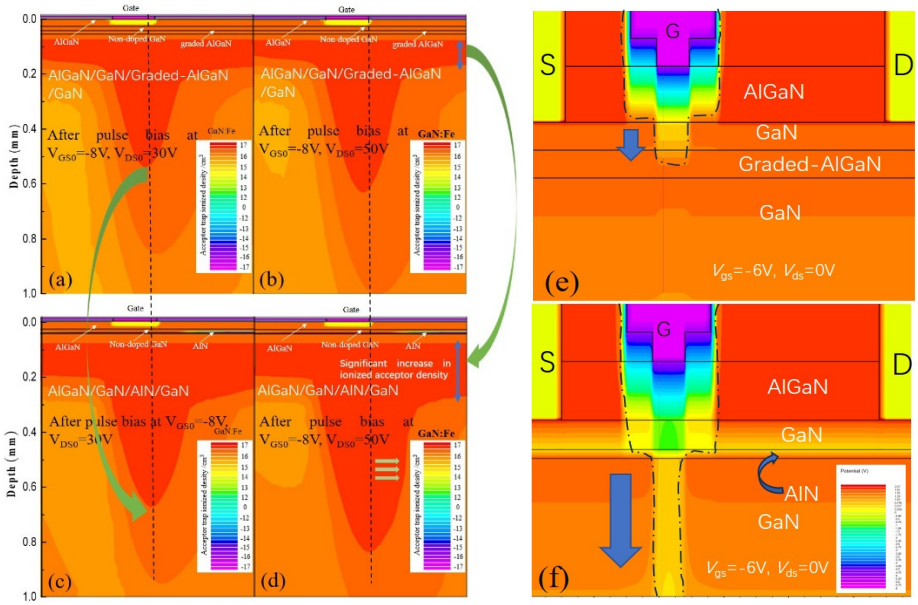

Figure 6 Simulation of trap ionized density of (a&b)DCGC- and (c&d) DCTB-HEMT Simulation potential of (e) DCGC- and (f) DCTB-HEMT at *V*gs = -6V,Vds=0V.

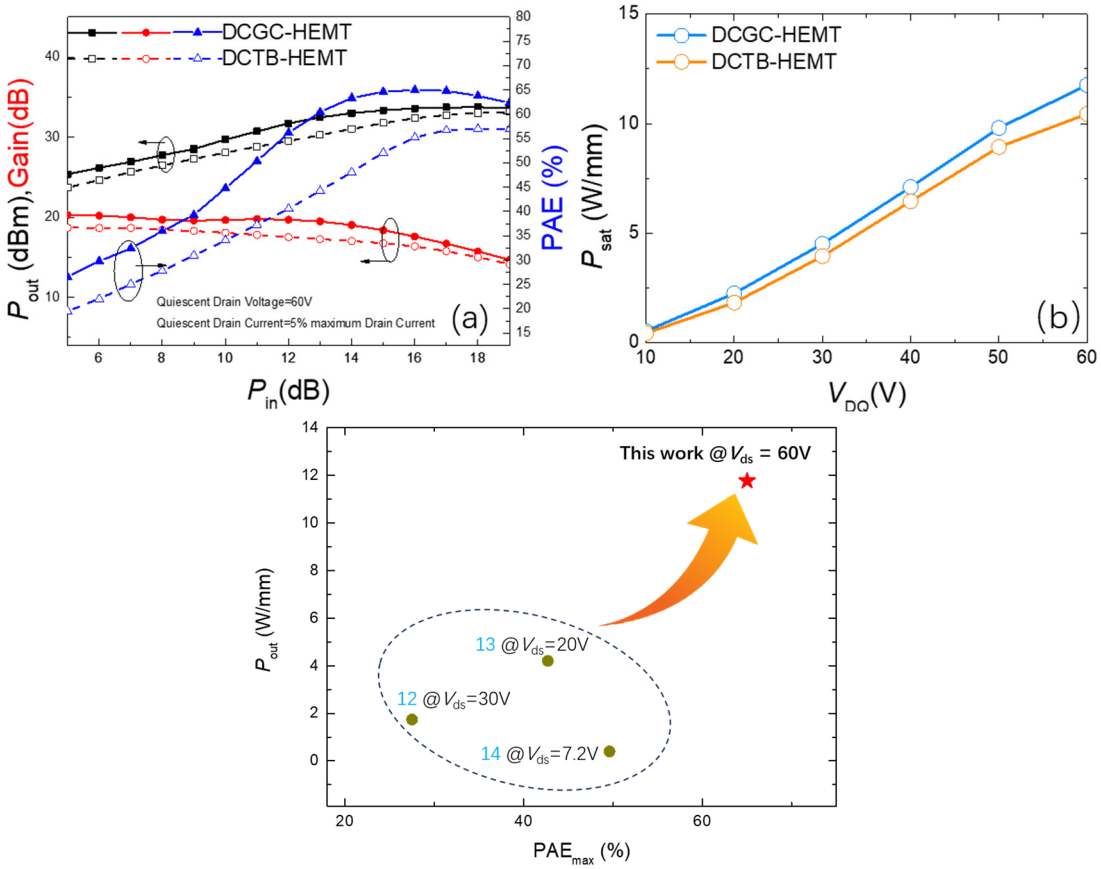

Figure 7 (a) Output characteristic of DCGC-/DCTB-HEMT at V_{DQ}=60V; (b) Saturated output power (P_{sat}) with different quiescent drain voltage (V_{DQ}) of DCGC-/DCTB-HEMT; (c) Benchmark of P_{out} and PAE_{max} of double-channel HEMTs.

In order to figure out difference in drain lag, the acceptor trap ionized density is simulated by TCAD. Fig. 6(a), (b), (c) and (d) are simulation of acceptor trap ionized density of DCGC-/DCTB-HEMT at different bias condition from TCAD. Considering the influence of iron doping tail [23], the doping depth is set much close to the bottom channel. As is shown in the picture, with increased V_{DS0}, acceptor trap ionized density of both devices increases. Nevertheless, the total ionized trap density of DCGC-HEMT is always less than that of DCTB-HEMT at same bias condition, indicating the bottom barrier of two devices have different influence on activating acceptor traps, resulting in different acceptor trap ionized density. The potential of two devices with Vgs = -6V, Vds = 0 V are simulated and shown in Fig. 6 (e) and (f). As it can be seen, with same Vgs, the potential under gate in DCTB-HEMT expand much deeper than DCGC-HEMT. It can be concluded that DCGC-HEMT has a electrostatic shielding effect in activating acceptor trap, implying its better DLR.

At 3.6 GHz continuous-wave mode, class AB bias condition, the on-wafer measurement of DCGC-/DCTB-HEMT were performed through Maury load-pull system to analyze their large-signal characteristics. Fig.7 (a) is output performance of two devices at V_{DQ} = 60V. DCGC-HEMT gets a PAE_{max} of 64.98%, and a P_{sat} of 11.76 W/mm while DCTB get a PAE_{max} of 56.7% and a P_{sat} of 10.30W/mm. Fig.7 (b) is saturated output power (P_{sat}) with different V_{DQ} of two devices. In the picture, DCGC-HEMT shows stronger power performance than DCTB-HEMT, especially at high V_{DQ}. Effective electrostatic shielding effect contributes to excellent large signal characteristic of DCGC-HEMT. Fig.7 (c) is the benchmark of P_{out} and PAE_{max} of Double-channel HEMT, respectively. As is exhibited in the figure, traditional double-channel HEMTs working voltage is below 30V, and exhibit poor RF performance. Our work greatly improved working voltage, P_{out} and PAE_{max} of double-channel HEMT, which reveals the potential of double channel HEMTs in high voltage and high power.

4 Conclusions

In summary, the double channel HEMT with graded channel (DCGC-HEMT) and the double channel HEMT with ultra-thin barrier (DCTB-HEMT) are systematically investigated. Due to utilization of graded AlGaN bottom barrier to provide more carriers and shield traps in buffer, the DCGC-HEMT exhibited greater saturated drain current and suppression in drain lag. As a result, DCGC-HEMT shows greater advantages in output performance. The breakthrough in superior large-signal characteristic reveals the potential in high performance RF PA application.

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