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A self-selecting memory element based on a method of interconnected ovonic threshold switching device

Jinyu WEN[1,2], Lun WANG[1], Jiangxi CHEN[1], Hao TONG[1,2,3*] & Xiangshui MIAO[1,2,3]

[1]*School of Integrated Circuits, Huazhong University of Science & Technology, Wuhan* 430074*, China;*
[2]*Institute of Artificial Intelligence, Huazhong University of Science & Technology, Wuhan* 430074*, China;*
[3]*Hubei Yangtze Memory Laboratories, Wuhan* 430205*, China*

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Currently, the 3-D cross-point structure has been successfully applied in phase change memory (PCM) to achieve scalable and stackable memory arrays [1]. The ovonic threshold switching (OTS) selector consists of a memory element that is used to suppress the parasitic current in the 3-D cross-point arrays due to its highly nonlinear current-voltage (I-V) characteristics which are significant for large-scale memory arrays [2]. However, the integration of PCM and OTS increases the complexity of memory arrays and even limits the performance of the memory cell. Recently, it has been reported that threshold voltage ($V_{\rm th}$) could increase obviously by the opposite polarity of voltage pulses in SiGeAsTe OTS devices [3]. The new phenomenon as reported indicates that threshold switching devices are promising to store messages themselves, meaning a way for self-selecting memory (SSM). The key working principle of the SSM is that threshold switching devices have two threshold voltage states which can be reversibly transformed under electrical operation. Based on the SSM of OTS devices, the complexity of the memory arrays will be fundamentally reduced. To realize the SSM, $V_{\rm th}$ needs to be changed controllably with some history dependent, like polarity dependent as reported. Besides, the difference between two $V_{\rm th}$ states ($\Delta V_{\rm th}$) means the memory window of the SSM, which is critical for large-scale arrays. The large enough $\Delta V_{\rm th}$ can ensure the distinction between state "0" and state "1" of SSM. Thus, it is critical to study the methods to realize controllable and large $\Delta V_{\rm th}$. At present, the studies about the $\Delta V_{\rm th}$ phenomenon mainly focused on finding the polarity dependent in the chalcogenide layers of OTS devices, such as SiGeAsTe [3]. However, it is a challenge to enlarge $\Delta V_{\rm th}$ of OTS devices controllably due to its unclear mechanism. Besides, in some chalcogenide layers of OTS devices, the $\Delta V_{\rm th}$ phenomenon is not obvious and stable enough to realize SSM. The $GeTe_9$ material is a promising OTS device due to its excellent endurance (1E10 cycles) and low leakage current (10 nA) [4], but it has nearly little $\Delta V_{\rm th}$ because of the lower $V_{\rm th}$. Thus, it is valuable to explore the $\Delta V_{\rm th}$ phenomenon with some methods that can easily get adjustable and large $\Delta V_{\rm th}$ for low $V_{\rm th}$ OTS materials. In this work, we propose a method to realize an SSM based on interconnected OTS devices. $\Delta V_{\rm th}$ of the interconnected $GeTe_9$ device is 0.34 V at cycle tests while it is just 0.09 V in a single $GeTe_9$ device. The leakage current of the interconnected device is 48 nA to ensure selectivity. Based on this method, we found that $\Delta V_{\rm th}$ of the interconnected device is relevant to $V_{\rm th}$ of the connected device so it is easily controllable and adjustable. In addition, cycles of read-and-write operations are passed accurately. Our work provides a method of OTS devices to get controllable and large $\Delta V_{\rm th}$ used as SSM for high-density memory.

Experimental. The $GeTe_9$ OTS device was fabricated with a via-hole structure (feature size is 250 nm) (see Figure 1(b)). First, the connection of the OTS devices was based on the bottom electrode deposited by physical vapor deposition (PVD). Second, electron beam lithography (EBL) was used to pattern the via-holes and inductively coupled plasma etching (ICPE) was used to etch the SiO_2 layer to get via-holes. Then, an ultraviolet (UV) lithograph was used to pattern the OTS layer and the top-electrode (TE) layer. After patterning, the 30 nm OTS film and the 100 nm W top-electrode film were deposited by magnetron sputtering in sequence. The OTS film was deposited by sputtering the $GeTe_9$ targets. Finally, after a lift-off process, the fabrication process was finished and the devices could be tested. In addition, the fast I-V characterization was done with a Keysight B1500A semiconductor analyzer with an embedded B1530A waveform generator/fast measurement unit (WGFMU). In order to ensure that the OTS devices will not fail due to excessive current impact, a 500 Ω resistor is connected in series during the tests.

Results. At first, to show $\Delta V_{\rm th}$ of the $GeTe_9$ OTS device as a comparison, the measurement with a series of pulses was applied, as shown in Figure 1(a). For negative readout polarity, the positive pulse ($V_{\rm pos1}$) was applied as the RESET pulse of SSM and $V_{\rm th}$ was higher after the opposite polarity pulse ($V_{\rm th1}$) than after the same polarity pulse ($V_{\rm th2}$, $V_{\rm th3}$). Because $V_{\rm th}$ was from $V_{\rm th1}$ to $V_{\rm th2}$ with the first negative pulse ($V_{\rm neg1}$), $V_{\rm neg1}$ was seen as the SET pulse of SSM. To confirm $\Delta V_{\rm th}$ repeatedly by the polarity pulses instead of the variations of the OTS devices, the same measurement was repeated and the distributions of $V_{\rm th}$ were shown in Appendix A Figure A1(a). We used the value of the median-to-median difference to define $\Delta V_{\rm th}$, which is just 0.09 V. The results indicate that $\Delta V_{\rm th}$ is too little to be used as a memory window, so it is hard to be applied for

* Corresponding author (email: tonghao@hust.edu.cn)

SSM application. To enlarge the $\Delta V_{\rm th}$ phenomenon of the polarity dependent, we applied an interconnected structure device, as shown in Figure 1(b). The applied voltage was from an OTS device TE to another OTS device TE. With the local charge of OTS devices, $\Delta V_{\rm th}$ can be enlarged in the interconnected device (see Figure A2). What is more, the polarity of $V_{\rm mid}$ is the same as the polarity of the applied pulse and its polarity is obvious. Thus, the interconnected device is promising to realize a larger $\Delta V_{\rm th}$ of low $V_{\rm th}$ materials like $GeTe_9$.

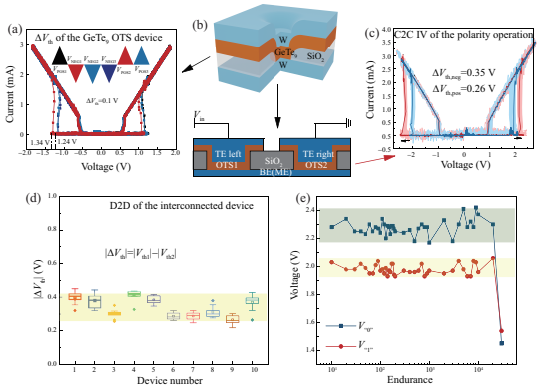

Figure 1 (Color online) (a) $\Delta V_{\rm th}$ (0.1 V) in $GeTe_9$ OTS device with the positive pulse as the RESET pulse and the first negative pulse as the SET pulse; (b) schematic diagram of via-hole structure and the interconnected device; (c) cycle to cycle *I-V* of the interconnected device, indicating stable $\Delta V_{\rm th}$ for both polarities; (d) device to device of $\Delta V_{\rm th}$ in the interconnected device; (e) $V_{\text{“0”}}$ and $V_{\text{“1”}}$ during the endurance tests.

To verify the effect of two OTS material layers, the interconnected device was tested, as shown in Figure 1(b). Similar pulses as Figure 1(a) were applied, as shown in Figure 1(c). The value of $\Delta V_{\rm th}$ increases to 0.35 V, much larger than $GeTe_9$ devices. To ensure large $\Delta V_{\rm th}$ phenomenon can be repeated, the same measurement of cycle tests was repeated to the interconnected device, as shown in Figures 1(c) and A1(b). There is still a 0.35 V difference between $V_{\rm th1}$ and $V_{\rm th2}$ during cycle to cycle tests with inconspicuous variations, which can ensure the read margin of the SSM. Besides, the interconnected device also has good selectivity with a leak current test (48 nA), as shown in Figure A3(a). Moreover, the distributions of $V_{\rm th2}$ and $V_{\rm th3}$ are almost coincident (see Figure A3(b)), demonstrating $V_{\rm th}$ will maintain stability at the SET state. It is important for SSM to read “1” repetitively. At last, a similar measurement was repeated for the ten interconnected devices, as shown in Figure 1(d). The distributions of $\Delta V_{\rm th}$ for the ten devices are about 0.35 V, meaning that the $\Delta V_{\rm th}$ phenomenon could be repeated well in the interconnected device.

Then, the storage feasibility of the interconnected device was verified through a read-and-write operation (see Figure A4(a)). In Figure A4(a), the positive pulse is defined as RESET pulse, the negative pulse whose voltage is higher than $V_{\text{“0”}}$ is defined as SET pulse, and the negative pulse whose voltage is higher than $V_{\text{“1”}}$ but lower than $V_{\text{“0”}}$ is defined as Read pulse. If the device has switched on with RESET pulse before, Read pulse cannot switch on the device and read out off-current ($I_{\rm off}$), so the state “0” can be read repetitively. If the device has switched on with SET pulse before, Read pulse can switch on the device and reads out on current ($I_{\rm on}$). Upon the results of Figure A3(b), $V_{\rm th}$ will have little change besides Read pulses, so the state “1” can be read repetitively. The endurance results are in Figures 1(e) and A4(b). $\Delta V_{\rm th}$ keeps larger than 0.2 V throughout the cycle test. The voltage of the Read pulse is 2.1 V and the results of $I_{\rm out}$ are in Figure A4(b). There is an obvious $I_{\rm out}$ window between $I_{\rm on}$ and $I_{\rm off}$. Moreover, it needs to be explained that $I_{\rm off}$ is obtained by Read pulse with the fast-sampling module of the B1530A, so it is significantly higher than the actual $I_{\rm off}$ due to the insufficient sampling accuracy of WGFMU under 10 mA range. The endurance is 2×10^4, confirming the feasibility of the read-and-write scheme of threshold switching memory. For further endurance optimization, it is important to reduce the operating current, which can protect the device from excessive currents. The effective way of reducing operating current is to introduce a semiconductor material (such as Ge, C [5]) as an interfacial layer between the chalcogenide glass and the electrode.

Conclusion. We demonstrated an SSM element based on a method of interconnected OTS devices. $\Delta V_{\rm th}$ of the interconnected structure device was proved an increment from 0.09 to 0.35 V compared to that of a single $GeTe_9$ OTS device. The leakage current of the interconnected device (48 nA) was tested to ensure the self-selecting characteristics. Through testing the voltage of the middle electrode, we found $\Delta V_{\rm th}$ of the interconnected device was relevant to $V_{\rm th}$ of the connected $GeTe_9$ devices, meaning that it is controllable and adjustable. Besides, to verify the function of the SSM, a read-and-write operation was adopted and the endurance reached 2×10^4. This work indicates the interconnected device can enlarge $\Delta V_{\rm th}$ of the single device and it is promising to get larger $\Delta V_{\rm th}$ for the low $V_{\rm th}$ OTS devices to be used as the SSM to realize high-density memory.

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Supporting information Appendix A. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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