SCIENCE CHINA
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• Supplementary File •

A Self-Selecting Memory element based on a method of interconnected Ovonic Threshold Switching device

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Appendix A Other important data covered in the letter

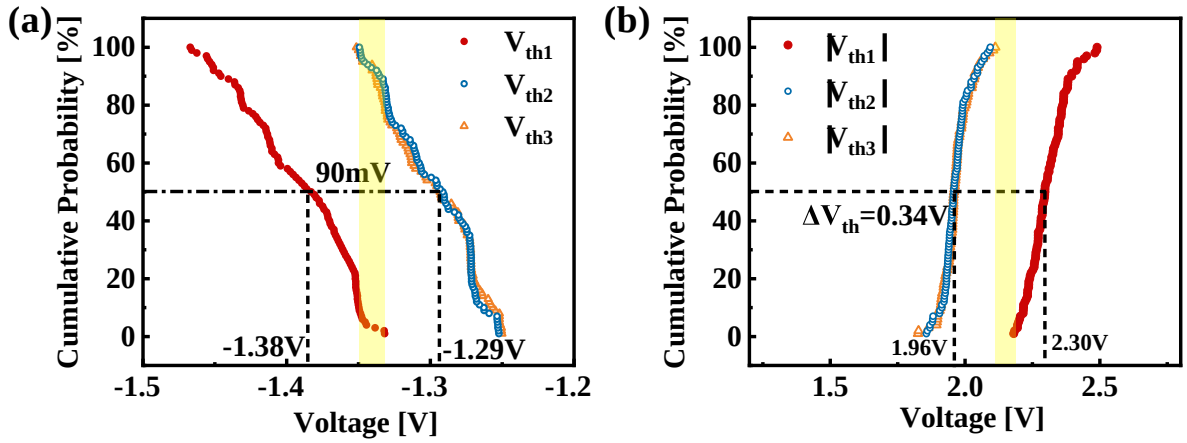

Figure A1 (a) The distributions of V_{th} in $GeTe_9$ OTS device; (b) The distributions of V_{th} in the interconnected device of $GeTe_9$ OTS devices.

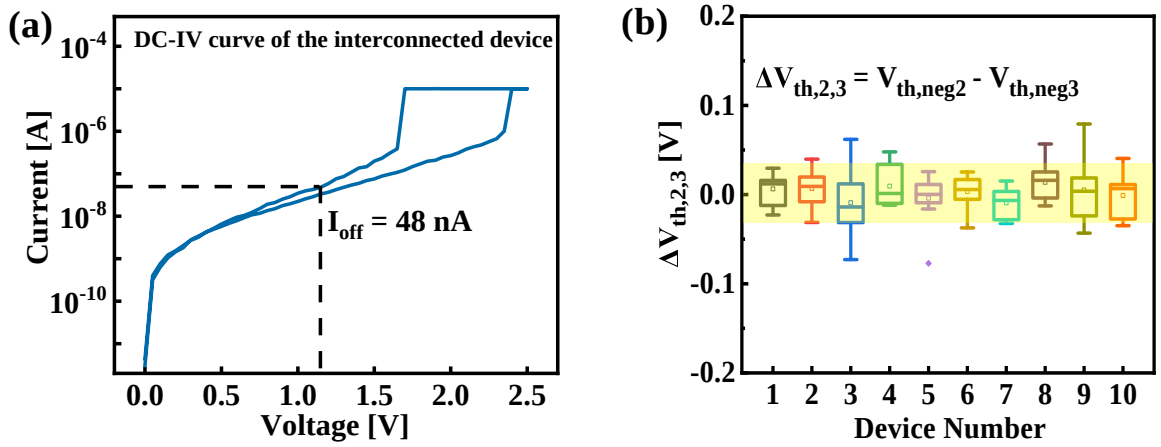

Figure A2 (a) Typical DC-IV characteristics of the interconnected device with the leakage current (48 nA); (b) Device to device of $\Delta V_{th,2,3}$ in the interconnected device.

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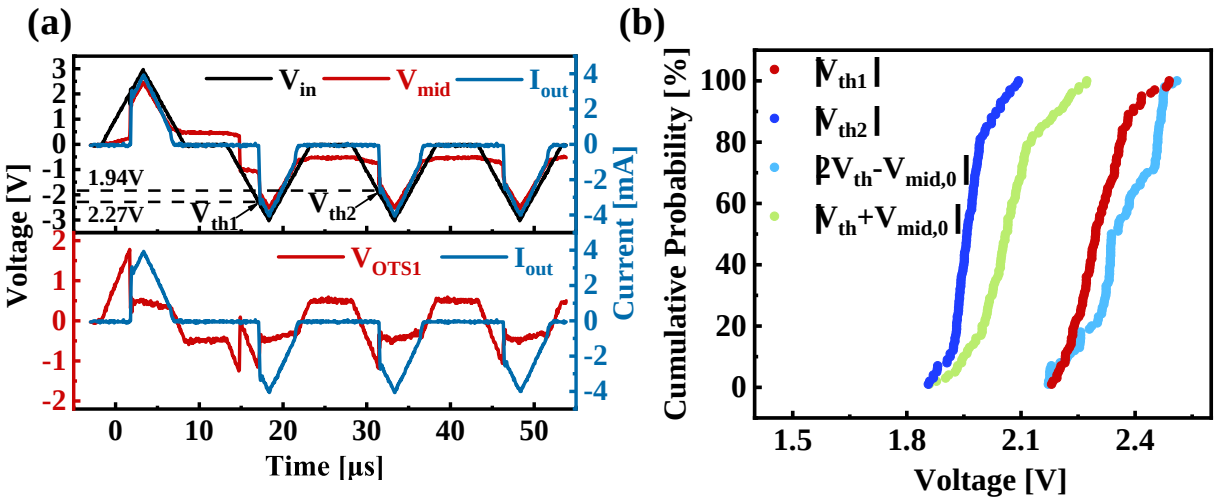

Figure A3 (a) The relationship besides V_{in}, V_{mid} and I_{out} still in the upper part of the figure and the relationship between the voltage of OTS1 (V_{OTS1}) and I_{out} in the lower part of the figure, showing V_{th1} and V_{th2} are relevant to V_{th} of $GeTe_9$ device. V_{mid} still maintains voltage bias after the input pulse applied ($V_{mid,0}$) due to the charge phenomenon. Thus, after a positive pulse, when the input voltage increases, V_{OTS1} increases synchronously. When V_{OTS1} is higher than its threshold voltage (V_{th}), OTS1 is switched on and off momentarily with V_{mid} changed. However, due to V_{mid} is lower than the threshold voltage of OTS2, the interconnected device will not be switched on until V_{in} is higher than the sum of V_{th} and V_{mid}. Therefore, it is thought that V_{th1} is related to $2V_{th}$-$V_{mid,0}$. After a negative pulse, the node charge has the same polarity as V_{in}. When OTS1 is switched on, V_{in} is higher than the threshold voltage of OTS2. Therefore, it is thought that V_{th2} is related to V_{th}+$V_{mid,0}$; (b) V_{th1} and V_{th2} of cycle tests compared with $2V_{th}$-$V_{mid,0}$ and V_{th}+$V_{mid,0}$ of cycle tests.

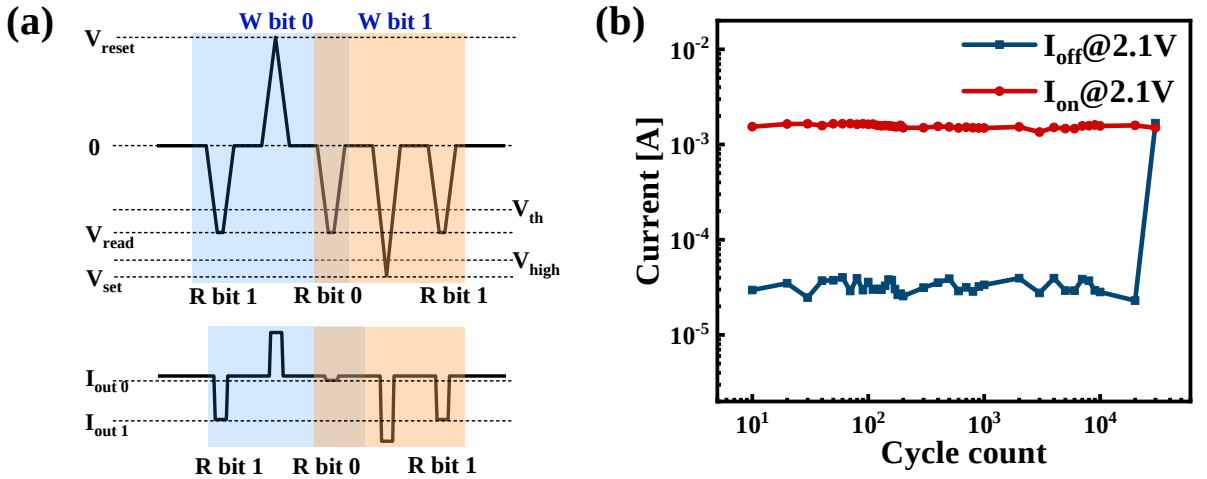

Figure A4 (a) Schematic diagram of a read-and-write operation of OTS-only memory; (b) I_{off} and I_{on} during the cycle tests.