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Ohmic-contact ballistic 2D InSe transistors: promising candidates for more Moore electronics

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The scaling of silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) approaches its physical limits at a gate length (L_G) of 12 nm and supply voltage (V_{DD}) of 0.6 V according to the International Roadmap for Devices and Systems (IRDS) blueprint, which defines the final integration density and power consumption for silicon-based chips. These performance limits result in the end of silicon-based Moore's law, as further miniaturization of silicon will bring untenable interfacial scattering and degraded carrier mobility. Two-dimensional (2D) layered semiconductors are proposed as successors to support further miniaturization due to their excellent electrostatics from the atomic-scale thickness and high carrier mobility from the smooth dangling-bond-free surface [1–3]. Substantial *ab initio* quantum transport simulations have predicted that 2D FETs outperform silicon FETs and can extend Moore's law down to the sub-10 nm L_G region [4].

However, no experimental 2D semiconductor-based FETs can exhibit comparable or better performance than silicon FETs because it is a great challenge to simultaneously realize a low-resistance Ohmic contact and ultrathin effective oxide thickness (EOT) in 2D FETs. Until very recently, Peng's group [5] from Peking University fabricated an Ohmic-contact ballistic InSe FET with an extremely small EOT of 0.4 nm and channel length of L_G = 10–20 nm. A strategy to improve electrode/2D channel contacts is to utilize a Y-doping-induced semiconductor-to-semimetal phase transition. Y substitution is precisely controlled at the active In sites for only the top layer of the few-layer InSe, while the underlying layers remain semiconducting. Because the interface between Y-doped InSe and pristine InSe remains van der Waals, there is no Fermi-level pinning effect. As a result, an n-type Ohmic contact is formed with a very small contact resistance of 62 $\Omega \cdot \mu$m. They deposited an ultrathin high-κ dielectric (2.6-nm-thick HfO_2) on a highly doped silicon substrate to form a back gate. The strategy to overcome the growth difficulty of a high-quality ultrathin dielectric on a smooth surface is to use 0.3–0.4 nm Al_2O_3 as the seed layer, which allows atomic layer deposition of 2.6-nm-thick top-gate HfO_2 on few-layer InSe. The HfO_2/Ti/Au top-gate also isolates the InSe channel from the moisture and oxygen environment, preventing the degradation of the as-prepared (by mechanical exfoliation) high-quality few-layer InSe.

A high on-state current of 1.5 mA/μm is predicted for a 7-nm-gate monolayer (ML) InSe FET at a V_{DD} of 0.64 V [6]. Inspiringly, the best on-state currents of the fabricated 2D InSe FETs (three-layer) reach 1.20 and 1.43 mA/μm at V_{DD}s of 0.5 and 0.7 V, respectively, which at least double that of the 20-nm-gate InGaAs (IBM) FinFET at a V_{DD} of 0.5 V (0.60 mA/μm) [7] and approach that of the 10-nm-node silicon (Intel) FinFET at a V_{DD} of 0.7 V (1.55 mA/μm) [8] (Figure S5(f) in [5]). The best peak transconductance of the 2D InSe FETs is up to 6 and 7.2 mS/μm at V_{DD}s of 0.5 and 0.7 V, respectively, which at least triple that of the InGaAs FinFET at a V_{DD} of 0.5 V (2.2 mS/μm) and slightly surpasses that of the silicon FinFET at a V_{DD} of 0.7 V (5.7 mS/μm) (Figure S5(g) in [5]). Both the on-state currents (0.7–1.2 mA/μm) and transconductances (3–6 mS/μm) of the 2D InSe FETs at a V_{DD} of 0.5 V are approximately one order of magnitude larger than those of other sub-50-nm 2D FETs at a larger V_{DD} = 1 V (Figures 3(c)–(d) in [5]). The best reported delay time and energy-delay product (EDP) of the 2D InSe FET are 0.32 ps and 4.32×10^{-29} Js/μm, which surpass those of the IRDS projected limit of 1.32 ps and $\sim 8 \times 10^{-28}$ Js/μm for a 12-nm-gate silicon sheet FET (Figures 3(g) and (h) in [5]), due to the extremely small capacitance from the atomic scale thickness of the 2D InSe.

A limit in ballistic ratio (i.e., transmittance) of 85% was reported in silicon FETs with L_G = 30–50 nm in 1999 [9], but some later reported silicon FETs with L_G = 10–70 nm show much lower ballistic ratios. In contrast, the room-temperature ballistic ratio of the 2D InSe FET with L_G = 10 nm reaches 83% (Figure 3(e) in [5]). The discrepancy in the ballistic ratio between the silicon and 2D materials is possibly attributed to the distinct surface conditions. The silicon FETs suffer from a large carrier scattering from the large surface roughness caused by lithography, while carrier scattering is suppressed in the 2D InSe FET due to the sig-

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nificant reduction in surface roughness and the absence of dangling bonds.

The device performance of the 2D FETs shows a trade-off with the channel thickness. Multiple layers may carry a higher current than a monolayer due to a larger density of states. However, the thicker channel simultaneously suffers from degraded electrostatic gate control. The on-state current of the 2D InSe FETs monotonically and slowly increases from 22 layers to 3 layers but suddenly decreases from 3 layers to a monolayer (Figure S8(d) in [5]). The on-state current of the fabricated ML InSe FET at a $V_{\rm DD}$ of 0.5 V is $\sim$ 0.1 mA/μm, which is only one-tenth that of the fabricated three-layer InSe FET and the simulated ML InSe FET [6]. The unexpectedly poor performance of the fabricated ML InSe FET is attributed to the direct Y doping on the ML InSe to form the electrode, where the strong covalent interaction between the metallic Y-InSe and semiconducting InSe in the lateral direction would result in a metal-induced gap state and thus a Schottky barrier [10]. A better scheme is to use bilayer InSe as electrodes and dope only the top layer so that an Ohmic contact can be established between doped and undoped InSe. Another cause of the observed poor performance is attributed to the structural instability of ML InSe.

The realization of ideal 2D InSe transistors in labs is a great academic breakthrough. In contrast to the mature CMOS technology based on silicon, substantial engineering challenges remain for applications of 2D FETs, such as controllable synthesis of high-quality wafer-scale 2D sheets, shrinkage of the contact lengths to below 20 nm, achievement of complementary *p*-type 2D FETs with comparable performance, and CMOS-compatible fabrication processes for 2D materials-based 3D structure transistors. From a theoretical perspective, the precise dependence of the figures of merit of the 2D InSe FETs on the layer number deserves investigation in the future.

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References

1 Chhowalla M, Jena D, Zhang H. Two-dimensional semiconductors for transistors. Nat Rev Mater, 2016, 1: 16052
2 Liu Y, Duan X, Shin H J, et al. Promises and prospects of two-dimensional transistors. Nature, 2021, 591: 43–53
3 Fiori G, Bonaccorso F, Iannaccone G, et al. Electronics based on two-dimensional materials. Nat Nanotech, 2014, 9: 768–779
4 Quhe R, Xu L, Liu S, et al. Sub-10 nm two-dimensional transistors: theory and experiment. Phys Rep, 2021, 938: 1–72
5 Jiang J, Xu L, Qiu C, et al. Ballistic two-dimensional InSe transistors. Nature, 2023, 616: 470–475
6 Wang Y, Fei R, Quhe R, et al. Many-body effect and device performance limit of monolayer InSe. ACS Appl Mater Interface, 2018, 10: 23344–23352
7 Auth C, Aliyarukunju A, Asoro M, et al. A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2017. 673–676
8 Convertino C, Zota C, Sant S, et al. InGaAs-on-insulator FinFETs with reduced off-current and record performance. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2018. 899–902
9 Timp G, Bude J, Bourdelle K K, et al. The ballistic nanotransistor. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 1999. 55–58
10 Wang Y, Liu S, Li Q, et al. Schottky barrier heights in two-dimensional field-effect transistors: from theory to experiment. Rep Prog Phys, 2021, 84: 056501