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A Ku-band image-rejection filtering LNA MMIC in 150-nm GaN-on-SiC technology

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The low noise amplifier (LNA) is one of the most important circuits in the transceiver. Many high-performance LNAs have been demonstrated based on GaN processes. For instance, by using a hybrid-matching topology with double-shunt capacitors to achieve broadband impedance matching, an LNA covering 25–31 GHz is designed for 5G new radio (NR) base station applications [1]. With the AlGaN/GaN-on-SiC 250-nm technology, a 12.8–14.8 GHz with a linear gain over 20 dB and a 14–18 GHz LNA with a noise figure (NF) of 2.4 dB at 16 GHz are designed in [2,3], respectively.

Apart from the LNA, the filter is also an essential component in transceivers. At the down conversion of a receiver, the filter can be used to reduce the interference at the image frequency band that will fold into the intermediate band. However, in Ku-/Ka-band frequencies, a front-end model (or LNA chip) is usually difficult to be integrated with an additional filter. To solve this problem, co-designs of filters and other front-end circuits such as power amplifiers, LNAs, and switches have been developed to realize multifunctional integrated circuits. In [4], three bandstop filters are integrated into three impedance matching networks of an LNA to design a CMOS filtering LNA. In [5], a mixed electric-magnetic coupling circuit is proposed to design a CMOS filtering LNA and filtering switch with compact sizes. Good out-of-band rejection can be achieved in the filtering LNAs in [4, 5]. However, the NF performance of LNAs in CMOS technology may be insufficient for some high-sensitivity applications. GaN LNAs with low NFs and filtering responses are useful in wireless applications.

In this study, a Ku-band filtering LNA is proposed in 150-nm GaN-on-SiC technology. The input matching network is designed to obtain low noise performance. To integrate the desired filtering response for image rejection, the inter-stage impedance matching network is realized using a highpass *L-C-L* network while the output matching network is designed with a transmission zero for enhancing the selectivity and out-of-band rejection level. Design theories and experimental results are presented.

Proposed filtering LNA schematic. The proposed filtering LNA is designed in a commercial 150-nm GaN-on-SiC technology. To obtain the desired gain of 20 dB, a three-stage topology is selected. Figure 1(a) shows the schematic of the proposed GaN filtering LNA. Three transistors are all used with the size of 2 × 50 μm. The drain supply voltage is set as V_d = 10 V. And the gate voltage is selected as V_g = −1.5 V. The LNA circuit consists of one input matching network, two inter-stage matching networks, and one output matching network. The input matching network is used to realize a low NF. The inter-stage matching network is designed into a π-shape highpass network. The gate bias and drain supply are connected to the shunted inductors for simplifying the circuit layout and reducing the chip area. The paralleled capacitor ($C_{\rm bp1}$) and the paralleled resistor ($R_{\rm bp2}$) with a capacitor ($C_{\rm bp2}$) are used as the bypass network for the voltage supply.

Filtering LNA design. For image-frequency band rejection, the inter-stage matching network of the proposed LNA is designed with a π-shape highpass filtering network consisting of two shunted inductors and one series capacitor (*L-C-L* π-shape network). In the LNA design, due to the parasitic capacitors at the gate and drain of the transistor, the input or output impedances of the transistor are usually capacitive. Thus, the source and load impedances for designing the *L-C-L* matching network (with the component values of L_{m1}, C_{m1}, L_{m2}) are capacitive, which can be transformed into the paralleled impedance using a resistor and a capacitor ($Z_S = R_S//C_S$, $Z_L = R_L//C_L$). Then, the desired values of L_{m1}, C_{m1}, and L_{m2} for the inter-stage matching network can be obtained by solving the following equations:

$$J = \omega_c C_{m1} = \frac{1}{\sqrt{R_S R_L}}, \tag{1}$$

$$\omega_c = \frac{1}{\sqrt{L_{m1}(C_{m1}+C_S)}} = \frac{1}{\sqrt{L_{m2}(C_{m1}+C_L)}}. \tag{2}$$

As for the output matching network, it is also designed with the highpass filtering response to improve the image rejection level, as shown in Figure 1(a). First, two *L-C-L* π-shape networks similar to the inter-stage matching network are cascaded to achieve the desired output impedance matching, which can be shown as *L-C-L-C-L* network after combing the two shunted inductors at the center. Here, the use of two cascaded π-shape highpass networks can reduce the impedance conversion ratios of each highpass network to achieve a wider impedance matching bandwidth. Then, a series *LC* circuit (L_z and C_z) is utilized to replace the shunted inductor at the center. In this way, a transmission zero can

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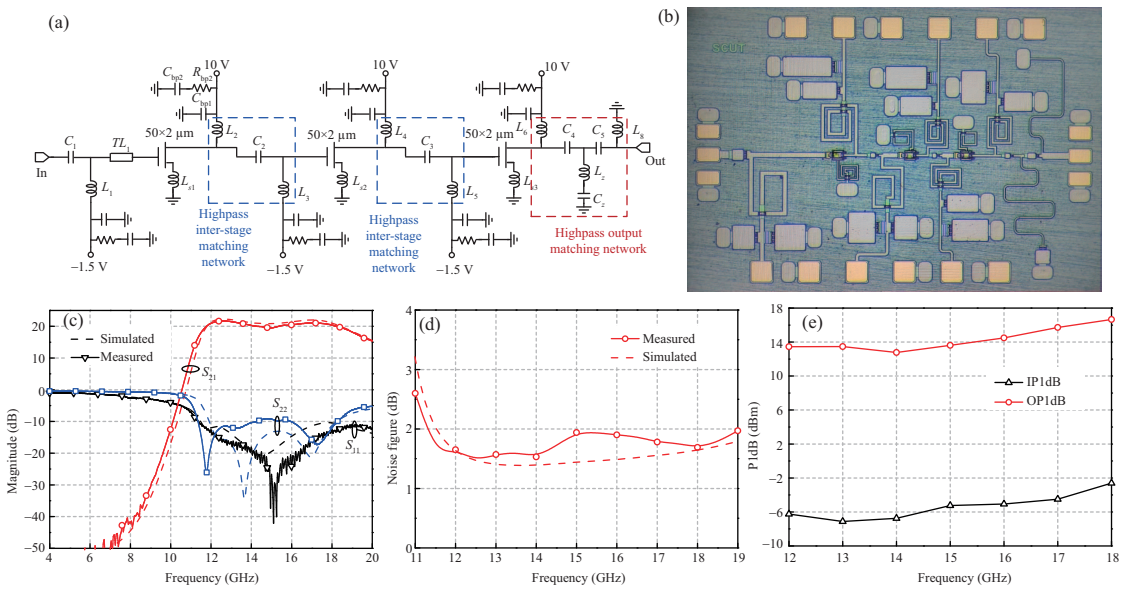

Figure 1 (Color online) (a) Schematic; (b) microphotograph of the filtering LNA chip; (c) simulated and measured S-parameters; (d) simulated and measured NFs; (e) measured IP1dB and OP1dB.

be generated. According to the above analyses, both the inter-stage matching network and output matching network of the LNA are designed with highpass responses, which can greatly improve the image-frequency rejection level.

Implementation. The proposed filtering LNA circuit is fabricated in 150-nm GaN-on-SiC technology. Figure 1(b) shows the microphotograph of the filtering LNA chip. The overall circuit area including the DC and RF pads is 1.65 mm × 1.15 mm, showing a compact size. The DC current is 53 mA, showing an overall DC power consumption of 530 mW. The small-signal S-parameter measurement is accomplished by on-wafer probing using Keysight PNA-X Network Analyzer N5244B. Figure 1(c) shows the simulated and measured S-parameters. Good agreement between them can be observed. The operating frequency band is measured as 12–18 GHz. The input and output return losses are better than 9.5 and 12 dB, respectively. The small signal gain is 20.6 ± 1.1 dB, showing good in-band flatness. The out-of-band rejection is higher than 34 dBc below 10 GHz and 64 dBc below 8 GHz, exhibiting good frequency selectivity and high image rejection level. The NF is measured using R&S FSW67 Signal & Spectrum Analyzer with a Noisecom NC346V 0.1–55 GHz noise source. Figure 1(d) shows the measured results, where the in-band NF is 1.5–1.9 dB. The linearity is measured using an R&S SMF 100A signal generator and the spectrum analyzer. The measured input and output 1-dB compression points (IP1dB and OP1dB) are from −7.1 to −2.6 dB and from 12.8 to 16.7 dB, respectively, as shown in Figure 1(e).

Conclusion. A three-stage Ku-band filtering LNA MMIC has been proposed using 150-nm GaN-on-SiC process in this paper. The design method has been detailed. *L-C-L* π-shape networks have been designed and used as inter-stage matching networks with highpass filtering responses. To further improve the frequency selectivity and out-of-band rejection level, the LNA output matching network has been designed with a transmission zero at the lower frequency band. Then, high out-of-band rejection for image suppression was obtained. For demonstration, the proposed filtering LNA has been implemented. The operating band was measured at 12–18 GHz with an NF of 1.5–1.9 dB and a gain of 20.6 ± 1.1 dB. High rejection levels of 34 dBc @10 GHz and 64 dBc @8 GHz have been achieved. The proposed design has been compared with previously published papers, showing good LNA performance with high image rejection.

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References

1 Ahn H B, Ji H G, Choi Y, et al. 25-31 GHz GaN-based LNA MMIC employing hybrid-matching topology for 5G base station applications. IEEE Microw Wireless Tech Lett, 2023, 33: 47–50
2 Resca D, Scappaviva F, Florian C, et al. A robust Ku-band low noise amplifier using an industrial 0.25-μm AlGaN/GaN on SiC process. In: Proceedings of European Microwave Conference, Nuremberg, 2013. 1467–1470
3 Guo F Q, Yao Z H. Design of a Ku-band AlGaN/GaN low noise amplifier. In: Proceedings of the 3rd Asia-Pacific Conference on Antennas and Propagation, Harbin, 2014. 1406–1408
4 Gao L, Rebeiz G M. A 24-43 GHz LNA with 3.1-3.7 dB noise figure and embedded 3-pole elliptic high-pass response for 5G applications in 22 nm FDSOI. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, 2019. 239–242
5 Li H Y, Xu J X, Gao L, et al. 24-35 GHz filtering LNA and filtering switch using compact mixed magnetic-electric coupling circuit in 28-nm bulk CMOS. IEEE Trans Circ Syst I, 2023, 70: 1071–1082