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Mobile-ionic FETs with ultra-scaled amorphous dielectric achieving ferroelectric behaviors and sub-kT/q swing with temperature down to 77 K

Huan LIU^{1,2}, Qiyu YANG², Chengji JIN¹, Jiajia CHEN¹, Lulu CHOU², Xiao YU^{1*}, Yan LIU^{2*} & Genquan HAN^{1,2}

¹Research Center for Intelligent Chips, Zhejiang Lab, Hangzhou 311121, China; ²School of Microelectronics, Xidian University, Xi'an 710071, China

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The steep subthreshold swing (SS) could be achieved in negative capacitance field-effect transistors (NCFET) to reduce power dissipation in modern electronics. Polycrystalline HfO₂-based ferroelectric materials have attracted great interest due to their better thickness scalability and CMOS process compatibility [1]. However, the undesired leakage current along the grain boundaries increases exponentially as the ferroelectric film thickness decreases, thus deteriorating SS characteristics. Additionally, the effect of NC on transistor SS was found to be negligible for HfZrO_x (HZO) thicknesses below 4 nm [2].

Besides the polycrystalline ferroelectric HfO_2 , the ferroelectric behavior also can be observed in devices with amorphous (a-) ZrO_2 dielectrics enabled by mobile-ionic related oxygen ions-vacancies, which shows advantages in the thermal budget, endurance, operation voltage, and scaling limits, and have been demonstrated for non-volatile memory and neuromorphic application [3]. It is natural to investigate the proposed ferroelectric characteristics with ultrascaled dielectric.

In this study, we have demonstrated mobile-ionic FETs (MIFETs) based on ultra-scaled (3.5 nm) amorphous ZrO_2 dielectric achieving sub-kT/q SS, which exhibits a stable ferroelectric-type hysteresis at the wide temperature range from room temperature to 77 K.

As shown in Figure 1(a), a-ZrO₂ MIFETs were fabricated using a conventional CMOS process, starting with an n-type Ge substrate. The source/drain region is formed by BF²⁺ implantation and dopant activation. After the pre-gate cleaning, the gate stack was formed by depositing ZrO₂ by atomic layer deposition, followed by the TaN gate deposition. After gate patterning and etching, highresolution transmission electron microscope (HRTEM) images of the fabricated metal-oxide-semiconductor (MOS) are shown in Figure 1(b). The a-ZrO₂ layers with a thickness of 3.5 nm have been confirmed from the images. Corresponding energy-dispersive X-ray spectroscopy (EDX) mapping of the MOS gate stack is also shown, indicating there was no contamination of other elements included in the dielectrics. Additionally, a sub-nm thick oxide layer at the interface between metal and ${\rm ZrO}_2$ will be generated due to oxygen diffusion.

As shown in Figure 1(c), the hysteresis loops of polarization (P) versus voltage (V) measured for the TaN/ZrO₂/Ge MOS capacitors with various frequencies exhibit ferroelectric-like behavior. It should be noted that the asymmetry of the P-V hysteresis curves of MOS can be attributable to the depletion of semiconductors. Such a strong frequency dependence of polarization should be attributable to the ion drift mechanisms. As the frequency increases, P-V hysteresis loops reduce because of its comparative large response time of mobile ions in a-ZrO₂ film.

Figure 1(d) shows the measured transfer curves of ZrO₂based MIFET at the drain voltage ($V_{\rm DS}$) of -0.05 V. The ferroelectric-type hysteresis can be observed in drain current (I_{DS}) . It can be noted that the device with a gate voltage $(V_{\rm GS})$ sweeping step of 0.05 V achieves the average forward SS (SS_{for}) and reverse SS (SS_{rev}) of 25 and 19 mV/decade for $I_{\rm DS}$ over 2 orders of magnitude, respectively. It is demonstrated that the surface potential amplification effect of the semiconductor is induced by ions movement in the amorphous dielectric. It is noted that ion mobility will affect the accumulation of mobile ions at the dielectric interface related to the surface potential of the channel. When $V_{\rm GS}$ sweeping step decreases to 0.01 V, which increases total measurement time, $\rm SS_{for}$ of 58 mV/decade and smaller ferroelectric-type hysteresis is achieved. The higher $I_{\rm DS}$ achieved with the smaller $V_{\rm GS}$ step results from having enough time for the response of mobile ions, which will decrease the hysteresis of I_{DS} - V_{GS} loops. Additionally, the charge trapping/detrapping effect with more slow traps that respond at the interface as the measurement time increases also reduces the ferroelectric type hysteresis and increases the SS. Figure 1(e) shows the corresponding point SS as a function of $I_{\rm DS}$. The device with a $V_{\rm GS}$ step of 0.01 V demonstrates the minimum steep $\mathrm{SS}_{\mathrm{for}}$ and $\mathrm{SS}_{\mathrm{rev}}$ of 18 and 21 mV/decade, respectively. Gate current $(I_{\rm G})$ is also measured and plotted in Figure 1(f). The ultralow leakage current can be achieved. It is noted that current peaks in $I_{\rm G}$ can be observed and will be inhibited in the



Figure 1 (Color online) (a) Key fabrication process flows and schematic of a-ZrO₂-based MIFET; (b) HRTEM images and the corresponding EDX mapping profiles of amorphous ZrO₂ films in TaN/ZrO₂/Ge MIFETs; (c) measured P-V curves of TaN/a-ZrO₂/Ge capacitors with various frequencies; (d) measured $I_{\rm DS}$ - $V_{\rm GS}$ curves at $V_{\rm DS} = -0.05$ V for a-ZrO₂ MIFETs with $V_{\rm GS}$ sweeping steps of 0.05 and 0.01 V; (e) the corresponding point SS vs. $I_{\rm DS}$ extracted from (d); measured (f) $I_{\rm G}$ - $V_{\rm GS}$ curves and (g) $I_{\rm DS}$ - $V_{\rm DS}$ curves for a-ZrO₂ based MIFET; (h) transfer curves of a-ZrO₂-based MIFET with $V_{\rm GS}$ step of 0.05 V at different temperatures; (i) temperature dependence of the $V_{\rm TH}$ and the hysteresis of MIFET and HZO FeFET; (j) SS_{min} as a function of temperature for MIFET and HZO NCFET.

subthreshold region of Fe-like FET, indicating that the displacement currents induced by the mobile ions will be suppressed due to the small depletion capacitance. A sudden drop of $I_{\rm G}$ with $V_{\rm GS}$ sweeping forwardly and reversely (AA' and BB') indicates the reduction of voltage across the ZrO_2 film, contributing to the amplification of the internal voltage and channel surface potential [1]. Figure 1(g) shows the output characteristics of a- ZrO_2 MIFET, and the obvious negative differential resistance (NDR) phenomenon is observed. The NDR phenomenon can be explained as follows. For the fixed gate bias— $V_{\rm GS}$, mobile ions in a-ZrO₂ are polarized down. As $|V_{\rm DS}|$ increases and finally $|V_{\rm DS}|$ is larger enough than $|V_{\rm GS}|$ to reverse the migration of mobile ions, the polarization is locally changed at the drain-side, resulting in a reduction of the charge density in the channel near the drain. Therefore, $I_{\rm DS}$ decreases and NDR happens.

To investigate the effects of temperature dependency on the characteristics of ZrO_2 MIFET, the temperature dependence of $I_{\rm DS}\text{-}\,V_{\rm GS}$ curves in a wide temperature ranging from 300 K down to 77 K has been measured. Figure 1(h) shows the $I_{\rm DS}\text{-}V_{\rm GS}$ curves at different temperatures with a $V_{\rm DS}$ of -0.05 V. The ferroelectric hysteresis and the steep SS are exhibited among all the temperatures. The temperature dependence of the corresponding threshold voltage $(V_{\rm TH})$ and the hysteresis is shown in Figure 1(i), compared with those of crystalline HZO FeFET [4]. Here, hysteresis is defined as the difference between $V_{\rm TH}$ ($V_{\rm GS}$ at $I_{\rm DS} = 10^{-8}$ A/µm) for forward and reverse sweeps. It is worth noting that hysteresis keeps stable for the a-ZrO₂ MIFET, while the HZO-based device is getting large since its coercive field is closer to the intrinsic value in cryogenic. This phenomenon indicates the total amounts of mobile ions remain stable until 77 K. Additionally, the minimum SS_{min} is independent of temperature

in cryogenic, as shown in Figure 1(j) [5].

Conclusion. In summary, ferroelectric behavior and steep SS have been demonstrated in MIFETs with ultra-scaled (3.5 nm) amorphous ZrO_2 dielectric. Amorphous ZrO_2 -based MIFET exhibits a stable ferroelectric-type hysteresis and steep SS with the decrease of the temperature until 77 K, indicating the potential utilization for cryogenic applications.

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