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Polarity tunable complementary logic circuits

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The utilization of excellent electrical characteristics of 2D semiconductors has led to a series of revolutionary developments in the research fields of neuromorphic circuits, reconfigurable circuits, and large-area thin-film electronics [1–4]. In order to further explore the potential of 2D materials in the development of electronic technology, it is necessary to explore the appropriate characteristics of 2D materials to improve the performance of ultra-low static power (ULSP) circuits. The ULSP circuit is of great significance for the realization of low-power chips, and has been implemented by using complementary transistors to construct complementary logic (CL) architecture. However, the conventional CL architecture is not suitable for 2D material electronics. Because 2D materials cannot achieve large-scale and highly uniform polarity (P- or N-type) regulation based on ion implantation technology, thus it is challenging to realize complementary device based on 2D materials [5]. A promising approach to solve this problem is to utilize the ambipolar characteristics of two-dimensional materials, which shows that the field effect characteristics can be dynamically adjusted between P- and N-type through the external electric field [4, 5]. By designing splitting-gate (SG) architecture, independently tuning the SG voltage polarity and engineering the local device polarity are allowed, and it can achieve diverse electrical transport characteristics beyond the single-gate device [4]. Therefore, it is highly desirable to explore novel circuit architecture to implement ULSP logic functions with fewer device resources by utilizing the diverse electrical characteristics of the SG ambipolar transistor.

Here, we propose a polarity tuneable complementary logic (PTCL) architecture and implement the corresponding logic circuits with the SG ambipolar transistors. We employ the WSe_2 as channel material to fabricate the SG ambipolar transistor and construct a three-input logic unit. We further show that the cascading diversity between the logic units allows for the implementation of arbitrary complex logic functions. Based on the proposed PTCL architecture, we construct a 1-bit multifunctional arithmetic and logic circuit and demonstrate that the logic density and logic depth of the designed circuit are enhanced by 133% and reduced by 50%, respectively, over the conventional CL architecture. The work may pave the way for designing energy-efficient logic circuits based on 2D semiconductors.

Result and discussion. The SG ambipolar transistor (see Figure 1(a)) with the diverse switching characteristics (see Figure S1) can be used to implement the PTCL circuit. By independently tuning the polarity of two SG voltages, as shown in Figure S1, the electrically tunable homojunction characteristics of the SG device are much more diverse than that of the conventional transistor with only P- or N-type field-effect switching characteristics. To implement Boolean logic by utilizing the diverse switching characteristics of the device, we analyze the Boolean logic relationship between the input operating voltage signals and the current output. For device M1(M2) (see Figure 1(b)), the input signals $A(C)$, B, and $C(A)$ are injected into the source and two gate electrodes respectively, and output signal $F_1(F_2)$ is sensed at the drain terminal. According to the homojunction conductive characteristics (see Appendix A), the dependence of the input voltage signal on current output can be transformed into the corresponding Boolean algebra of $F_1 = F_2 = A(\overline{B}+C) + \overline{AB}C = C(\overline{B}+A) + \overline{CB}A = 1$, $\overline{F_1} = \overline{F_2} = AB\overline{C} + \overline{A}(B+\overline{C}) = CB\overline{A} + \overline{C}(B+\overline{A}) = 0$. We conclude that the logical relationship between the input voltage signals (A, B, and C) and the output current signal (F_1 or F_2) is unchanged for the devices M1 and M2, despite exchanging input voltage signals A and C. Therefore, the logic unit circuit (LUC) can be designed by connecting two SG transistors in series (see Figures 1(c) and S2). The working mechanism and output characteristics of the LUC are shown in Figure S3. The measured static current flow through the LUC is within the range of pA (as shown in Figure S3(c)), thus ensuring ULSP and meeting the requirements of the CL circuits. In addition, the reliability of the proposed 2D PTCL circuits is better than conventional CL circuits due to the unique polarity-tunable characteristics of

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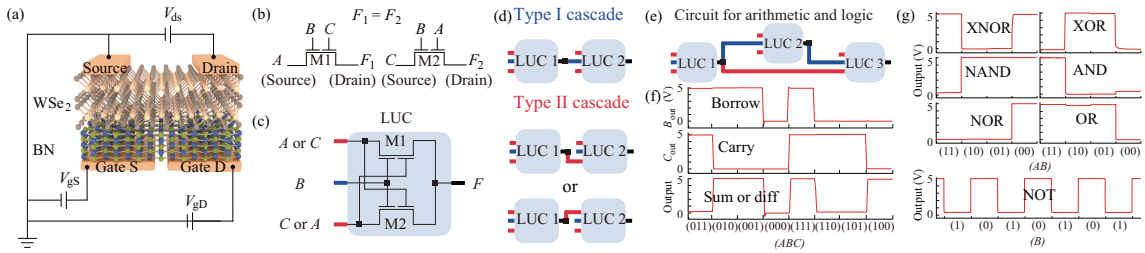

Figure 1 (Color online) (a) Schematic of the device. (b) The combinational logic switching characteristics of the device. The input signal is A, B, and C, and the output signal is F_1 and F_2. The logic function of device M1 is $F_1 = A(\overline{B}+C)+\overline{A}\overline{B}C = 1$ and $\overline{F_1} = AB\overline{C}+\overline{A}(B+\overline{C}) = 0$, the logic function of device M2 is $F_2 = C(\overline{B}+A)+\overline{C}BA = 1$ and $\overline{F_2} = CB\overline{A}+\overline{C}(B+\overline{A}) = 0$. (c) The diagram of the designed LUC. (d) The Types I and II cascade rules. (e) The hybrid cascading diagram based on 3 LUCs of multifunctional arithmetic and logic block. (f) The measured output voltages of 1-bit full adder and subtractor arithmetic functions. (g) The measured output voltages of XNOR, XOR, NAND, AND, NOR, OR, and NOT logic functions.

the SG transistor (see Figure S12).

In order to evaluate the advantages of the PTCL-based circuits, both logic depth and logic density are used as figures of merit (see Appendix C). Compared with the conventional CL circuit implementing the same logic function, the logic depth and the logic density of the LUC-based PTCL architecture are reduced by 80% and increased by 250%, respectively (see Figure S4).

The LUC can be used as building blocks to construct arbitrarily complex logic circuits based on different types of cascades between the LUCs. The LUC circuit can realize several basic logic functions, including NOT, AND, OR, and other functions (see Figure S5). According to the Boolean algebra (i.e., $F = AC + A\overline{B} + C\overline{B}$) for the LUC, exchanging the input signal A and C would not change the logic function of the circuit ($AC + A\overline{B} + C\overline{B} = CA + C\overline{B} + A\overline{B}$), resulting in two distinct types of cascades (as indicated by blue and red lines in Figure 1(d), respectively). Based on these two different types of LUC circuit cascading strategies, three types of topological structures of signal transmission pathways can be designed, which may provide flexibility to diversify the logic functions implemented with the PTCL architecture (see Figure S6).

To show the advantages of cascading the LUC, we design the multifunctional arithmetic and logic circuits in the 1-bit ALU based on the hybrid structure of the signal transmission pathway, which is the key computing unit of modern digital processors (see Figure 1(e)). The circuit can implement various logic functions by selecting different functional signals (see Figures 1(f), (g), and S7). The circuit shows a shallower logic depth and higher logic density than the conventional CL circuit (see Figure S8), which indicates that the input and output signal delay of the designed circuit can be shorted, and the dynamic power consumption during logic flip can be reduced.

Conclusion. We propose a PTCL design rule for implementing arbitrarily complex logic functions. The LUC is realized by connecting two SG ambipolar transistors in series. Based on the distinct cascading type of the LUC, we construct the key computing unit of modern digital processors with a shallower logic depth and higher logic density than conventional CL circuits. The logic design demonstrated in this work may offer a new and convenient approach for realizing fast and energy-efficient CL circuits based on 2D materials.

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Supporting information Appendixes A–L. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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