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• **Supplementary File** •

Polarity tunable complementary logic circuits

Chen Pan[1], Jingwen Shi[2], Pengfei Wang[2], Shuang Wang[2], Cong Wang[2], Bin Cheng[1], Shi-Jun Liang[2*] & Feng Miao[2*]

[1]*Institute of Interdisciplinary Physical Sciences, School of Science, Nanjing University of Science and Technology, Nanjing* 210094*, China;*
[2]*Institute of Brain-Inspired Intelligence, National Laboratory of Solid State Microstructures, School of Physics, Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing* 210093*, China*

Appendix A The combinational logic switching characteristics of the device

For device M1 (see the top of Figure 1(b)), the input signals A, B, and C are injected into the source and two gate electrodes respectively, and output signal F_1 is sensed at the drain terminal. Forward biasing of PN, PP and NN junctions allows for transmitting a high-level signal ($A = 1$) from the source terminal to the drain terminal of device M1. In this way, the dependence of the input voltage signal on current output can be transformed into corresponding Boolean algebra of $A(\overline{B}+C) = 1$. Reverse biasing of the NP junction enables the prevention of a low-level signal ($\overline{A} = 0$) at the source terminal from being transmitted to the drain terminal of device M1. This corresponds to a Boolean algebra of $\overline{A}\ \overline{B}C = 1$. A similar Boolean algebra of $F_2 = C(\overline{B}+A)+\overline{C}\ \overline{B}A = 1$ can be obtained for the output signal of high level in the device M2, where the input signal terminals C and A are exchanged (see the bottom of Figure 1(b)). With the use of a similar analysis, the Boolean algebra of $\overline{F_1} = \overline{F_2} = AB\overline{C}+\overline{A}(B+\overline{C}) = CB\overline{A}+\overline{C}(B+\overline{A}) = 0$ can be obtained for the output signal of low level in the devices M1 and M2.

Appendix B The working mechanism and output characteristics of the LUC

We design the PTCL circuit by connecting two splitting-gate transistors in series, in which both devices M1 and M2 are represented by electrical switch symbols (see Supplementary Figure S3(a)). According to Boolean algebra of $F = F_1 = F_2 = AC(B + \overline{B}) + A\overline{C}\ \overline{B} + \overline{A}C\overline{B} = 1$ and $\overline{F} = \overline{F_1} = \overline{F_2} = A\overline{C}B + \overline{A}CB + \overline{A}\ \overline{C}(B + \overline{B}) = 0$, the operating mechanism of the PTCL circuit can be divided into six distinct scenarios for output of high-level signal ((i), (ii), (iii) in Supplementary Figure S3(a)) and output of low-level signal ((iv), (v), (vi) in Supplementary Figure S3(a)), respectively. When both input signals A and C are at high level (*i.e.*, $A = C = 1$), no current flows through M1 and M2 regardless of input signal B. In this case, both device M1 and M2 are turned on and a high-level output signal (*i.e.*, $F = 1$) is generated (see (i) in Supplementary Figure S3(a)). When input signal A is at high level (*i.e.*, $A = 1$) and input signal B and C are at low level (*i.e.*, $\overline{B} = \overline{C} = 0$), the device M1 is turned on and the device M2 is turned off. Consequently, current flowing in the circuit is blocked and a high-level signal (*i.e.*, $F = 1$) can be output through the device M1 (see (ii) in Supplementary Figure S3(a)). Exchanging input signal A and C (*i.e.*, $\overline{A} = 0$ and $C = 1$) and keeping input signal B at low level (*i.e.*, $\overline{B} = 0$) lead to switching off device M1 but turning on device M2. Thus, the current flow in the circuit is prevented and a high-level output signal (*i.e.*, $F = 1$) is obtained (see (iii) in Figure S3(a)). Similarly, (iv), (v), (vi) in the Supplementary Figure S3(a) show the analysis for the working mechanism of the circuit generating low-level output signals ($\overline{F} = 0$). It is worth pointing out that the current flow through the circuit is suppressed in all these cases, which is consistent with the essential characteristics of the complementary logic circuit. Based on the above detailed analysis of the working mechanisms, we design a logic unit circuit (LUC) by connecting two splitting-gate transistors in series, with the corresponding circuit shown in Supplementary Figure S3(b). To verify whether the operating mechanism of the LUC is consistent with the above analysis, we measured the output voltages of the circuit (red curve) and present the experimental data in Supplementary Figure S3(c). A typical square-wave output signal is observed and the high-level ($\sim$ 5 V) and low-level ($\sim$ 0 V) logic states are well separated. In addition, we also characterized the power consumption of the designed PTCL circuit by monitoring the current flowing through the circuit during operation, as indicated by blue points in Supplementary Figure S3(c). In each stable logic state, the current is on the order of picoamperes, which indicates that the LUC based on the PTCL architecture has low static power consumption and meets the basic requirements of CL technology.

Appendix C The definition of logic depth and logic density

The logic depth, which indicates input and output delay characteristics of the circuit in performing logic operations, is defined as the number of logic gates connected in series between input and output ports in the circuit. The shallow logic depth leads to less delay in performing the same logic function. The logic density can be manifested in the number of gate electrodes in the circuit (logic density=$1/N_{gates}$, where N_{gates} is the number of gate electrodes). A smaller number of gate electrodes in the circuit indicates that less dynamic power is consumed during the logic state transition.

* Corresponding author (email: sjliang@nju.edu.cn., miao@nju.edu.cn.)

Appendix D The CMOS circuit of implementing the function of LUC

To implement the function of LUC ($F = AC + \overline{AB} + \overline{CB}$), 14 complementary metal-oxide-semiconductor (CMOS) devices are used, with the corresponding circuit diagram shown in Supplementary Figure S4(a). Based on the definition given in the Supplementary Appendix B, the logic density of the LUC based on the CMOS device is $\frac{1}{14}$. Compared with the LUC circuit based on the CMOS device, the logic density ($\frac{1}{4}$) of LUC based on the PTCL architecture is increased by ($\frac{1/4}{1/14} - 1$) = 250%. Supplementary Figure S4(b) displays the gate-level diagram of the CMOS circuit that requires 5 logic gates connected in series between input and output ports. The logic depth of the CMOS circuit is 5. Compared to the conventional CMOS circuit solutions, the logic depth of the LUC based on the PTCL architecture is reduced by $(1 - \frac{1}{5}) = 80\%$.

Appendix E The reconfigurable functions of LUC

The LUC can implement the three-input logic functions ($F = V_{\mathrm{in1}}V_{\mathrm{in3}} + V_{\mathrm{in1}}\overline{V_{\mathrm{in2}}} + V_{\mathrm{in3}}\overline{V_{\mathrm{in2}}}$), which can be configurable by varying input signals, as shown in Supplementary Figure S5. The implemented logic functions include the AND, OR, and NOT, which constitutes the functionally complete set of constructing arbitrarily complicated logic functions. To implement "AND" logic function, V_{in2} is set to high-level ($V_{\mathrm{in2}} = 1$), and input signals V_{in1} and V_{in3} are applied to terminals A and B respectively. The logic output of the circuit can be described by the Boolean algebra $F = V_{\mathrm{in1}}V_{\mathrm{in3}} + V_{\mathrm{in1}}\overline{V_{\mathrm{in2}}} + V_{\mathrm{in3}}\overline{V_{\mathrm{in2}}} = AB$. When V_{in2} is set to low level (V_{in2}=0), the "OR" logic function can be obtained, with the Boolean algebra $F = V_{\mathrm{in1}}V_{\mathrm{in3}} + V_{\mathrm{in1}}\overline{V_{\mathrm{in2}}} + V_{\mathrm{in3}}\overline{V_{\mathrm{in2}}} = A + C$. To realize "NOT" logic function, signal V_{in2} is input to the terminal A, and V_{in1} and V_{in3} are set to opposite levels, with the Boolean algebra given by $F = V_{\mathrm{in1}}V_{\mathrm{in3}} + V_{\mathrm{in1}}\overline{V_{\mathrm{in2}}} + V_{\mathrm{in3}}\overline{V_{\mathrm{in2}}} = \overline{A}$. In addition to these three fundamental logic functions, other logic functions are shown in Supplementary Figure S5(b).

Appendix F Cascading LUCs to construct complex logic functions

Supplementary Figure S6(a) shows the chain-like structure comprised of LUC 1, LUC 2, and LUC 3 connected in series. In this structure, four different cascading schemes are present, as indicated by the distinct configurations of blue and red arrows. When the input signals are simultaneously fed into LUC 1 and LUC 2, and the output signals of LUC 1 and LUC 2 are used as parallel input to LUC 3, a tree-like structure of the signal transmission pathway can be generated, corresponding to the scheme in Supplementary Figure S6(b). Combining the chain- and tree-like structure gives rise to the hybrid structure including 6 different cascade schemes, as demonstrated in Supplementary Figure S6(c). By using the three topological structures of the signal transmission pathway and the two distinct cascading rules, it is achievable to construct PTCL circuits of arbitrary complex logic functions.

Appendix G The CMOS circuit of implementing the logic function of 1-bit full adder

To realize the 1-bit full adder, 28 conventional CMOS devices (see Supplementary Figure S8(a)) are used, indicating the corresponding logic density is $\frac{1}{28}$. Supplementary Figure S8(b) displays the gate-level diagram of the CMOS circuit and the logic depth is 6. Compared to the CMOS circuit, the logic density of the LUC circuit based on the PTCL architecture is enhanced by ($\frac{1/12}{1/28} - 1$) = 133% and the logic depth is reduced by $(1 - \frac{3}{6}) = 50\%$.

Appendix H The inverter and follower based on LUCs

The inverter is the most fundamental circuit for complementary logic technology. It can not only realize "NOT" logic operations but also be used to restore signals and improve the circuit's noise tolerance due to its high noise margin. Supplementary Figure S9(a) and (b) demonstrates the voltage transfer curve of the logic inverter based on splitting-gate ambipolar transistors at different V_{dd} and the corresponding Gain (Gain = dV_{in}/dV_{out}). Supplementary Figure S9(c) demonstrates the voltage transfer curve of the logic inverter based on splitting-gate ambipolar transistors at V_{dd} = 5 V, the corresponding circuit diagram (same as LUC) is shown in the inset of the figure. The noise margin (NM) of the measured inverter is 79 %, which can be further improved by contact engineering of the transistor. The basic operating speed of the circuit is characterized by the dynamic response of the inverter, with results shown in Supplementary Figure S9(d). The operating frequency of the inverter can reach 100 kHz, which can be further increased by mitigating the parasitic capacitance in the measurement system. [1] Two inverters can be cascaded to form a follower (see Supplementary Figure S9(e)), which can be used as a buffer stage. The follower has an ultra-high noise margin ($\sim$ 99%, see Supplementary Figure S9(f)) and allows for higher quality restoration of circuit signals.

Appendix I The reconfigurable 2-input logic circuit based on type-I cascade rule

The reconfigurable 2-input logic circuit ($Output = S(\overline{AB}) + \overline{S}(\overline{A+B})$) is implemented based on 2 LUCs with type-I cascade rule (see Supplementary Figure S10(a)), the corresponding circuit diagram and configuration schemes for achieving NAND and NOR Boolean functions are shown in Supplementary Figure S10(c) and (d), respectively. The input signals A and B are input from the V_1 and V_3, and the functions selection signal S is input from V_2. V_4 and V_5 in LUC 2 are fixed to the opposite level signal. The LUC 1 implements the AND or OR logic functions under the control of S and the LUC 2 realizes the NOT logic function (the output of LUC 1), thereby achieving the NAND or OR logic functions (see Supplementary Figure S10(d)). In contrast, the same function shown in Supplementary Figure S10(c) can be realized by using 14 conventional CMOS devices (see Supplementary Figure S10(e)), indicating that the corresponding logic density is $\frac{1}{14}$. Supplementary Figure S10(f) displays the gate-level diagram of the CMOS circuit with the logic depth equal to 2. Hence, compared to the corresponding CMOS circuit, the logic density of the LUC circuit based on the PTCL architecture is enhanced by ($\frac{1/8}{1/14} - 1$) = 75% for the same logic depth.

Appendix J Reconfigurable 3-input logic circuit based on type-II cascade rule

The reconfigurable 3-input logic circuit ($Output = S_1S_2(A+B+C) + S_1\overline{S_2}(A+B)C + \overline{S_1}S_2(AB+C) + \overline{S_1}\ \overline{S_2}ABC$) is implemented based on 2 LUCs with type-II cascade rule (see Supplementary Figure S11(a)), the corresponding circuit diagram and configuration schemes for achieving AND, AND-OR, OR-AND, and NOR Boolean functions are shown in Supplementary Figure S11(b) and (c), respectively. The input signals A and B are input from the V_1 and V_3, and the functions selection signal S_1 is input from V_2. The V_4 and V_5 of LUC 2 are applied to the terminal C and functions selection signal terminal S_2, respectively. When S_1 is fixed to

a high-level (or low-level), the cell 1 outputs $F_1 = AB$ (or $F_1 = A + B$). When S_2 is fixed to a high-level (or low-level), the cell 2 outputs $F_2 = F_1C$ (or $F_2 = F_1 + C$). Hence, by setting the function selection signal (S_1, S_2) to (1,1), (1,0), (0,1) and (0,0), respectively, the 3-input logic functions AND, AND-OR, OR-AND, and NOR can be realized (see Supplementary Figure S11(d)). Note that the same function shown in Supplementary Figure S11(c) can be realized by consuming 42 conventional CMOS devices (see Supplementary Figure S11(e), indicating the corresponding logic density is $\frac{1}{42}$. Supplementary Figure S11(f) displays the gate-level diagram of the CMOS circuit and the logic depth is 4. Hence, compared to the corresponding CMOS circuit, the logic density of the LUC circuit based on PTCL architecture is enhanced by $(\frac{1/8}{1/42} - 1) = 425\%$ and the corresponding logic depth is reduced by $(1 - \frac{2}{4}) = 50\%$.

Appendix K The reliability of the PTCL technology

According to the measurement result, although the electrical performance of LUC is not well uniform due to the limitations of the fabrication process, it does not affect the realization of the logic function of the circuit. In Supplementary Figure S12(a), the voltage transfer curves of logic inverters show obvious difference, but these three LUCs can achieve ideal logic functions, as shown in Supplementary Figure S12(b). The measured output voltages exhibit a typical square-wave output signal, and the high-level ($\sim$ 5 V) and low-level ($\sim$ 0 V) logic states are well separated, and three complete logical cycles are realized repeatedly. Furthermore, according to the analysis of the working mechanism of LUC (see Supplementary Figure S3), the non-uniformity of inverter characteristics only affects four logic states, as shown in the light blue area of Supplementary Figure S12(b). The other four logic states are stable, because the input signal is equal to logic "1" (or "0"), so each node of the LUC has the same potential, ensuring that the output signal is stable to "1" (or "0"). Compared with the conventional CL technology, all output logic states are affected by inverter characteristics (ref [2]), and the proposed PTCL technology has better reliability.

Appendix L Supplementary Figure

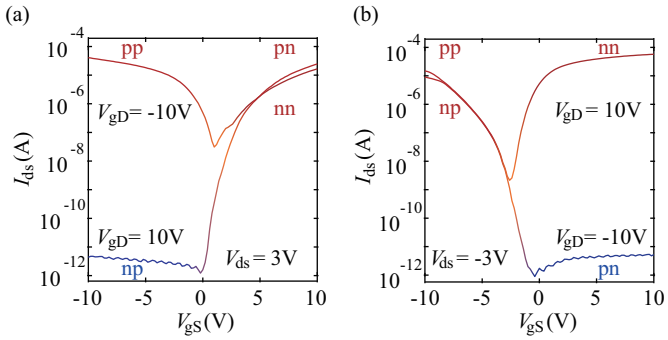


Figure S1 The electrical switching characteristics of the device for V_{ds} = 3 V and -3 V, respectively.

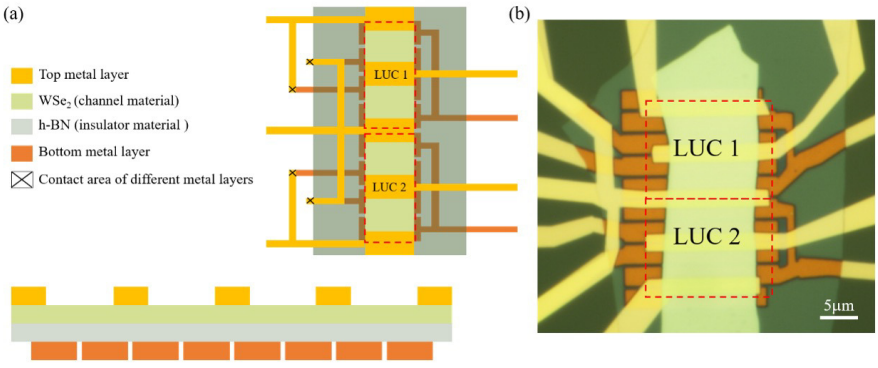


Figure S2 (a) Top view (top right) and side view (bottom) of two serial logic unit circuits. (b) Optical image of the circuit in figure (a) fabricated on Al_2O_3 substrate.

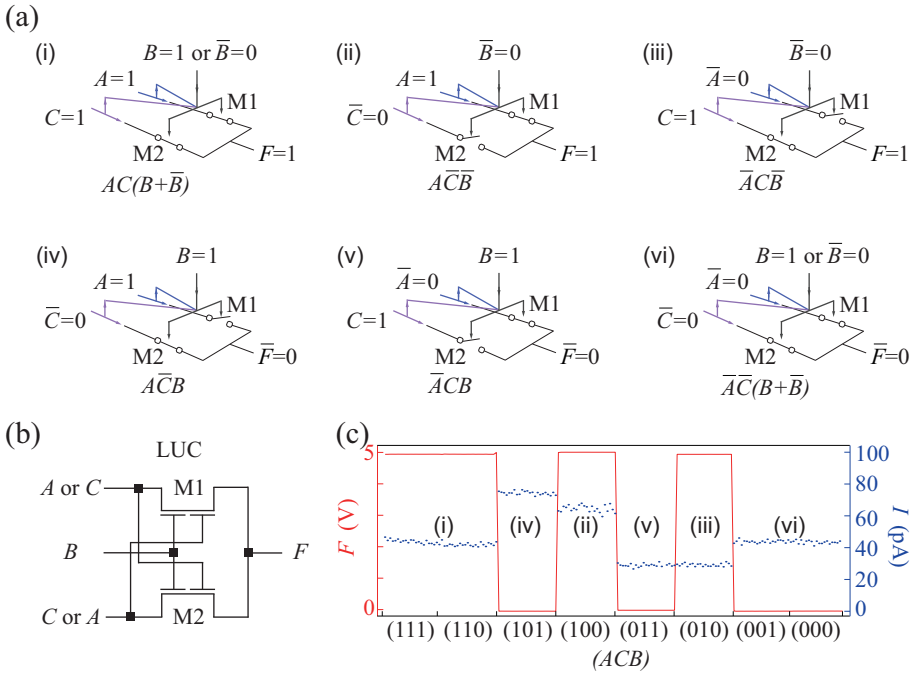


Figure S3 The construction of the LUC. (a) Analysis of the operating mechanism of the LUC, the Boolean logic output of the LUC is described by $F = AC(B + \overline{B}) + A\overline{C}\ \overline{B} + \overline{A}C\overline{B} = 1$ and $\overline{F} = A\overline{C}B + \overline{A}CB + \overline{A}\ \overline{C}(B + \overline{B}) = 0$. (b) The diagram of the designed LUC. (c) The measured output voltages of the LUC, and the logic states indicated by (i)-(vi) correspond to the diagrams shown in (a). The blue points represent the measured current at each stable logic state.

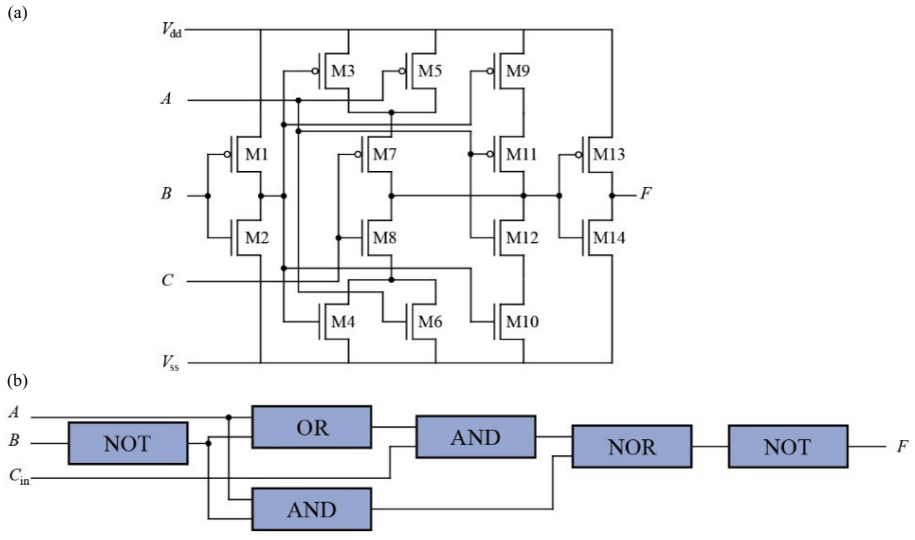
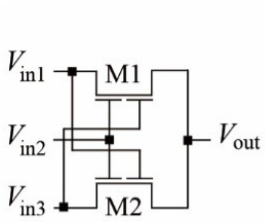


Figure S4 (a) The 14 CMOS devices are consumed to construct a circuit that implements the LUC function ($F = AC(B + \overline{B}) + A\overline{C}B + \overline{A}C\overline{B} = 1$)) as shown in the main text. (b) The gate-level diagram of the circuit in figure (a) shows that the logic depth is 5. (The circuit diagram is adapted from the ref [2])

(a)



(b)

V_{in1}	V_{in2}	V_{in3}	V_{out}	Functions
A	1	B	AB	AND
A	0	B	$A+B$	OR
1 (or 0)	A	0 (or 1)	$\overline{A}$	NOT
1 (or 0)	1 (or 0)	A	A	Follower
1	0	A	1	Truth
0	1	A	0	False
A	B	1	$A+\overline{B}$	IMP
A	B	0	$A\overline{B}$	NIMP
A	B	C	$AC+A\overline{B}+C\overline{B}$	Borrow out

Figure S5 (a) The diagram of the logic unit circuit. (b) Configuration schemes for achieving different logic functions.

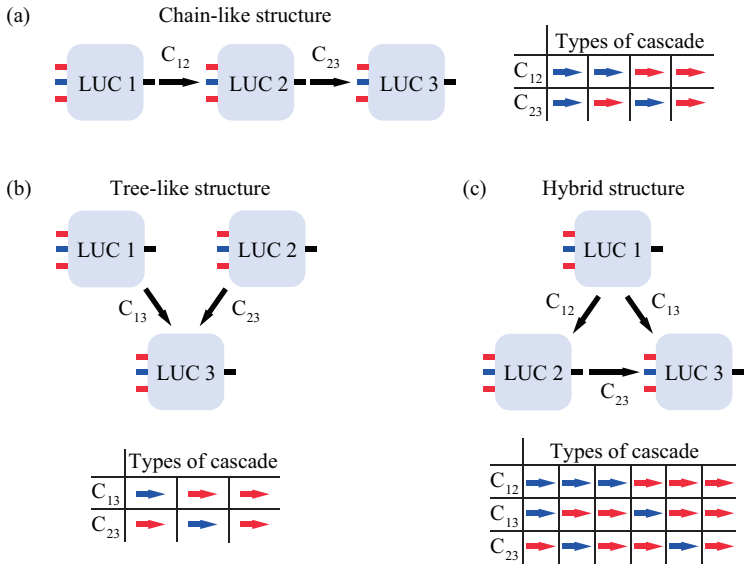
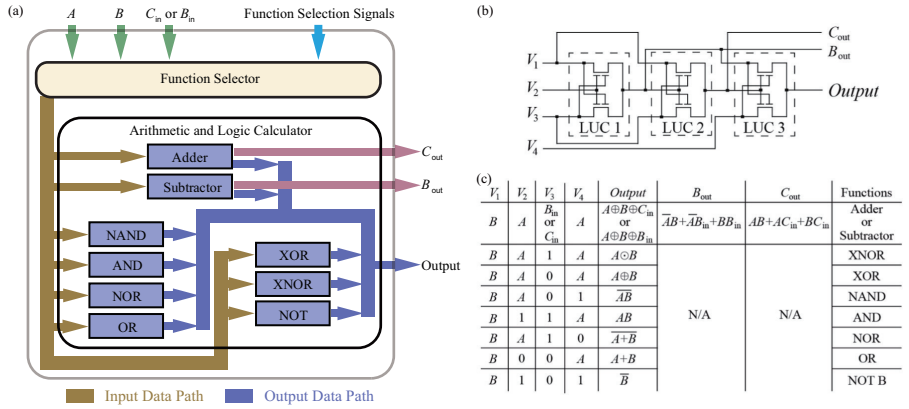


Figure S6 Cascading LUCs to construct complex logic functions. (a) Left: the diagram of the chain-like structure of signal transmission pathway; Right: Cascade schemes of 3 LUCs in the chain-like structure circuit. The C_{12} represents the cascade between the LUC 1 and the LUC 2. (b) Top: the diagram of the tree-like structure of signal transmission pathway; Bottom: Cascade schemes of 3 LUCs in the tree-like structure circuit. (c) Top: the diagram of the hybrid structure of signal transmission pathway; Bottom: Cascade schemes of 3 LUCs in the hybrid structure circuit.



V_1	V_2	V_3	V_4	Output	B_{out}	C_{out}	Functions
B	A	B_{in} or C_{in}	A	$A\oplus B\oplus C_{in}$ or $A\oplus B\oplus B_{in}$	$\overline{A}B+\overline{A}B_{in}+BB_{in}$	$AB+AC_{in}+BC_{in}$	Adder or Subtractor
B	A	1	A	$A\odot B$			XNOR
B	A	0	A	$A\oplus B$			XOR
B	A	0	1	$\overline{AB}$			NAND
B	1	1	A	AB	N/A	N/A	AND
B	A	1	0	$\overline{A+B}$			NOR
B	0	0	A	$A+B$			OR
B	1	0	1	$\overline{B}$			NOT B

Figure S7 (a) The function diagram of multifunctional arithmetic and logic block. (b)The diagram of the multifunctional arithmetic and logic circuit. (c) Configuration schemes for achieving different logic functions.

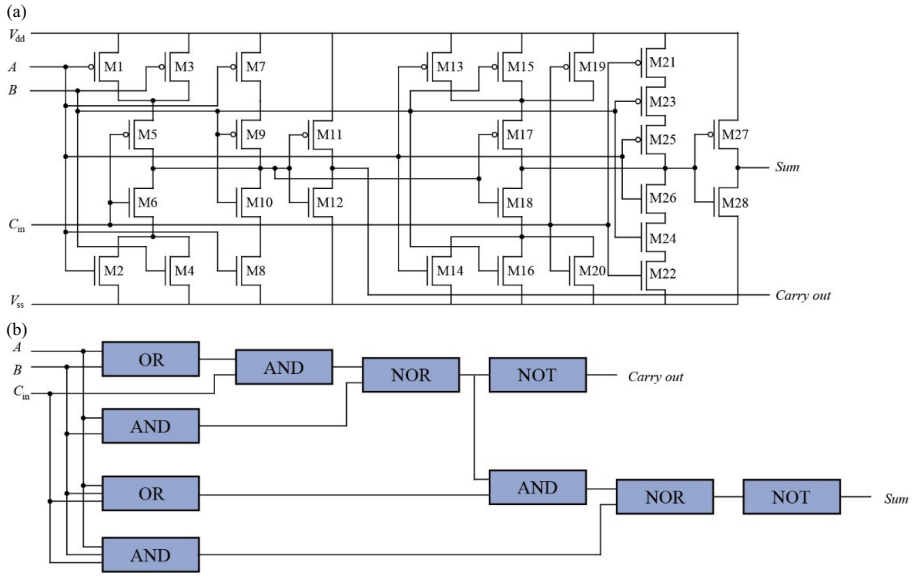


Figure S8 (a) Circuit diagram of 1-bit full adder logic function based on the hybrid cascade scheme of three LUCs ($C_{\rm out} = BC + BA + CA$ and $Sum = A \bigoplus B \bigoplus C$). (b) The gate-level diagram of the circuit in figure (a) shows that the logic depth is 6. (The circuit diagram is adapted from the ref [2])

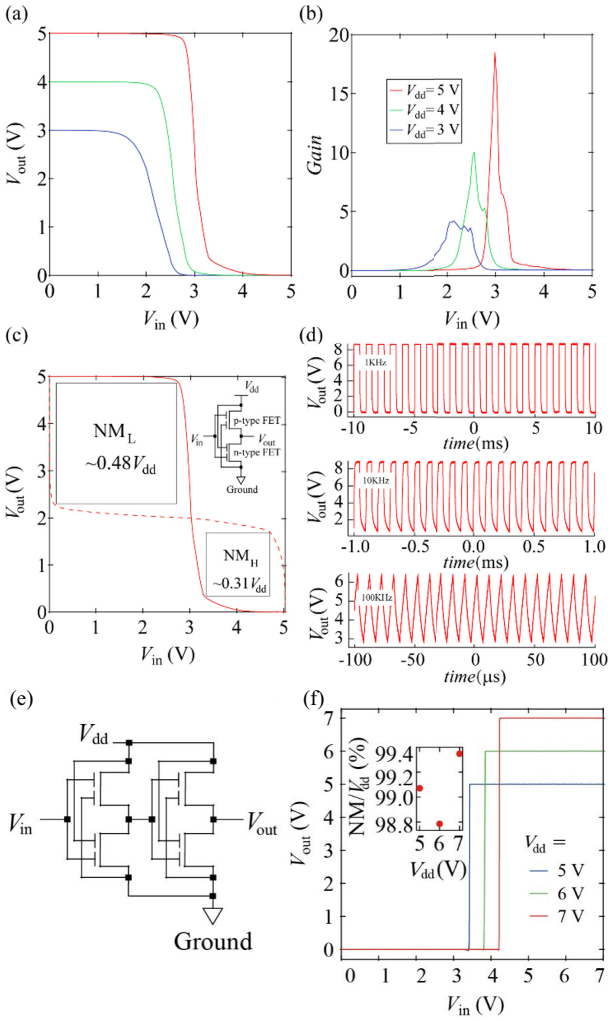


Figure S9 (a) The voltage transfer curves of the logic inverter based on the splitting-gate transistor with different V_{dd}. (b) The Gain of the invertor corresponding to (a). (c) The voltage transfer curve (solid line) and its mirror curve (dash line) of the logic inverter based on the splitting-gate transistor at V_{dd} = 5 V. The insert shows the corresponding circuit diagram. (d) The measured dynamic response (1 kHz, 10 kHz, and 100 kHz) of the inverter. (e) The circuit diagram of the logic follower based on 4 splitting-gate transistors. (f) The voltage transfer curves of the logic follower for V_{dd} = 5 V, 6 V and 7 V. The insert shows the noise margin of the logic follower.

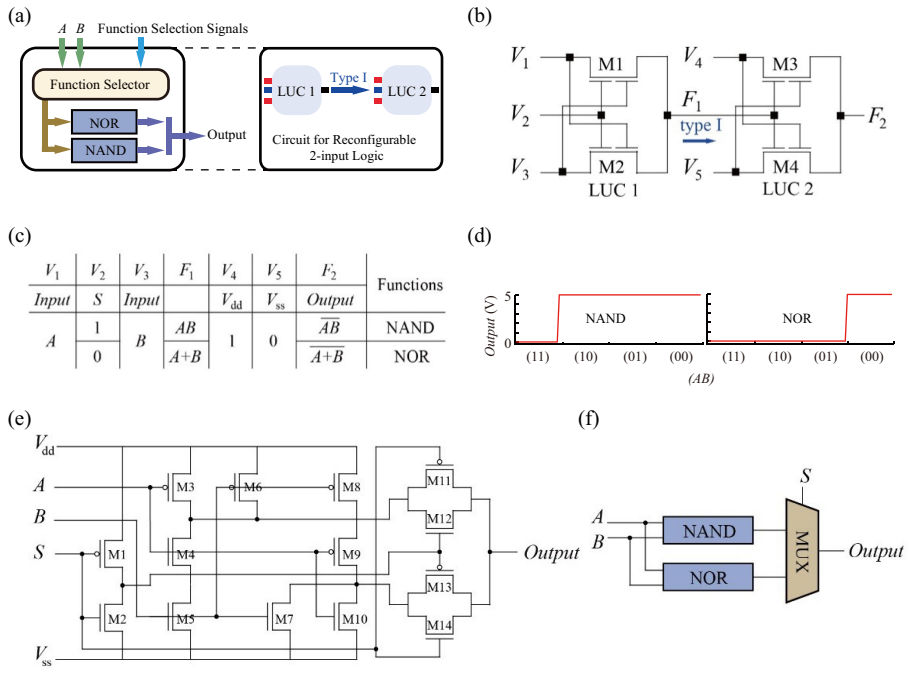
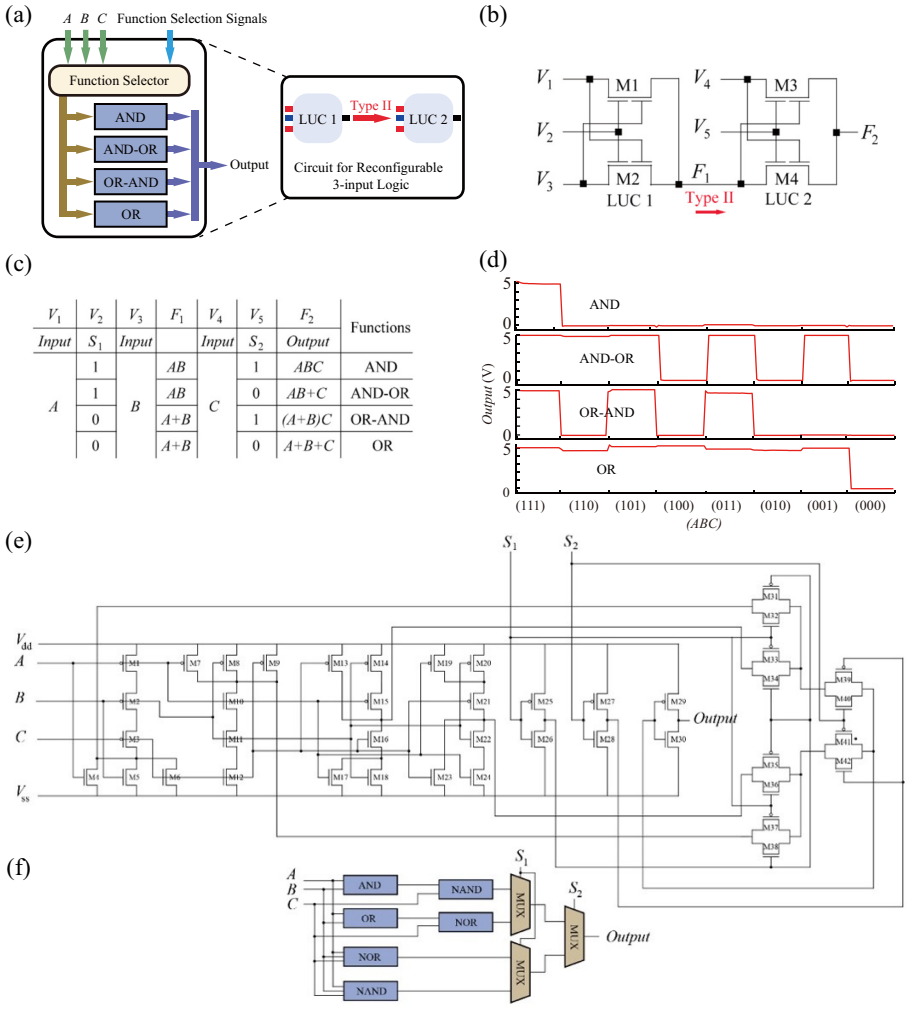


Figure S10 (a) The function diagram of a reconfigurable 2-input logic block for calculation function. (b) Reconfigurable 2-input logic circuit based on two LUCs with type-I cascade rule. (c) The corresponding configuration schemes for achieving NAND and NOR Boolean functions based on the circuit shown in (a). (d) The measured output voltages of 2-input NAND and NOR logic functions. (e) 2-input reconfigurable logic function ($Output = S(\overline{AB}) + \overline{S}(\overline{A+B})$), which can be implemented with 14 CMOS devices. (f) The gate-level diagram of the circuit in figure (e) shows that the logic depth is 2. (The circuit diagram is adapted from the ref [2])



V_1	V_2	V_3	F_1	V_4	V_5	F_2	Functions
Input	S_1	*Input*		*Input*	S_2	*Output*	
	1		*AB*		1	*ABC*	AND
A	1	*B*	*AB*	*C*	0	*AB+C*	AND-OR
	0		*A+B*		1	*(A+B)C*	OR-AND
	0		*A+B*		0	*A+B+C*	OR

Figure S11 (a) The function diagram of a reconfigurable 3-input logic block for calculation function. (b) Reconfigurable 3-input logic circuit based on two LUCs with type-II cascade rule. (c) The corresponding configuration schemes for achieving AND, AND-OR, OR-AND, and NOR Boolean functions based on the circuit shown in (a). (d) The measured output voltages of 3-input AND, AND-OR, OR-AND, and OR logic functions. (e) Circuit diagram of 3-input reconfigurable logic function described by $Output = S_1S_2(A+B+C) + S_1\overline{S_2}(A+B)C + \overline{S_1}S_2(AB+C) + \overline{S_1}\,\overline{S_2}ABC$, which can be realized by consuming 42 CMOS devices. (f) The gate-level diagram of the circuit in figure (e) shows that the logic depth is 4. (The circuit diagram is adapted from the ref [2])

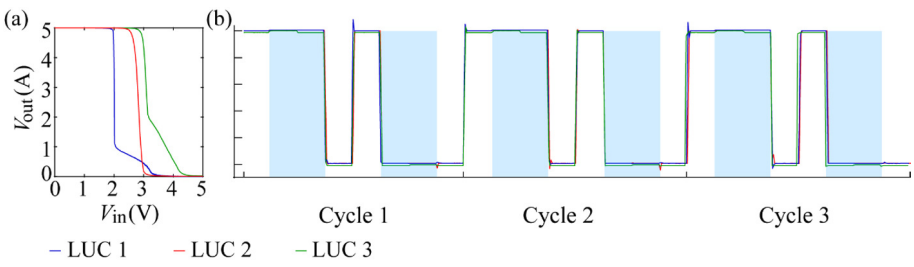


Figure S12 (a) The voltage transfer curves of logic inverters of the three different LUCs. (b) The measured output voltages (3 complete logical cycles) of three different LUCs corresponding to (a). The light blue area represents the logic state determined by the inverter characteristics.

References

1 Pan, C., Wang, C., Liang, S., Wang, Y., Cao, T., Wang, P., Wang, C., Wang, S., Cheng, B., Gao, A., Liu, E., Watanabe, K., Taniguchi, T., Miao, F. Reconfigurable Logic and Neuromorphic Circuits Based on Electrically Tunable Two-Dimensional Homojunctions. Nat. Electron. 2020, 3(7): 383-390

2 Kang, S., Leblebici, Y. CMOS digital integrated circuits. (Tata McGraw-Hill Education, 2003).