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All-van der Waals stacking ferroelectric field-effect transistor based on In_2Se_3 for high-density memory

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Abstract High-density integration of ferroelectric field-effect transistors (FeFETs) is hindered by factors such as interfacial states, short-channel effects, and ferroelectricity degradation in ultrathin films. Accordingly, the introduction of two-dimensional (2D) materials could effectively solve these problems. However, most current studies focus on the replacement of Si-based channels with 2D channels. Little progress has been made in addressing issues caused by bulk-phase ferroelectric gate layers, such as the unavoidable rough interfaces and the fading of ferroelectricity in ultrathin films. Herein, the 2D ferroelectric material In_2Se_3 is introduced as the gate dielectric. Combined with 2D insulating h-BN and 2D channel MoS_2, an all-van der Waals (vdW) stacking FeFET is fabricated to provide a straight solution for the abovementioned issues. First, the robust ferroelectric phase of In_2Se_3 is verified in an ultrathin film case and a high-temperature case, which is outstanding among recently reported 2D ferroelectrics. Second, device-level out-of-plane ferroelectric polarization switching is achieved in the cross-structure device. Based on these results, In_2Se_3 is adopted as the ferroelectric gate dielectric to fabricate all-vdW stacking FeFETs. The subsequent transistor performance measurement on the fabricated FeFETs indicates that the ferroelectric polarization of the In_2Se_3 layer plays a dominating role in forming a counterclockwise hysteresis loop. Further pulse response measurements manifest the feasibility of nonvolatile channel conductance tuning of these devices with a proper pulse design. Our findings suggest that In_2Se_3 is a suitable 2D ferroelectric gate material and that all-vdW stacking FeFETs based on 2D ferroelectrics are promising in the application of high-density memory.

Keywords high-density memory, ferroelectric field-effect transistors, two-dimensional ferroelectrics, van der Waals, In_2Se_3

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1 Introduction

The past few years have witnessed a drastic increase in data volume, and we are entering the era of big data and the Internet of Things with increasing demands on large data storage and processing. To fulfill these demands, emerging nonvolatile memory technologies with high density and fast access memory cells are highly required [1–4]. Ferroelectric memory has long been considered one of the most promising technologies in this field, featuring nonvolatile, fast read/write access, ultralow power, and extreme radiation hardness [5–8]. The early ferroelectric random access memory based on a ferroelectric capacitor has suffered from a scaling bottleneck below 130 nm CMOS nodes. The main reasons include process compatibility and fade of ferroelectricity in thin perovskite-based ferroelectric films such as lead zirconate titanate and strontium bismuth tantalate [9, 10]. The three-terminal ferroelectric field-effect transistor (FeFET) has been considered an alternative solution, which separates the read/write process and does not detect capacitive charges as a memory state, thus possessing merits such as high scalability and nondestructive readout [11–13].

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Most traditional FeFETs use bulk ferroelectrics as gate dielectric materials and bulk semiconducting materials as conducting channels. In addition, an insulating layer is usually inserted to prevent ferroelectric semiconductor interactions during fabrication and limit the gate leakage current, forming a metal ferroelectric insulator semiconductor stacking structure [14–17]. Because of the unavoidable dangling bonds in bulk materials, complex interfaces occur in insulator ferroelectric and insulator semiconductor contact areas. In addition, the ferroelectricity of bulk ferroelectrics tends to fade in thin films due to the critical size limit [10,18,19]. The existence of these issues has limited the performance of small-footprint FeFETs due to their low endurance and poor retention of the memorized states [20,21]. Recently, with the development of two-dimensional (2D) materials, FeFETs based on 2D channel materials (e.g., graphene and MoS_2) have been frequently studied due to their good performance in reducing interfacial states and suppressing short-channel effects [22–25]. However, because the ferroelectric gate material remains in the bulk phase, interfacial states and ferroelectricity fading in ultrathin films have limited the thickness of the ferroelectric gating layer to hundreds of nanometers [26,27].

Recently, 2D ferroelectrics have been discovered and attracted much attention due to features such as low dimensional ferroelectric stability and free bonds [28–32]. They might provide a straightforward way to totally exclude the interfacial states and ferroelectricity fading issue use 2D ferroelectrics instead of bulk ferroelectrics to form the all-van der Waals (vdW) stacking FeFET. Among the reported 2D ferroelectrics, In_2Se_3 is outstanding due to its stability and reversal switching of out-of-plane ferroelectric polarization [29,33,34]. The unique in-plane-out-of-plane polarization coupling effect in 2D In_2Se_3 also triggers much interest in physics [33] and engineering fields [35,36]. In addition to these features, the growth of In_2Se_3 thin films can be finished at low temperatures ($\sim$250°C), which makes the integration process less disturbing to the performance of semiconducting channels [37].

In this study, In_2Se_3 is adopted as the 2D ferroelectric gate dielectric to form all-vdW FeFETs. First, the high-temperature and thin film ferroelectric stability of In_2Se_3 is examined by Raman spectroscopy and piezoresponse force microscopy (PFM), respectively. Second, a cross structure two-end device is fabricated to explore the device-level out-of-plane ferroelectric switching behavior of In_2Se_3 flakes. Based on these results, utilizing In_2Se_3 as a ferroelectric gate dielectric, h-BN as an insulating layer and MoS_2 as a semiconducting channel, all-vdW stacking FeFETs are fabricated. Then, their transistor and memory performances are examined.

2 Experimental

For the Raman test, the In_2Se_3 flake is mechanically exfoliated from a single crystal (HQ Graphene, 2H α-phase) and then transferred onto the Si/SiO_2 substrate. For the PFM test, the In_2Se_3 flake is transferred onto a Si substrate coated with a Cr/Au (10 nm/40 nm) film as the bottom electrode. The cross-structure Cr/Au-In_2Se_3-Cr/Au devices are fabricated with ultraviolet photolithography and E-beam evaporation, and the electrode (bottom 3 nm Cr/20 nm Au, top 10 nm Cr/40 nm Au) width is 5 μm.

All dry-transfer methods are used for FeFET fabrication [38]. The multilayer MoS_2 nanosheets are exfoliated and transferred with Polydimethylsiloxane onto a Si/SiO_2 substrate as the conductive channel. For good performance, 5–10-nm-thick MoS_2 nanosheets are chosen [39,40]. Few-layer h-BN (4–8 nm) and In_2Se_3 (15–25 nm) are transferred onto MoS_2 in sequence to form the all-vdW stacking structure. Afterward, the Cr/Au (10 nm/50 nm) electrodes are deposited with E-beam evaporation at the E-beam lithography patterned area.

3 Results and discussion

α-phase In_2Se_3 is a 2D ferroelectric material with intercorrelated in-plane and out-of-plane polarization [29,41]. The quintuple layer (QL) structure of the α-In_2Se_3 monolayer is shown in Figure 1(a). In previous studies for In_2Se_3, the thickness of a monolayer of approximately 1.2 nm and that of a bilayer of approximately 2.3 nm have been measured [34,42]. The center layer Se can be switched by an external electric field between positions "a" and "b", resulting in simultaneous in-plane and out-of-plane polarization flipping. For multilayer α-In_2Se_3 films, the adjacent QLs are stacked via vdW interactions.

For application in memory, temperature stability is important, especially for 2D materials that are sensitive to the ambient environment [28,43]. To identify if the ferroelectric phase is stable at high temperatures, variable temperature Raman spectroscopy is performed on a 22-nm-thick In_2Se_3 flake.

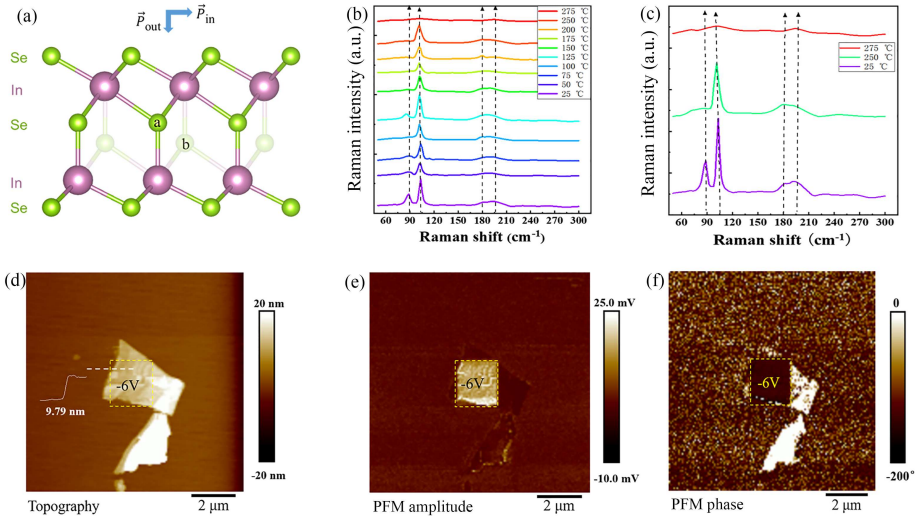

Figure 1 (Color online) (a) Lattice structure of α-In_2Se_3 QL (monolayer). When the central layer Se atoms are at position "a", the corresponding directions of the in-plane and out-of-plane polarization are shown above. (b) Variable temperature Raman spectra of a 22-nm-thick In_2Se_3 flake. (c) Raman spectra measured at 25°C, 250°C, and 275°C. (d) AFM topography of an exfoliated In_2Se_3 flake. The line profile gives the thickness of the flake (9.79 nm). (e) and (f) PFM amplitude and phase response of the flake, respectively. The center 2 μm × 2 μm area was swept with −6 V DC before 1000 mV AC scanning (with a driving frequency of 300 kHz) for domain imaging.

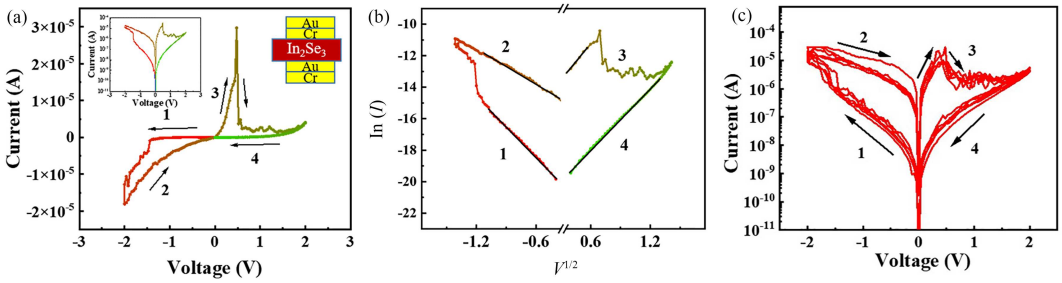

Figure 2 (Color online) (a) Switching behavior in a cross-structure device based on In_2Se_3; the insert curve shows the log(I)-V; (b) the Schottky emission fitting of the I-V curve in (a), showing a good linear fitting; (c) repeated measurement of another cross-structure device for five cycles.

The ferroelectric phase of In_2Se_3 is the α-phase, as verified by previous studies, and the main Raman peak of the α-phase is near 104 cm^{-1}, corresponding to phono mode A_1(LO+TO) [34,41,44]. As shown in Figures 1(b) and (c), as the temperature increases, the Raman peak at 104 cm^{-1} remains stable even at a high temperature of 250°C, proving that the ferroelectric α-phase is still a stable phase at a high temperature. These results indicate that the ferroelectricity of 2D In_2Se_3 is robust at high temperatures and not as sensitive as other 2D materials [28,45]. Figure 1(d) shows the atomic force microscope (AFM) topography of an exfoliated In_2Se_3 flake. From the line profile, a thickness of 9.79 nm is confirmed. Figures 1(e) and (f) show the PFM amplitude and phase response of the In_2Se_3 flake after poling by scanning at a small area (2 μm × 2 μm) with an electrically biased conductive tip (SCM-PIT-V2 Ir/Pt coated). Similar to the previous report, a clear phase contrast of nearly 180° appeared after −6 V polling. As the PFM phase response represents the polarization direction of the domain [45,46], this result verifies the switching ability of ferroelectric polarization in an ∼10 nm In_2Se_3 flake.

Afterward, the cross-structure Cr/Au-In_2Se_3-Cr/Au devices are fabricated for device-level ferroelectricity exploration. As an n-type semiconductor with a work function (WF) of ∼4.9 eV [37], In_2Se_3 forms a Schottky contact with high WF Au (∼5.1 eV) and an ohmic contact with a low WF Cr (∼4.6 eV). Therefore, the as-fabricated cross structure device can be regarded as a one-side Schottky diode. A zero-crossing hysteretic I-V curve was observed in this diode, as shown in Figure 2(a). When a negative voltage sweeps from 0 to −2 V, the resistance of the In_2Se_3 device switches from high resistance to low resistance (phase 1 to phase 2). Then, when a positive voltage sweeps from 0 to 2 V, the resistance switches back from low to high (phase 3 to phase 4). As shown in Figure 2(b), the good linear fitting

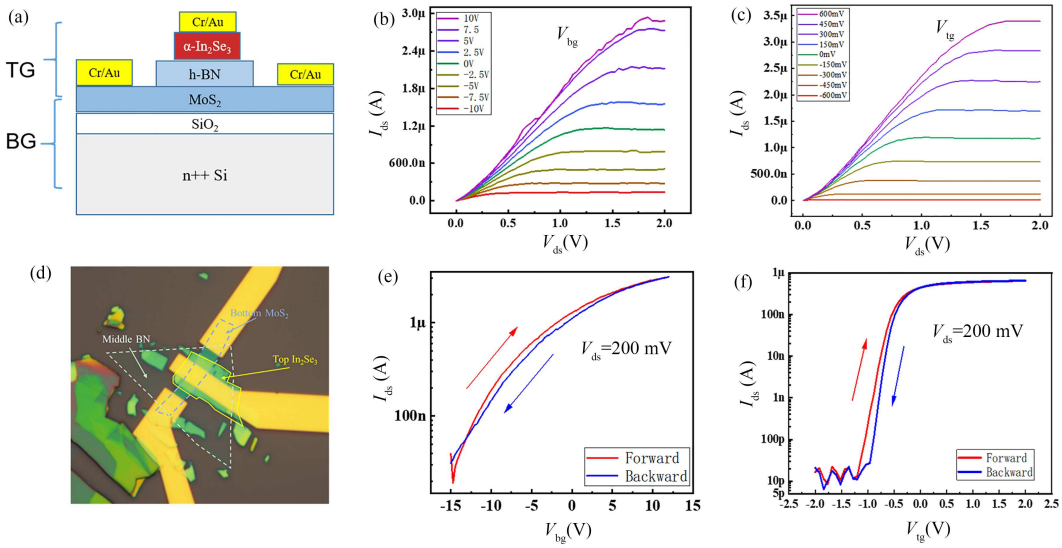

Figure 3 (Color online) (a) Cross-sectional schematic illustration of the all-vdW stacking FeFET device. (b) and (c) Output and transfer characteristic curves under BG tuning, respectively. (d) Optical microscopic image of an as-fabricated FeFET device. The outlines of the bottom MoS_2, middle hBN and top In_2Se_3 are shown. (e) and (f) Output and transfer characteristic curves under TG tuning, respectively.

of all four phases with the $\ln(I)$-$V^{1/2}$ relation suggests that Schottky emission is the main conduction mechanism in this device [47]. Hence, the change in resistance states can be explained by the Schottky barrier height control under different ferroelectric polarizations of In_2Se_3. From phase 1 to phase 2, the negative voltage changes the ferroelectric polarization to point to the Au side, which results in a Schottky barrier height decrease, and thus a resistance decrease [48]. From phase 3 to phase 4, the positive voltage switches the polarization back to the Cr side, which results in a Schottky barrier height increase and thus a resistance increase. The repeated measurement in Figure 2(c) shows that this switching behavior is reproducible. The results on the cross structure device indicate the device-level out-of-plane ferroelectric switching ability of In_2Se_3.

The above results confirm the robust and switchable out-of-plane ferroelectricity of 2D In_2Se_3 flakes, which is important for the realization of all-vdW stacking FeFETs. Figure 3(a) shows a schematic illustration of a typical In_2Se_3-FeFET device. An optical microscopic image of an as-fabricated FeFET device is shown in Figure 3(b). In this device, the flake thicknesses of the bottom-layer MoS_2 (8 nm), middle layer h-BN (4 nm), and top-layer In_2Se_3 (15 nm) are measured by the AFM. The channel length and width are 10 and 5 μm, respectively. Based on the MoS_2 channel and different gates, the device could be treated as two field-effect transistors, that is, a back-gate (BG) transistor and a top-gate (TG) transistor. The BG transistor utilizes a heavily doped n-type silicon substrate as the gate electrode, and 90 nm SiO_2 serves as the gate dielectric. For the TG transistor, all-vdW stacking (MoS_2–BN–In_2Se_3–Au) is adopted. The out-of-plane ferroelectric polarization of In_2Se_3 is used to provide a nonvolatile electric field for channel conductance tuning, and the BN is a 2D insulator for limiting the leakage current between the top gate and channel. The BN layer helps suppress the leakage current from In_2Se_3—a semiconducting ferroelectric. If the BN layer is too thin, the tunneling current will degenerate the device performance [49]. Considering the MoS_2 stack as a ferroelectric capacitor in series with the BN capacitor, if the thickness of the BN increases, the capacitance of the BN capacitor will decrease, and then less gate voltage will be loaded on the ferroelectric capacitor. Hence, a thicker BN layer will lead to a larger gate voltage needed for ferroelectric switching.

The BG output characteristics with different gate biases are shown in Figure 3(c). A sweeping voltage of 0–2 V is applied between the source and drain (V_{ds}). A positive BG voltage results in a channel current (I_{ds}) increase, whereas a negative BG voltage results in a current decrease, revealing that the MoS_2 layer is an n-type channel. In Figure 3(d), the transfer characteristics of the BG device at V_{ds} = 0.2 V show a clockwise hysteresis loop, which is usually caused by factors such as interfacial states between MoS_2−SiO_2 or adsorbates in ambient air [50].

The TG output and transfer characteristics are shown in Figures 3(e) and (f), respectively. Because of the thinner insulating layer, the controllability of the TG is better than that of the BG. From the

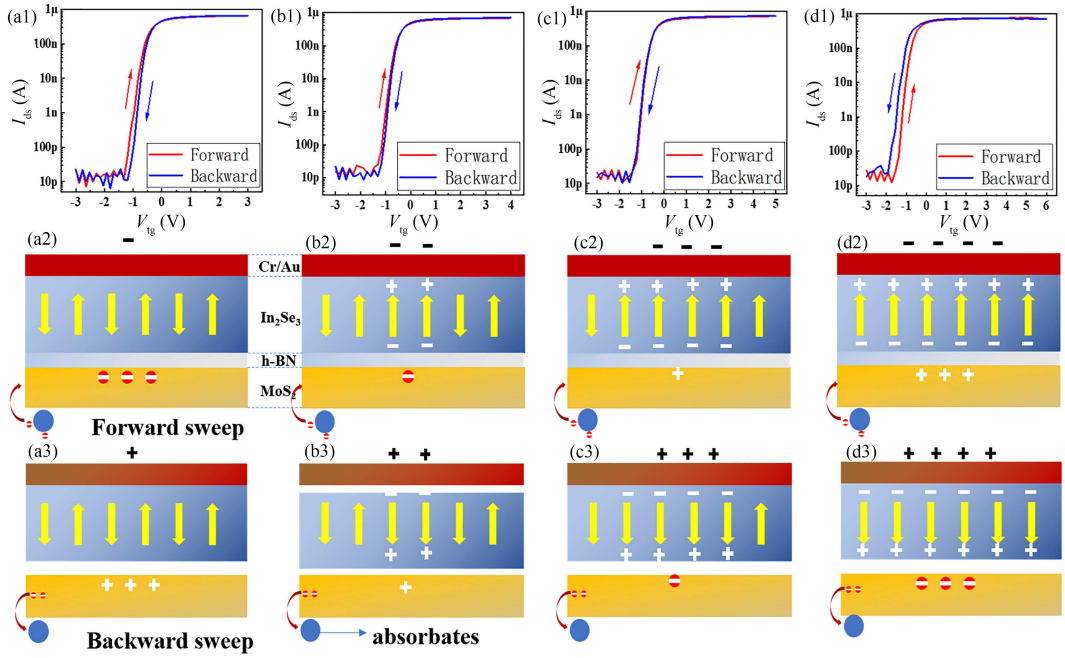

Figure 4 (Color online) Transfer characteristics of a TG device under different sweeping voltages. As $V_{\max}$ increases from 3 to 6 V, the direction of the curve changes from clockwise to counterclockwise, as shown in (a1)–(d1). The influence of absorbance-induced trapping-detrapping charges and ferroelectric polarization-induced screening charges are illustrated in (a2)–(d3). (a2)–(d2) correspond to the forward sweeps, and (a3)–(d3) correspond to the backward sweeps.

transfer curve, an on-off ratio of $\sim 10^5$ is achieved, and the minimum subthreshold slope (SS) reaches 107 mV/dec, manifesting the good performance of the TG device as a transistor. In addition, a similar clockwise hysteresis loop to the BG is observed when applying a TG sweeping voltage ($V_{\rm tg}$) in the direction of -2 V$\rightarrow$2 V$\rightarrow$ -2 V. As the TG structure is all-vdW stacking, the interfacial states can be excluded, and this clockwise hysteresis loop might be caused by adsorbates in the air [43, 51].

In subsequent measurements, higher voltages are applied to the top gate. As shown in Figures 4(a1)–(d1), the negative maximum gate voltage ($-V_{\max}$) of the transfer curves is kept at -3 V, whereas the positive maximum gate voltage ($V_{\max}$) increases from 3 to 6 V. When $V_{\max}$ is 3 V, the transfer curve shows a clockwise hysteresis loop. Upon increasing $V_{\max}$ to 5 V, the hysteresis loop nearly disappears. By increasing $V_{\max}$ to 6 V, a counterclockwise hysteresis loop is achieved, which is different from the loop caused by absorbates. Meanwhile, according to previous studies on common transistors with MoS_2/h-BN/gate stacking, no counterclockwise hysteresis loop has been observed, which can exclude the memory effect of MoS_2 and h-BN [48, 52]. Based on these facts, we speculate that this behavior is caused by channel conductance tuning under different ferroelectric polarizations of the In_2Se_3 layer [52, 53].

To elucidate the change in the hysteresis loop from clockwise to counterclockwise, an analysis is given as follows: In the TG transistor, the voltage sweeping from negative to positive is defined as forward. First, the influence of absorbates on the MoS_2 channel conductance is considered. At the beginning of the forward sweep, a negative $V_{\rm tg}$ depletes the MoS_2 channel. When $V_{\rm tg}$ increases, electrons trapped at absorbates are released and transferred to the MoS_2 channel, producing additional negative charges in the channel and enlarging $I_{\rm ds}$. In the backward sweep, the situation is contrary, a positive $V_{\rm tg}$ results in channel electron accumulation, and then some electrons are trapped by absorbates, increasing the depletion level of the channel and reducing $I_{\rm ds}$. Therefore, the charge trapping-detrapping process will lead to a counterclockwise hysteresis loop [53]. Conversely, when increasing $V_{\rm tg}$ to over the coercive voltage of the In_2Se_3 layer, dipole switching will have an impact on the channel conductance. A forward sweep from $-V_{\max}$ leads to dipoles pointing upward, inducing additional positive screening charges in the MoS_2 channel, which will reduce $I_{\rm ds}$. This reduction persists until a positive voltage changes the direction of dipoles downward. A backward sweep starts with dipoles pointing downward, such that the induced negative screening charges will enlarge $I_{\rm ds}$. Consequently, the ferroelectric polarization of the In_2Se_3 layer results in a counterclockwise hysteresis loop. The situation observed in Figures 4(a1)–(d1) can be explained by the combination of the abovementioned two mechanisms. At a small $V_{\max}$, the macroscopic

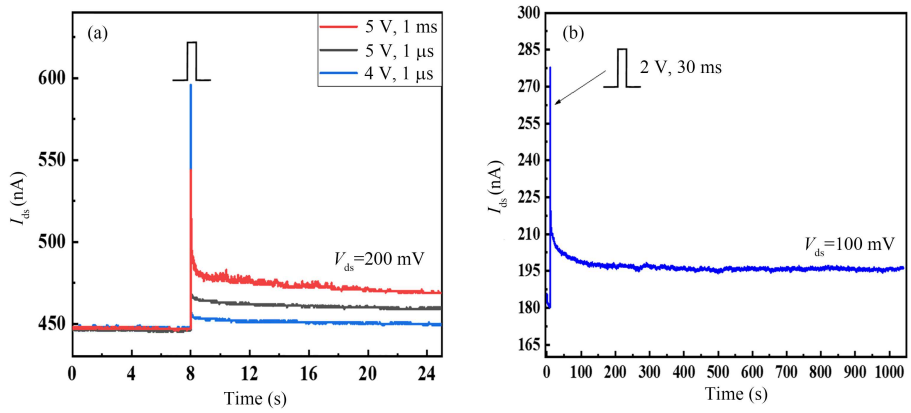

Figure 5 (Color online) (a) Channel current changes after different pulses are applied through the TG; (b) retention property of another all-vdW stacking FeFET after a suitable pulse (2 V, 30 ms) is applied to the TG.

polarization of In_2Se_3 is zero, so the absorbance trapping-detrapping process dominates (Figures 4(a2) and (a3)), resulting in the observed clockwise hysteresis loop presented in Figure 4(a1). When V_{max} increases, the influence of polarization will play an increasingly important role (Figures 4(b2)–(d3)), resulting in a gradual change in the hysteresis loop direction from clockwise to counterclockwise.

In particular, the memory window of the In_2Se_3 based FeFET is not large. We speculate that the WF difference on the two surfaces of the polarized In_2Se_3 layer plays an important role. According to Kang et al. [54]'s first-principles calculations, there is a large WF difference on the two surfaces of the polarized In_2Se_3 monolayer. Considering that this is similar in a multilayer In_2Se_3, the WF difference will produce an electric field opposite to the depolarization field (E_d) inside the In_2Se_3 layer. As a result, fewer screening charges are needed in the MoS_2 channel for the cancellation of E_d and thus the memory window of the FeFET is expected to decrease. This is an important factor that we should consider when applying 2D ferroelectrics in FeFETs. To better understand the influence of the WF difference, more quantitative studies related to the WF difference measurement of 2D ferroelectric layers and their impact on the performance of the all-vdW FeFET should be conducted in the future research.

In addition, the pulse response of the TG transistor is explored. In Figure 5(a), I_{ds} under a V_{ds} of 200 mV can be tuned by different pulses. A larger pulse amplitude and wider pulse width can result in a larger channel current increase, which indicates that the partial switching of ferroelectric domains can be achieved by varying the pulse amplitude and width. Meanwhile, the retention of memorized states is important. In Figure 5(b), I_{ds} increases after a suitable gate pulse can persist over 1000 s, showing the nonvolatile property of the all-vdW FeFET device.

4 Conclusion

In summary, the stability of In_2Se_3's ferroelectric phase over 250°C and the ferroelectricity of In_2Se_3 thin films down to ~10 nm have been confirmed by variabletemperature Raman spectroscopy and PFM, respectively. These results show the robust 2D ferroelectricity of In_2Se_3 flakes. Afterward, the device-level ferroelectric polarization switching of In_2Se_3 is demonstrated in a cross-structure sample. Based on these results, 2D In_2Se_3 is thought to be a suitable material for 2D ferroelectric gate dielectrics, and all-vdW FeFETs are fabricated by adopting an In_2Se_3 layer. An obvious transition from a clockwise hysteresis loop to a counterclockwise hysteresis loop has been observed in the TG device. Hence, the ferroelectric polarization of the In_2Se_3 layer plays a dominating role when a large gate voltage is applied. Furthermore, a pulse-induced nonvolatile and tunable channel conductance change has been achieved in the FeFET device, showing the possibility of its application in multilevel memory. Because of the all-vdW stacking, the scaling issue and interfacial-state issue in traditional FeFETs and FeFETs using 2D channels have been resolved, and the robust memory effect has been shown, paving the way for FeFETs toward ultrahigh-density integration. Our results suggest that In_2Se_3 is a suitable 2D ferroelectric gate dielectric material, and all-vdW stacking FeFETs are promising for achieving high-density ferroelectric memory.

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