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Experimental investigation of a novel junction-modulated hetero-layer tunnel FET with the striped gate for low power applications

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Silicon-based tunneling field effect transistor (TFET) with a band-to-band tunneling mechanism has been widely studied due to its ultra-steep subthreshold swing (SS), ultra-low leakage current ($I_{\rm off}$), and good complementary metal-oxide-semiconductor process compatibility [1]. However, the operation of silicon-based TFET faces two major challenges. On the one hand, the large indirect band gap of silicon reduces the tunneling probability, and thereby the on-state current ($I_{\rm on}$) [2]. On the other hand, it is difficult to experimentally form abrupt source tunneling junctions [3], and the average SS ($\rm SS_{avg}$) of experimental TFETs is relatively large [4].

In this study, a novel junction-modulated hetero-layer TFET (JHL-TFET) proposed in [5] is experimentally demonstrated for the first time. Owing to the advantageous hybrid mechanism of the junction modulation effect and adaptive energy band engineering, the minimum SS ($\rm SS_{min}$) of the fabricated JHL-TFET is reduced by 38% compared with conventional TFET. The SS remains largely constant over a current range of 4 decades, leading to an enhancement of three orders of magnitude in $I_{\rm on}$. On further optimizing the equivalent oxide thickness (EOT), the $I_{\rm on}$ can attain values up to 17.2 μA/μm with $V_{\rm DS} = -0.6$ V.

Device structure and experiment. The JHL-TFET combines the advantages of both the junction-modulated TFET (JTFET) [6] and heterostacked TFET (HS-TFET) [7], and its device structure is illustrated in Figures 1(a–c). On the one hand, the striped gate of the JHL-TFET extends into the source region of the device, leading to a steeper band-to-band tunneling junction when the tunneling window is open [5, 6] with a smaller $\rm SS_{min}$ and higher $I_{\rm on}$. On the other hand, the active area of the JHL-TFET is formed by two layers of materials with different band gaps, in which the upper layer has a larger band gap than the lower layer. This causes the adaptive energy band engineering mechanism [5, 7] to suppress SS degradation and enhance $I_{\rm on}$ simultaneously.

The p-type Si-$\rm Si_{0.67}Ge_{0.33}$ JHL-TFETs and traditional TFETs of the same footprint are fabricated as illustrated in Figure 1(d). Figure 1(e) depicts the good crystalline quality of the epitaxial SiGe layer and the Si layer. Figure 1(f) illustrates the top view scanning electron microscopy image of the fabricated Si-$\rm Si_{0.67}Ge_{0.33}$ JHL-TFET, and Figure 1(g) illustrates the cross-sectional view transmission electron microscopy images of the epitaxial stack structure for the Si-$\rm Si_{0.67}Ge_{0.33}$ JHL-TFET devices.

Results and discussion. The measured transfer characteristics of the experimentally fabricated Si-$\rm Si_{0.67}Ge_{0.33}$ JHL-TFETs with a 5 nm Al_2O_3 (EOT = 3.3 nm) are illustrated in Figure 1(h-I). Because the Si-$\rm Si_{0.67}Ge_{0.33}$ JHL-TFET enables a steeper band-to-band tunneling junction at the source junction compared with the conventional Si TFET, the fabricated device exhibits a 38% reduction in the $\rm SS_{min}$. Meanwhile, because the adaptive bandgap engineering can achieve the adaptive current replenishment behavior with an increasing $V_{\rm GS}$, thereby suppressing SS degradation in the JHL-TFET, the extracted SS degradation factor (defined as $(\rm SS - SS_{min})/SS_{min}$ [7]) of the fabricated Si-$\rm Si_{0.67}Ge_{0.33}$ JHL-TFET is effectively reduced, as depicted in Figure 1(h-II). Moreover, because the $\rm Si_{0.67}Ge_{0.33}$ in the underlying layer has a smaller bandgap than the Si in the upper layer, the fabricated Si-$\rm Si_{0.67}Ge_{0.33}$ JHL-TFET can achieve an on-

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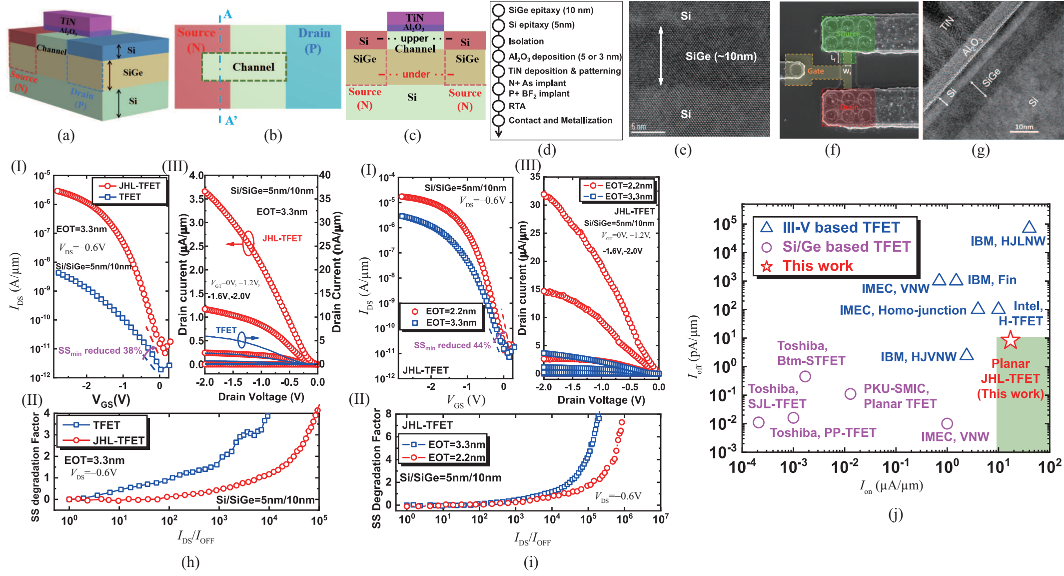

Figure 1 (Color online) (a) Schematic diagram of the novel junction-modulated hetero-layer tunneling field effect transistor (JHL-TFET) fabricated; (b) top view of the device after removal of the gate in (a); (c) cross-sectional view of the device along the direction of AA' in (b); (d) process flow of Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET; (e) good crystalline quality of the epitaxial SiGe layer and the Si layer; (f) top view scanning electron microscopy image of Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET; (g) cross-sectional view of the epitaxial stack structure for Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET through transmission electron microscopy; (h-I–III) measured transfer characteristics, extracted subthreshold swing (SS) degradation factor, and measured output characteristics of Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET and conventional Si TFET; (i-I–III) measured transfer characteristics, extracted SS degradation factor, and measured output characteristics of Si-$Si_{0.67}Ge_{0.33}$ JHL-TFETs with different equivalent oxide thicknesses; (j) comparison of $I_{\rm on}$ vs. $I_{\rm off}$ for experimentally fabricated Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET with other reported Si/Ge or III-V-based TFETs.

current enhancement of nearly three orders of magnitude compared with the conventional Si TFET. Further, the measured output characteristics of the fabricated Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET demonstrate a better output saturation behavior than those in the traditional Si TFET, as illustrated in Figure 1(h-III).

Furthermore, the gate dielectric has been optimized to improve the gate electrical control of the proposed device. As demonstrated in Figures 1(i-I) and (i-II), compared with 5 nm Al_2O_3 (EOT = 3.3 nm), the optimized Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET with 3 nm Al_2O_3 (EOT = 2.2 nm) exhibits superior subthreshold characteristics with the $SS_{\rm min}$ reduced by 44% and further suppressed SS degradation behavior due to a better gate electrical control. Moreover, the $I_{\rm on}$ of the optimized Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET can reach up to 17.2 μA/μm with $V_{\rm DS} = -0.6$ V while maintaining a low $I_{\rm off}$. Moreover, the optimized JHL-TFET with a reduced EOT can achieve superior output characteristics with a lower output resistance in the saturation region, as depicted in Figure 1(i-III). Benchmarking with the published Si/Ge or III-V-based TFETs, the fabricated Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET demonstrates a high $I_{\rm on}$ that is comparable with that of III-V-based TFETs and an off-current comparable with that of silicon-based TFETs, as illustrated in Figure 1(j).

Conclusion. We have experimentally demonstrated a novel JHL-TFET with the striped gate. The fabricated Si-$Si_{0.67}Ge_{0.33}$ JHL-TFET exhibits a hybrid modulation mechanism of junction depletion effect and adaptive bandgap engineering with a significant enhancement in subthreshold characteristics and drive capability over conventional Si TFETs while maintaining a low $I_{\rm off}$. The experimental results indicate that the JHL-TFET has immense potential for ultra-low power applications, such as the internet of things and wearable devices.

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