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Impact of polarization switching on the effective carrier mobility of $HfZrO_x$ ferroelectric field-effect transistor

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Doped-HfO_2 ferroelectrics have attracted tremendous research interest for non-volatile memory and memory-in-computing applications due to their CMOS compatibility, advantages of non-destructive reading, and low power consumption [1, 2]. Recently, various studies were conducted to boost the electrical performance and reliability of HfO_2-based ferroelectric field effect transistors (FeFETs), in terms of wake-up, imprint, limited endurance, and so on [3–5].

The effective channel mobility ($\mu_{\rm eff}$) is a key factor in determining the driving current of the transistor. Interface defect is one of the main factors affecting $\mu_{\rm eff}$ [6]. For FeFET, polarization (P) switching will also affect the density of interface states and the trapping/detrapping at the ferroelectric/channel interface, which will affect the $\mu_{\rm eff}$ of the device. However, there is still a lack of research on the impact of P switching on the $\mu_{\rm eff}$ in HfO_2-based FeFETs, and the change of $\mu_{\rm eff}$ during the retention and endurance measurements must be investigated.

In this study, the impact of P switching, retention, and endurance on the $\mu_{\rm eff}$ of $HfZrO_x$ (HZO) Si-channel FeFETs is experimentally investigated.

Figure 1(a) shows the key steps in the fabrication of HZO FeFET, commencing with a p-Si (100) substrate and using a gate last process. After the source/drain (S/D) was defined and implanted with phosphorus ions (30 keV, 2 $\times$ 10^{15} $\rm cm^{-2}$), dopant activation was performed by rapid thermal annealing at 900°C, followed by the deposition of TaN/HZO stacks. Subsequently, reactive ion etching was used to form the gate electrode, and a 30-nm-thick Ni was deposited in S/D via a lift-off process. Finally, the device was annealed at 550°C for HZO crystallization and S/D metallization. The top view of the fabricated HZO FeFET is shown in Figure 1(b).

Figure 1(c) shows the high-resolution transmission electron microscope image of the TaN/HZO/SiO_2/Si gate stack structure. The sharp interfaces are observed in the metal-ferroelectric-insulator-semiconductor structure. The thicknesses of HZO and SiO_2 layers are 10 nm and 1.1 nm, respectively. Figure 1(d) shows the grazing incidence X-ray diffraction (GIXRD) patterns of the TaN/HZO/SiO_2/Si structure. The incident angle is 1°.

Figure 1(e) shows the polarization-voltage (P-V) curve of the TaN/HZO/SiO_2/Si stack, measured using the axiACCT TF Analyser 3000 at a frequency of 1 kHz. Figure 1(f) shows the measured drain voltage ($I_{\rm D}$) vs. gate voltage ($V_{\rm G}$) curves of the HZO FeFET after write/erase (W/E) pulses. The $I_{\rm D}$-$V_{\rm G}$ curve moves to the positive/negative direction after −7.8 V/+4.5 V, 1 μs pulse, providing a memory window (MW) above 1 V. The threshold voltage ($V_{\rm TH}$) shift is opposite to that caused by charge trapping, confirming the dominant cause of ferroelectric polarization [7].

Here, the C-V split method is used to extract the $\mu_{\rm eff}$ of the transistor, which can be expressed as [8]

$$\mu_{\rm eff} = \frac{L}{W} \cdot \frac{I_{\rm D}(V_{\rm G}) - I_{\rm D}(V_{\rm TH})}{V_{\rm D}} \cdot \frac{1}{(V_{\rm G} - V_{\rm TH}) \cdot C_{\rm OX}}, \quad (1)$$

where L and W are the gate length and width of the transistor, respectively. The L and W of the device are 3 μm and 100 μm, respectively. $V_{\rm D}$ is 0.01 V, $V_{\rm TH}$ is defined by maximum transconductance method. $I_{\rm D}$ ($V_{\rm G}$) and $I_{\rm D}$ ($V_{\rm TH}$) are $I_{\rm D}$ at a given $V_{\rm G}$ and $V_{\rm TH}$, respectively. $C_{\rm OX}$ is the capacitance value under the maximum voltage within the scanning range as shown in Figure 1(g). Figure 1(h) shows the $\mu_{\rm eff}$ as a function of channel inversion charge density ($Q_{\rm inv}$) and $Q_{\rm inv}$ is obtained by $(V_{\rm G} - V_{\rm TH}) \cdot C_{\rm OX}$. At $Q_{\rm inv}$ of 5 $\times$ 10^{15} $\rm cm^{-2}$, the $\mu_{\rm eff}$ of 178 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$ and 148 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$ are obtained after write and erase $V_{\rm G}$ pulses, respectively, both are lower than that for the

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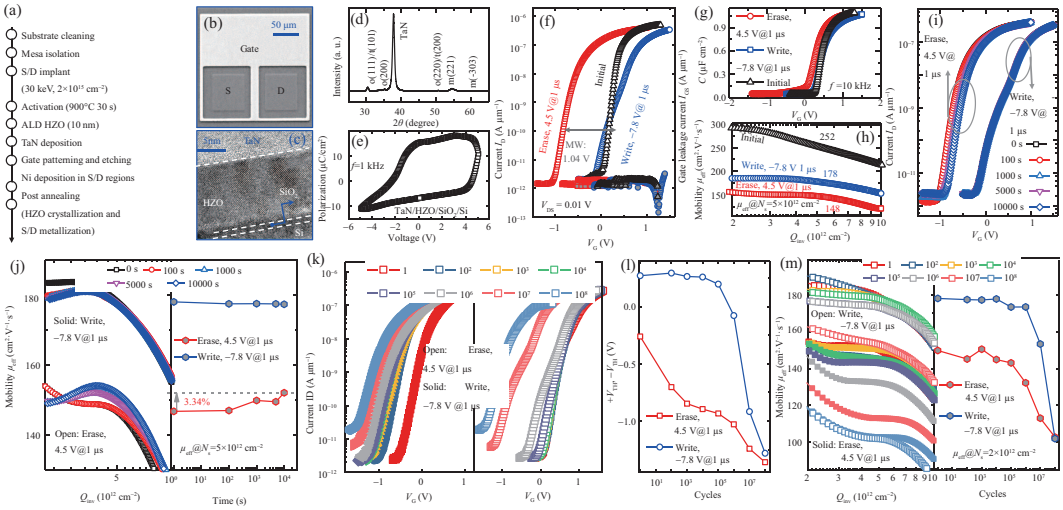

Figure 1 (Color online) (a) Key process steps for fabricating $HfZrO_x$ FeFET; (b) top-view SEM image of $HfZrO_x$ FeFET; (c) TEM image of the gate stack indicating the thicknesses of SiO_2 and $HfZrO_x$ as 1.1 nm and 10 nm, respectively; (d) GIXRD of the TaN/HZO stacks; (e) *P*-*V* curve of the TaN/HZO/SiO_2/Si stack; (f) I_D-V_G curves, (g) *C*-*V*, and (h) μ_{eff}-Q_{inv} of $HfZrO_x$ FeFET for the initial, and the "write" (−7.8 V/1 μs) and "erase" (+4.5 V/1 μs) states; (i) I_D-V_G curves measured at different retention durations; (j) calculated μ_{eff} vs. Q_{inv} during the retention test and the extracted value at a Q_{inv} of 5×10^{12} cm^{-2}; (k) and (l) endurance characteristics of I_D-V_G and V_{TH} evolution; (m) μ_{eff} vs. Q_{inv} during the endurance test and the extracted value at a Q_{inv} of 5×10^{12} cm^{-2}.

initial state, 252 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Undergoing an erase pulse (4.5 V, 1 μs), the V_{TH} of the device moves to the negative V_G direction, due to the positive charges (e.g., oxygen vacancies V_O^{2+}) being trapped at the SiO_2 interfacial layer. Conversely, the write pulse leads to the detrapping of positive charges. During the polarization switching, both trapping and detrapping processes increase the scattering effect of the channel carriers, degrading the μ_{eff}, with a greater effect by the former.

The retention characteristics of I_D-V_G curves after W/E (−7.8 V/+4.5 V, 1 μs) pulses are shown in Figure 1(i), and the extracted corresponding μ_{eff} vs. Q_{inv} curves are shown in Figure 1(j). From the results in Figure 1(j), it can be observed that for the erase state, the μ_{eff} at a Q_{inv} of 5×10^{12} cm^{-2} increases with the retention time possibly due to the neutralization or detrapping of trapped positive charges at the SiO_2 layer by depolarization. For the write state, the μ_{eff} maintains a stable value.

The endurance characteristics of I_D-V_G curves after multiple W/E pulses are shown in Figure 1(k), and Figure 1(l) shows the shift of V_{TH} inducing the wake-up, imprint, and MW reduction of the device. From the pristine state to the 10^8 cycles, the $-V_{TH}$ of the device under 4.5 V V_G erase pulses shifts toward the negative V_G direction, due to the trapping of V_O^{2+} in the SiO_2 IL. For the device under −7.8 V V_G write pulses, the V_{TH} remains stable until 10^5 cycles, indicating the complete detrapping of the V_O^{2+}. However, when the write cycles exceed 10^6, V_{TH} also shifts toward the negative V_G direction, indicating that the trapped V_O^{2+} are only partially detrapped.

Figure 1(m) shows the calculated μ_{eff} vs. Q_{inv} curves for the device and the evolution of μ_{eff} at Q_{inv} of 5×10^{12} cm^{-2} during the endurance test. The μ_{eff} evolution with W/E cycles is consistent with that of the V_{TH} of read I_D-V_G curves of the devices with different W/E pulse cycles. This demonstrates that the trapping/detrapping of V_O^{2+} leads to the degradation/recovery of μ_{eff} of FeFET.

Conclusion. In this study, HZO FeFETs with polarization switching affecting μ_{eff} were experimentally realized. It is demonstrated that the μ_{eff} at Q_{inv} of 5×10^{12} cm^{-2} are 178 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 148 $cm^2 \cdot V^{-1} \cdot s^{-1}$ after W/E (−7.8 V/+ 4.5 V, 1 μs) pulses, respectively, both written and erased μ_{eff} are lower than that for the initial state. The degradation of the μ_{eff} is responsible for the increased scattering effect caused by positive charge trapping and detrapping during polarization switching, and the former's effect is greater.

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