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Implementation of 16 Boolean logic operations based on one basic cell of spin-transfer-torque magnetic random access memory

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Abstract In-memory computing (IMC) systems based on emerging nonvolatile memories (NVMs) provide a thorough solution for memory wall issues and von Neumann bottlenecks. Massive IMC schemes have been proposed by utilizing ingenious structures and additional auxiliary components. However, these schemes are not compatible with the basic cell (one memory unit and one transistor) of emerging random-access memory (RAM), which goes against low-power and high-density requirements. In this paper, we propose a logic implementation scheme based on one magnetic tunnel junction and one transistor (1MTJ-1T), which is the basic cell of spin-transfer-torque magnetic RAM (STT-MRAM). With no other assistance, complete 16 logic operations can be accomplished in two steps with their logic outputs in-situ stored in the MTJ. The area (0.2 μm^2) and energy consumption per logic operation (1.1–2.6 pJ) of the logic gates under 14 nm process node are evaluated using SPICE simulations, indicating its excellent performance. Our work exhibits a 1MTJ-1T-based logic operation implementation, which can bridge the gap between STT-MRAM and high-performance IMC applications.

Keywords in-memory computing, logic operation, magnetic tunnel junctions, transistor, spin transfer torque

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1 Introduction

Emerging nonvolatile memories (NVMs), such as resistance switching memory (RSM), phase-change memory (PCM), and magnetic tunnel junctions (MTJs) have facilitated the development of in-memory computing (IMC), for their resistance state can be a computation operand as well as the in-situ calculation result [1–12]. For example, with proper programmable voltage applied to memristors, the implication (IMP) logic operation can be implemented using 2 $Pt/TiO_2/Pt$ RSM units and 1 load resistor [13]. Based on a TiN/GeSbTe/TiN PCM unit, the 'NOR' and 'NAND' logic operations can be accomplished by two sequential inputs [14]. However, the RSM has worse uniformity and lower endurance, and PCM may require higher operation voltage than MTJs configured by spin-transfer-torque (STT) effect [15–18].

Meanwhile, researchers have put massive efforts into investigating the potential of MTJs for IMC implementation over the last several decades. Already in early 2003, a single magnetic element (MTJ or

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spin valve) along with 3 parallel input lines was proposed to fulfill logic operations through the current-induced Oersted field [4]. Later, a full adder employing 12 transistors and 4 MTJs was proposed [19]. In 2010, 4 logic functions based on the STT effect were presented by directly connecting 3 parallel input MTJs with 1 output MTJ in series [20]. More recently, with the assistance of a current coil and intermediate electronic circuitry, 16 Boolean logic functions were achieved on an MTJ through tri-cycle operation [21]. To improve the on/off ratio, a rectified tunnel magnetoresistance (TMR) device was constructed by combining an MTJ with a diode in parallel, which carries out 4 Boolean logic operations [22]. Although reconfigurable logic functions have been performed based on the memory unit of NVMs combined with ingenious structures and additional auxiliary components, these schemes are not compatible with the basic cell of emerging random-access memory (RAM), i.e., one memory unit and one transistor (1T), which brings high energy consumption and/or integration degradation.

Here, we propose a scheme for implementing reconfigurable logic operations using the basic 1MTJ-1T cell of STT magnetic RAM (STT-MRAM). 16 Boolean logic operations are experimentally performed by configuring the initial state and the working voltage applied to the 1MTJ-1T cell. After proper optimization, the scheme can be well cascaded. We further perform SPICE (simulation program with integrated circuit emphasis) simulations under 14 nm process node to verify the feasibility and reveal the high-density and low-power potential of our proposal. This state-of-the-art demonstration can break the boundary between RAM and IMC applications, and inspire more high-performance computation systems.

2 Results and discussion

2.1 Device fabrication

Our MTJ stacks containing Ta(3)/Ru(20)/Ta(0.7)/Pt(1.5)/$[Co(0.5)/Pt(0.35)]_6$/Co(0.6)/Ru(0.8)/Co(0.6)/$[Pt(0.35)/Co(0.5)]_3$/Pt(0.25)/Ta(0.2)/Co(1.2)/W(0.25)/$Co_{20}Fe_{60}B_{20}$(0.9)/MgO(0.8)/$Co_{20}Fe_{60}B_{20}$(1.2)/W(0.3)/$Co_{20}Fe_{60}B_{20}$(0.5)/MgO(0.5)/Pt(1.5)/Ta(3.0)/Ru(7) (from bottom to top, the numbers in the parentheses denote the thickness in nanometers) are sputtered on the top of vapor-deposited SiO_2 on the fabricated complementary metal-oxide-semiconductor (CMOS) circuit, using a Singulus magnetron sputtering machine and post annealed under vacuum for 1 h at 300°C. The average surface roughness of the substrate, assessed by atomic force microscope, is slightly larger than that of thermally oxidized silicon. Then, the Ta/Ru hard masks were fabricated using electron-beam lithography and inductive coupling plasma etching. The junctions were defined by multistep Ar ion beam etching while varying the beam angle. During milling, we monitored the secondary-ion mass spectra and stopped the milling operation when the signal was detected through the bottom 1.5 nm-thick Pt layer. The bottom residual metal layers were used as the bottom electrode (BE) for electrical measurement. After milling, the MTJs were ex-situ covered with a Si-N passivation layer by using chemical vapor deposition. Subsequently, the Ta hard mask of the nanopillars was formed using a self-aligned process. To form electrical contacts, Ti(10 nm)/Pt(100 nm) top electrodes (TEs) were made on top of the MTJs using photolithography and lift-off. The N-metal-oxide-semiconductor (NMOS) transistor in the experiments is a standard commercial product.

2.2 Basic properties of the discrete MTJ and transistor

Figure 1(a) illustrates the basic structure of the 1MTJ-1T cell, with an MTJ contacted on the drain of an NMOS transistor with its BE [23]. With an appropriate voltage applied to the gate, source and the TE of the MTJ, the resistance state of the MTJ can be configured, thanks to the STT effect [24–27]. In our experiments, a separated MTJ and NMOS transistor are used with peripheral interconnecting wire to imitate the integrated 1MTJ-1T cell, where the free layer (FL) is adjacent to the drain.

Figure 1(b) illustrates the core structure of the used perpendicular MTJ (p-MTJ). Typically, a basic MTJ structure contains 3 layers, i.e., a ferromagnetic (FM) reference layer (RL) with pinned magnetization direction, a nonmagnetic (NM) tunnel barrier and an FM FL with a flexible magnetization direction [28]. Note that a synthetic antiferromagnetic (SAF) layer is required in some perpendicular MTJs to pin the RL [29]. When the magnetizations of the FL and RL are parallel (P), the resistance of an MTJ is low (R_P); otherwise, the resistance is high (R_{AP}). The transmission electron microscopy (TEM) image of an 80-nm-diameter p-MTJ pillar shown in Figure 1(c) demonstrates the high quality of the device fabrication.

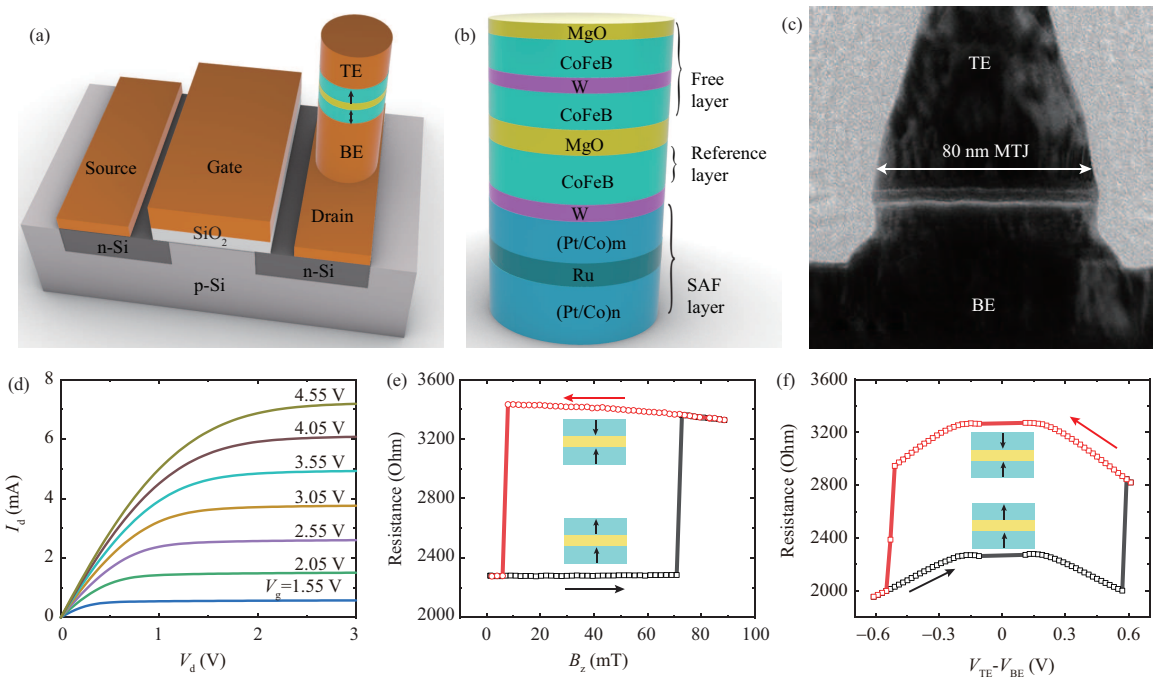


Figure 1 (Color online) (a) Schematic of the 1MTJ-1T cell; (b) basic structure of the fabricated MTJ; (c) TEM photograph of an 80-nm-diameter MTJ; (d) characteristic curve of the NMOS transistor. $I_{\rm d}$: drain current; $V_{\rm d}$: drain voltage; (e) R-H loop of the MTJ in (c). $B_{\rm z}$: the applied magnetic field along z-axis; (f) STT loop of the MTJ in (c) with applied $B_{\rm z} = -27.5$ mT.

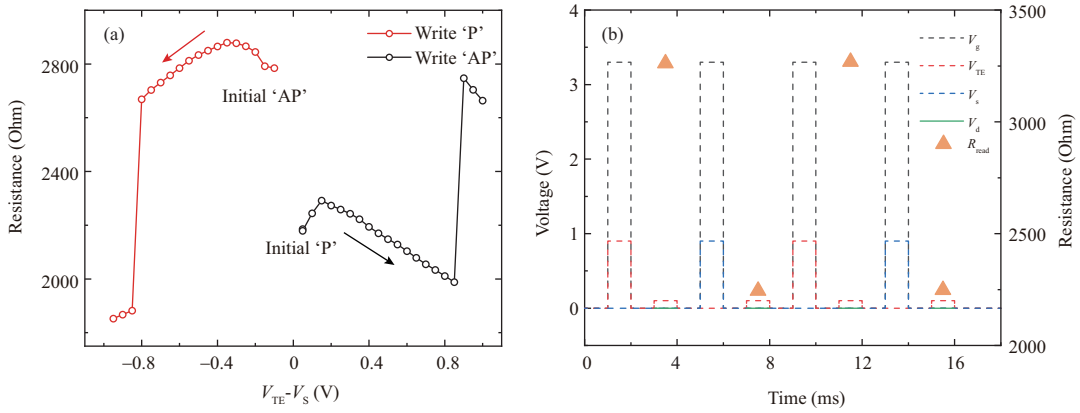


Figure 2 (Color online) (a) MTJ resistance varying with the writing voltage between the TE and the source under $V_{\rm g} = 3.3$ V. $V_{\rm TE}$: TE voltage; $V_{\rm s}$: source voltage. (b) Continuous writing and reading process of the 1MTJ-1T cell. $R_{\rm read}$: reading the resistance of the MTJ.

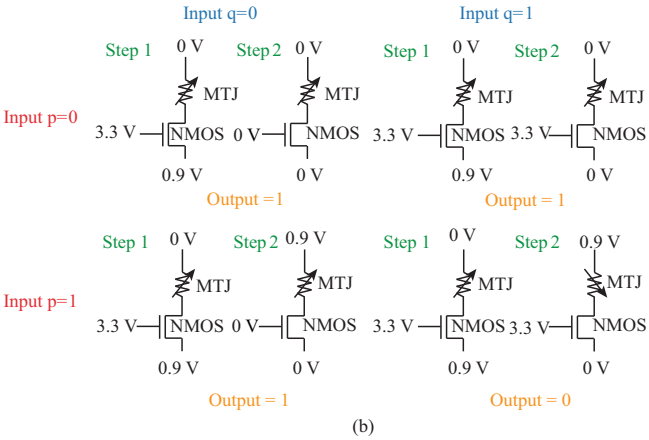
Figure 1(d) plots the typical output curve of the NMOS transistor in use, whose threshold voltage is approximately 1.1 V. Figure 1(e) shows the junction resistance of the MTJ as a function of applied external fields (R-$B_{\rm z}$), from which we can derive TMR ratio of 47.3%. Here, the TMR ratio is given by $(R_{\rm AP} - R_{\rm P})/R_{\rm P} \times 100\%$. The TMR of the p-MTJ is relatively low compared with those of the state-of-the-art works, which may originate from the relatively high roughness of our substrate. Note that the center of the R-$B_{\rm z}$ loop shifts along the x-axis, which probably results from the stray field of the SAF layer. Figure 1(f) is the STT-induced junction resistance switching loop of the MTJ, indicating that voltage exceeding ± 0.58 V between the TE and BE can switch the MTJ state between AP and P, with an applied external field of -27.5 mT.

2.3 Writing and reading process of the 1MTJ-1T cell

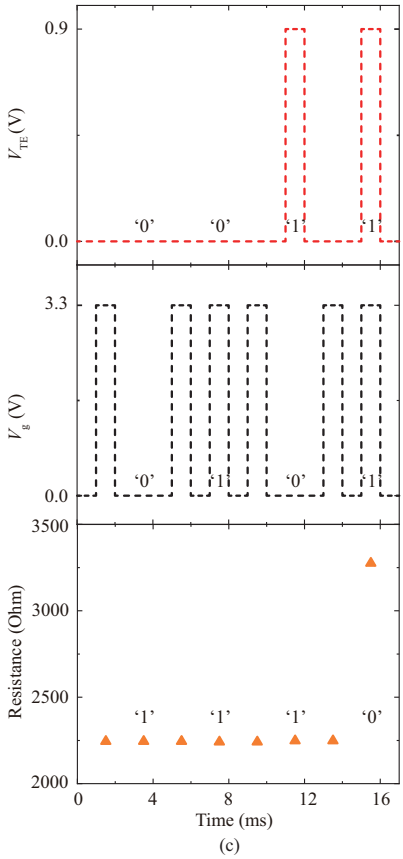
To evaluate the proper writing voltage between the TE and source ($V_{\rm TE} - V_{\rm s}$), continuous voltage tests are carried out as shown in Figure 2(a). When the initial state of the MTJ at $(V_{\rm TE} - V_{\rm s}) = 0$ is set as

Operation steps for NAND Logic					
Logic operation		p NAND q			
Input	p	0	0	1	1
	q	0	1	0	1
S1 preset I=1	T	0			
	G	1			
	S	1			
S2 writing T=p G=q S=0	T	0	0	1	1
	G	0	1	0	1
	S	0	0	0	0
Logic output		1	1	1	0

(a)



(b)



(c)

Figure 3 (Color online) (a) 2-step NAND logic implementation; (b) operation schematics of NAND logic; (c) experimental measurement of NAND logic.

'P', with the voltage of '$V_{TE} - V_s$' up to 0.82 V, the MTJ state can be switched to 'AP'. Similarly, the MTJ state would change from the initial 'AP' to 'P' state when ($V_{TE} - V_s$) down to −0.8 V. Note that the gate voltage (V_g) of the NMOS transistor is always set to 3.3 V in the test. According the above measurements, we can find that the writing voltage can be ±0.9 V between the TE and source.

Figure 2(b) presents the continuous writing and reading test results of the 1MTJ-1T cell. For example, from 1–2 ms, a 3.3, 0.9, and 0 V voltage pulses are applied to the gate ($V_g = 3.3$ V), TE ($V_{TE} = 0.9$ V) and source ($V_s = 0$), repectively. Therefore, the MTJ will be set to the 'AP' state. Then in 3–4 ms, a 0.1 V reading voltage ($V_{read} = 0.1$ V) is applied to TE, while 0 V is applied to the drain (BE) with all other electrodes suspended. By measuring the current flow, the resistance (R_{read}) of MTJ is obtained. The similar process of writing 'P' state and following the reading process is carried out in 4–8 ms. More writing and reading processes are implemented thereafter, showing good repeatability.

2.4 Implementation of 16 Boolean logic operations

According to the above results, we find that the resistance state of MTJ can be flexibly configurated through setting the working voltage of source, gate, and TE, which provides multi-dimensional manipulation capability for realizing reconfigurable logic operations. Here, the high voltage (3.3 V for V_g and 0.9 V for V_{TE} or V_s) and low resistance (R_P) are defined as bit '1'; otherwise bit '0'. To implement the logic operations, we derive a 2-step process based on a 1MTJ-1T cell, including setting the initial state of MTJ (i.e., preset process) and the following data writing process.

In the following, we take 'NAND' logic operation as an example to introduce the logic operation process. Configuration parameters for implementing 'NAND' logic operation are presented in Figure 3(a). At preset step S1, the initial state of MTJ, represented by 'I' is set to be '1'. Then at step S2, a voltage equal to input 'p' is applied to TE (T = p), while 'q' is applied to gate (G = q) and '0' to source (S = 0). The final state of MTJ can be the result of 'p NAND q'. Figure 3(b) illustrates the steps for different

Table 1 Full logic implementation

Logic function	S 1		S 2		Input p	0	0	1	1
	I	G	T	S	Input q	0	1	0	1
0	0	0	p	q		0 (3261)*	0 (3261)	0 (3261)	0 (3261)
1	1	0	p	q		1 (2244)	1 (2244)	1 (2244)	1 (2244)
p	p	0	q	0		0 (3261)	0 (3261)	1 (2244)	1 (2244)
q	q	0	p	0		0 (3261)	1 (2244)	0 (3261)	1 (2244)
$\overline{p}$ (NOT p)	0	1	p	1		1 (2266)	1 (2266)	0 (3305)	0 (3305)
$\overline{q}$ (NOT q)	1	1	q	0		1 (2265)	0 (3295)	1 (2265)	0 (3295)
p+q (OR)	p	q	p	1		0 (3275)	1 (2251)	1 (2251)	1 (2251)
pq (AND)	0	q	p	0	Output	0 (3258)	0 (3265)	0 (3271)	1 (2241)
$\overline{p}$+$\overline{q}$ (NAND)	1	q	p	0		1 (2241)	1 (2241)	1 (2248)	0 (3275)
$\overline{p} \cdot \overline{q}$ (NOR)	$\overline{q}$	p	1	q		1 (2251)	0 (3275)	0 (3268)	0 (3278)
$\overline{p}$+q (IMP)	1	p	1	q		1 (2254)	1 (2260)	0 (3265)	1 (2241)
p+$\overline{q}$ (RIMP)	1	1	q	p		1 (2251)	0 (3275)	1 (2265)	1 (2251)
$\overline{p}$q (RNIMP)	0	q	p	1		0 (3291)	1 (2251)	0 (3305)	0 (3305)
p$\overline{q}$ (NIMP)	p	p	q	$\overline{q}$		0 (3258)	0 (3268)	1 (2241)	0 (3275)
p$\overline{q}$+$\overline{p}$q (XOR)	p	q	p	$\overline{p}$		0 (3265)	1 (2241)	1 (2241)	0 (3275)
pq+$\overline{p} \cdot \overline{q}$ (XNOR)	$\overline{p}$	q	$\overline{p}$	p		1 (2265)	0 (3275)	0 (3275)	1 (2251)

* The number in the brackets denotes the resistance of MTJ, dimension: Ω.

logic inputs. At S1, $V_g = 3.3$ V, $V_s = 0.9$ V, and $V_{TE} = 0$ V are applied to set MTJ as 'P' state (I = 1). Then at S2, for logic input (p, q) = (1, 1), $V_g = 3.3$ V, $V_{TE} = 0.9$ V, and $V_s = 0$ V are applied to switch the MTJ from 'P' to 'AP' state, corresponding to logic output '0'. For the other logic inputs, i.e., (p, q) = (1, 0), (0, 1), or (0, 0), either V_g or V_{TE} is set to '0', the MTJ cannot be switched and would maintain its initial 'P' state, corresponding to logic output '1'. The experiment results in Figure 3(c) exhibit the resistance states of MTJ under different V_g and V_{TE}, demonstrating the 'NAND' logic operation.

Similar to 'NAND' logic operation, all 16 Boolean logic operations can be implemented in 2 steps as shown in Table 1 through configuring the initial state of MTJ, V_{TE}, V_g, and V_s. It is notable that the initial state of MTJ is variable for some logic operations, which can be preset to be 'p', 'q', '$\overline{p}$', '$\overline{q}$'. Here, '$\overline{p}$' ('$\overline{q}$') represents the negation of 'p' ('q'). All the outputs are experimentally measured and the results are attached in Table 1.

We take 'XOR' as an example to clearly reveal the logic operations with variable initial states. For logic inputs (p, q) = (1, 1) and (1, 0), initial state of MTJ is set to 'P' at step S1 (I = p = 1). For (p, q) = (1, 1), $V_g = 3.3$ V (G = q = 1), $V_{TE} = 0.9$ V (T = p = 1) and $V_s = 0$ V (S = $\overline{p}$ = 0) are applied to switch the MTJ from 'P' to 'AP' state, corresponding to logic output '0' at step S2. For (p, q) = (1, 0), the state of MTJ cannot be switched because $V_g = 0$ V (G = q = 0), corresponding to logic output '1' at step S2. For logic inputs (p, q) = (0, 0) and (0, 1), initial state of MTJ is set to 'AP' at step S1. For (p, q) = (0, 1), $V_g = 3.3$ V (G = q = 1), $V_{TE} = 0$ V (T = p = 0) and $V_s = 0.9$ V (S = $\overline{p}$ = 1) are applied to switch the MTJ from 'AP' to 'P' state, corresponding to logic output '1' at step S2. For (p, q) = (0, 0), the state of MTJ cannot be switched because $V_g = 0$ V (G = q =0), corresponding to logic output '0'. The 'XOR' logic operation is carried out.

However, the operation scheme as shown in Table 1 is not stateful, for the 2 operands are voltages while the output is resistance state of MTJ. Here, based on our experimental results, we propose another operation scheme (see Appendix A) which takes the resistance state of MTJ as one of the operands with the result in-situ stored in the MTJ, and thus the optimized scheme can be well cascaded. Note that most of the logic function can be realized in 1 step except NAND and NOR logic, which require 2 steps.

2.5 Discussion

Toward practical applications, some technical factors including scaling, operation speed and power consumption play a vital role and should be deeply considered. Therefore, we evaluate the performance of our proposal and provide a discussion and comparison with other work from the mentioned perspectives.

We conducted SPICE simulations under 14 nm node to evaluate the performance of our proposal. The STT-p-MTJ model is an open-source resource of Spinlib [30][1)]. More details of the SPICE model

1) http://spinlib.com/STT_PMA_MTJ.html.

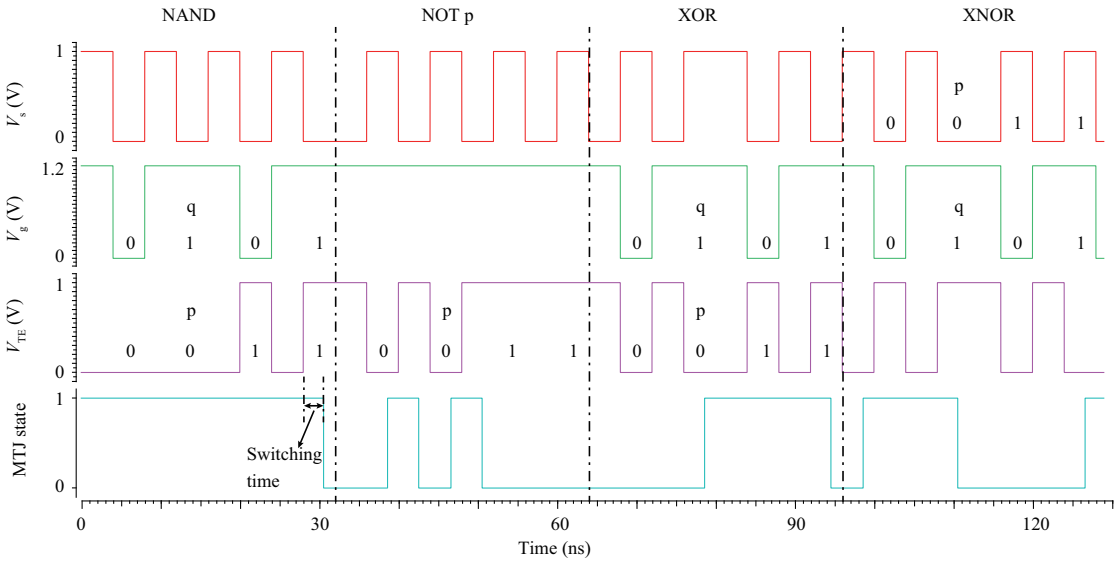


Figure 4 (Color online) Transient simulation of programmable logic operations for 1MTJ-1T cell. 4 different logic functions are presented as examples. When MTJ is ready to change its resistance state, an approximately 2.4 ns latency remains after the applied pulse, donating the switching time (or speed).

can be found in Appendix B. The 50-nm-diameter MTJ is vertically stacked on the drain of a CMOS transistor with the fin width of 10 nm. In this case, the 1MTJ-1T cell area, which mainly depends on the transistor, is approximately 0.2 μm^2. Then, we determine the instantaneous state of MTJ varying with applied pulses voltage of V_g, V_{TE}, and V_s according to the electrical models of MTJ and transistor. The transient results in Figure 4 can not only verify the feasibility of the proposed logic, but also prove that the 1MTJ-1T cell is an excellent time-resolved programmable logic gate. Considering the trade-off between the speed and energy cost, our proposal can achieve ∼2.4 ns switching speed from P to AP state while ∼2.15 ns from AP to P state, and <1.4 pJ writing energy (∼1.3 pJ @ writing bit '0' and ∼1.1 pJ @ writing bit '1'), indicating for one logic function including S1 and S2, the total time cost and power consumption can be less than 4.8 ns and 2.6 pJ, respectively. That is, in the time and energy scale of 4.8 ns and 2.6 pJ, the calculation and data storage are realized simultaneously with no data transition. In comparison, at least a 4.9 ns time delay and 2.5 pJ power consumption occur when using standard CMOS logic to calculate as well as STT-MRAM to transfer and store data (see Appendix C). Our proposal has a similar performance to the CMOS circuit, but costs much less area. Moreover, the preset step S1 can be realized with pulse width of less than 0.8 ns when using our proposed toggle spin torque p-MTJ as an alternative [31]. Thus, the extra time delay of S1 can be significantly reduced. Notably, the energy cost for different logic inputs is variable because step S2 consumes almost no energy when $V_g = 0$ V. In this case, the total energy consumption of S1 and S2 is less than 1.4 pJ. The performance of our proposal can be further improved with the technology nodes scaling down and adopting other assistance effects, such as voltage controlled magnetic anisotropy.

Table 2 compares different IMC schemes based on various emerging NVM units. Except for the intrinsic advantages of STT-MRAM compared with other NVMs, we focus on the compatibility, integrability and functionality of these proposals. Our proposal, as we emphasized above, is perfectly compatible with RAM, because the logic operation is directly carried out in the basic cell of RAM. Meanwhile, the proposed 1MTJ-1T cell can be integrated with MTJ stacking vertically on the drain of the CMOS through silicon vias and metals, bringing almost no extra area cost. In contrast, some proposals may be compatible with RAM, such as resistive switching nonvolatile logic (RS-NVL) containing a pre-charge sense amplifier, a CMOS logic tree and NVM units, but these schemes bring extra complexity, latency and power consumption [32]. Although RS-NVL has good integrability, the complexity brought by intermediate circuits hinders its prospects. For some other proposals, such as 2 memristors and 1 load resistor or the rectified TMR device, an additional load resistor or diode are required, which is not compatible with RAM structure [13, 22, 33]. The load resistor or diode is also harmful to very-large-scale integration [34]. In addition, our proposal can accomplish full 16 Boolean logic operations in two steps, which can reduce the logic operation numbers and improve the efficiency for a certain computation

Table 2 Comparisons between our work and other IMC schemes

Logic unit	1MTJ-1T (this work)	2 RRAMs and 1 load resitor [13]	R-TMR (2 MTJs and 1 diode) [22]	RS-NVL (PCSA+CMOS Tree+2 MTJs) [32]	2 PCMs, 1 load resitor and a switch [33]
Compatible with RAM	Yes	No	No	Yes	No
Vertical integration	Yes	No	No	Yes	No
Logic type	Full logic	IMP	AND/OR/NOR/NAND	AND/XOR	AND/OR

task compared with those proposals realizing partial logic. For example, a half adder constituted by 'XOR' and 'NAND' logic can be efficienctly accomplished, while other schemes require to firstly perform 'XOR' logic operation through the multiple associative operations of 'AND', 'OR', 'NAND', and 'NOR'. Notably, a similar logic implementation scheme based on one RSM unit and one transistor was reported in 2017 [6]. However, compared with STT-MRAM, the endurance and uniformity of RSMs are unsatisfactory because certain randomness if found in the formation and disruption of conductance filament during data writing [5, 35]. Considering that one logic operation consists of two data writing steps, the STT-MRAM with better endurance and uniformity can support massive logic operations, benefiting IMC applications. Moreover, the higher working voltage of RSMs hinders its further application scenarios, such as battery-powered edge-computing devices.

3 Conclusion

In summary, we prove an in-memory logic operation method based on the basic 1MTJ-1T cell. 16 logic operations are experimentally demonstrated with the logic output in-situ stored in the MTJ. The technical factors of the proposed logic schemes are evaluated by SPICE simulations, indicating the high performance of our proposal. Our work outlines the feasibility of IMC application based on the data writing process of 1MTJ-1T basic cell of STT-MRAM.

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Supporting information Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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