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• **Supplementary File** •

Implementation of 16 Boolean Logic Operations Based on One Basic Cell of Spin-Transfer-Torque Magnetic Random Access Memory

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Appendix A The cascaded operation scheme

In the optimized scheme as shown in A1, one of the operands has the same physical state with the output, i. e. MTJ's resistance. Here we take the optimized OR logic as an example. The initial MTJ state serves as operand 'p', while the other operand 'q' is the source voltage V_s. The gate voltage is always high (G = 1), while the top electrode of MTJ is low (T = 0). The final resistance state of MTJ serves as computation result. For input operands (p, q) = (0, 0) (or (1, 0)), there is no current flowing through the NMOS transistor, thus the MTJ will keep its initial AP (or P) state as logic result '0' (or '1'). For logic inputs (p, q) = (0, 1) (or (1, 1)), the transistor is turned on and the flowing current will switch the MTJ from its initial state (whether AP or P) to P state, representing the logic output '1'. The logic result represented by the resistance state of MTJ can further serve as logic input of next computing process. Besides, most of the logic function in the optimized scheme can be realized in 1 step except for NAND and NOR logic.

Table A1 Full Logic Implementation

Logic Function	S 1				S 2			Input p	0	0	1	1
	I	G	T	S	G	T	S	Input q	0	1	0	1
0		1	1	0					0 (3261)[1)]	0 (3261)	0 (3261)	0 (3261)
1		1	0	1					1 (2244)	1 (2244)	1 (2244)	1 (2244)
p		1	$\overline{p}$	p					0 (3261)	0 (3261)	1 (2244)	1 (2244)
q		1	$\overline{q}$	q					0 (3261)	1 (2244)	0 (3261)	1 (2244)
$\overline{p}$ (NOT p)		1	p	$\overline{p}$					1 (2266)	1 (2266)	0 (3305)	0 (3305)
$\overline{q}$ (NOT q)		1	q	$\overline{q}$					1 (2265)	0 (3295)	1 (2265)	0 (3295)
p+q (OR)	p	1	0	q					0 (3275)	1 (2251)	1 (2251)	1 (2251)
pq (AND)	p	1	1	q					0 (3258)	0 (3265)	0 (3271)	1 (2241)
$\overline{p}$+$\overline{q}$ (NAND)	p	1	0	1	p	q	0	Output	1 (2241)	1 (2241)	1 (2248)	0 (3275)
$\overline{p} \cdot \overline{q}$ (NOR)	p	1	1	0	$\overline{p}$	0	$\overline{q}$		1 (2251)	0 (3275)	0 (3268)	0 (3278)
$\overline{p}$+q (IMP)	q	1	p	1					1 (2254)	1 (2260)	0 (3265)	1 (2241)
p+$\overline{q}$ (RIMP)	p	1	q	1					1 (2251)	0 (3275)	1 (2265)	1 (2251)
$\overline{p}$q (RNIMP)	q	1	p	0					0 (3291)	1 (2251)	0 (3305)	0 (3305)
p$\overline{q}$ (NIMP)	p	1	q	0					0 (3258)	0 (3268)	1 (2241)	0 (3275)
p$\overline{q}$+$\overline{p}$q (XOR)	p	q	p	$\overline{p}$					0 (3265)	1 (2241)	1 (2241)	0 (3275)
pq+$\overline{p} \cdot \overline{q}$ (XNOR)	p	$\overline{q}$	p	$\overline{p}$					1 (2265)	0 (3275)	0 (3275)	1 (2251)

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† Yan Huang and Kaihua Cao have the same contribution to this work.
1) The number in the brackets denotes the resistance of MTJ, dimension: Ω.

Appendix B Details of the MTJ's SPICE model

The STT-p-MTJ model is open-source resource of Spinlib, as mentioned in the main text [1]. The key parameters is listed in the Table B1.

Table B1 Key Parameters of STT-p-MTJ

Parameter	Value
MTJ diameter	50 nm
Thickness of oxide barrier	0.8 nm
Thickness of free layer	1 nm
Resistance-area product	7.8 $\Omega \cdot \mathrm{um}^2$
Resistance of P state	3.98 kΩ
TMR	100%
Critical switching current AP-P	50 μA
Critical switching current P-AP	75 μA
Temperature	300 K

Appendix C Comparison with standard CMOS logic

The proposed 1MTJ-1T logic scheme is non-volatile with little static power and the computation results are in-situ stored. Here, we take NAND logic as an example and compare our proposal with standard CMOS operation containing logic computation under 14 nm node and data transfer as well as storage in STT-MRAM. As shown in Table C1, our proposal can sharply decline the area cost compared with the CMOS logic. For logic inputs (p,q) = (0,0), the step S2 (i. e. writing step) possesses no option, for $V_g = 0V$ and thus consumes no energy. As a result, the proposed 1MTJ-1T logic operation will cost less than half energy but achieve the faster speed than CMOS logic. The situation would be similar for logic inputs (0,1) and (1,0). For logic inputs (1,1), though the step S2 cost more energy than S1, the total energy cost and time delay are still less than CMOS logic.

Table C1 The Comparison for NAND Logic Between 1MTJ-1T and Standard CMOS Logic

NAND Logic		Area	Power			Speed		
(p,q)=(0,0)	CMOS (4T)	2.1 um^2	Read	Computation	Storage	Read	Computation	Storage
			1.4 pJ	1.01 aJ	1.1 pJ	2.8 ns	10 ps	2.15 ns
	1MTJ-1T	0.2 um^2	Preset	Writing		Preset	Writing	
			1.1 pJ	0		2.15 ns	2.15 ns	
(p,q)=(1,1)	CMOS (4T)	2.1 um^2	Read	Computation	Storage	Read	Computation	Storage
			1.4 pJ	4.39 aJ	1.3 pJ	2.8 ns	10 ps	2.4 ns
	1MTJ-1T	0.2 um^2	Preset	Writing		Preset	Writing	
			1.1 pJ	1.3 pJ		2.15 ns	2.4 ns	

References

1 Zhang Y, Zhao W, Lakys Y, et al. Compact modeling of perpendicular-anisotropy CoFeB/MgO magnetic tunnel junctions. IEEE Trans. Electron Devices, 2012, 59(3):819–826