SCIENCE CHINA
Information Sciences

• PROGRESS •

June 2023, Vol. 66 160411:1–160411:7
https://doi.org/10.1007/s11432-023-3752-3

Special Topic: Two-Dimensional Materials and Device Applications

From lab to fab: path forward for 2D material electronics

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Received 7 March 2023/Accepted 24 April 2023/Published online 17 May 2023

Abstract The increasing demand for computation requires the development of energy-efficient logic devices with reduced dimensions. Owing to their atomic thickness, 2D semiconductors are expected to provide possible solutions at the sub-1 nm technology node. Furthermore, taking advantage of the van der Waals nature, the low-temperature back-end of line integration with silicon may occur in the near future. In this perspective, vital progress in material synthesis, device engineering, and integration technologies toward integrated circuits based on 2D materials is reviewed. The challenges and important milestones on the roadmap for the next decade toward the fab adoption of 2D materials are outlined. Particularly, performance, power, area, cost, and equipment for further technology development in this area are proposed as key metrics and enablers.

Keywords two-dimensional materials, transition-metal dichalcogenides, equipment, integrated circuits, roadmap

Citation Ning H K, Yu Z H, Li T T, et al. From lab to fab: path forward for 2D material electronics. Sci China Inf Sci, 2023, 66(6): 160411, https://doi.org/10.1007/s11432-023-3752-3

1 Introduction

Semiconductor device technologies are the cornerstone of the modern information society. From the first integrated circuit (IC) to fin field-effect transistor (FinFET)-based chips, Moore's law has a long history of more than six decades experiencing the happy scaling era (1960s–1990s), the equivalent scaling era (1990s–2020s), and the heterogeneous scaling era (2020s∼). In the next few years, the commercial complementary metal-oxide-semiconductor (CMOS) technology is expected to reach the sub-2 nm node, where the gate length is projected to be 12 nm with a 42 nm gate pitch [1]. It is apparent that the planar geometry will soon reach its physical limitations, and further advances in IC technology will require innovations from materials to 3D architectures. According to the latest international roadmap for devices and systems [1], 2D semiconductors, particularly transition-metal dichalcogenides (TMDCs), are considered promising channel materials to extend the scaling roadmap. After just more than a decade of research, 2D semiconductors already show compelling advantages in scaling below 1 nm nodes as well as low-temperature 3D back-end of line (BEOL) integration. We believe that the next decade will be critical for the transition of this technology from lab to fab.

In this perspective, we review the key milestones in the development of TMDC materials, devices, and integration technology in the past decade outline challenges and set near- and long-term targets toward fab adoption of TMDC at the sub-1 nm node. Furthermore, we propose balanced performance, power, area, cost, and equipment as key metrics for further technology development in this area.

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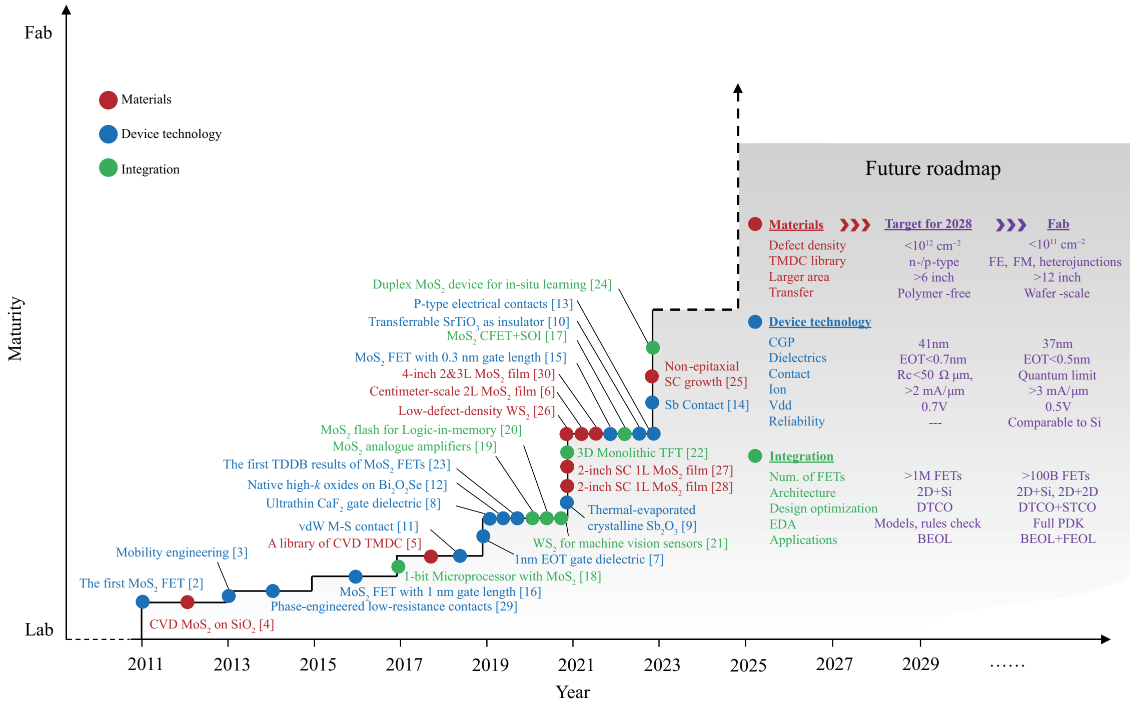

Figure 1 (Color online) Milestones and future roadmaps for 2D semiconductor electronics. CVD: chemical vapor deposition; vdW: van der Waals; CFET: complementary FET; SOI: silicon-on-insulator; EOT: equivalent oxide thickness; SC: single-crystal; TFT: thin-film transistor; TMDC: transition-metal dichalcogenides; FE: ferroelectrics; FM: ferromagnetics; CGP: contacted gate pitch; M: million; B: billion, DTCO: design technology co-optimization; STCO: system technology co-optimization; BEOL: back-end-of-line; FEOL: front-end-of-line; PDK: process design kit; and EDA: electronic design automation.

2 Current status of TMDC-based electronics

Since the first monolayer MoS_2 transistor was demonstrated in a laboratory [2], many important milestones have been achieved in TMDC-based electronics (Figure 1 [2–30]). Early research on TMDCs mainly adopted mechanically exfoliated few-layer or monolayer flakes, which were only appropriate for the demonstration of device prototypes. It was revealed early on that even exfoliated TMDCs had a large number of defects (mainly sulfur vacancies), leading to hopping transport and low mobility [3, 31]. The first breakthrough at the material level was utilizing the chemical vapor deposition (CVD) method to synthesize large-area TMDCs [4], allowing the researchers to throw away the scotch tape and fabricate device arrays. Following this pioneering work, considerable progress has been made to increase the material size (4 inches), library ($\sim$47 materials) [5], crystallinity (2-inch single crystal), quality (defect density $\sim 10^{12}$ cm^{-2}), precise control of the number of layers [6], and heterostructures [32–35].

Interface engineering, dielectric integration, and Ohmic contact have been the focus of 2D field effect transistor (FET) device research, leading to comprehensive improvements in device performance, power consumption, reliability, and uniformity. Recently, Intel [36–39], TSMC [40–44], and Interuniversity Microelectronics Centre (IMEC) [45–48] have initiated research and development on 2D materials. However, despite their efforts, the density of interface states (D_{it}) is still more than an order of magnitude higher than that of silicon. The absence of dangling bonds in the 2D interface makes dielectric integration a considerable challenge. Recent advances in sub-1 nm EOT dielectric integration include using monolayer molecular crystals as atomic layer deposition (ALD) buffer layers [7, 8], thermal-evaporated crystalline Sb_2O_3 [9], and high-κ perovskite membranes [10], which realized interfaces with lower D_{it} and oxides with higher dielectric constant. Another alternative to classical ALD is van der Waals (vdW) integration, which is used to deposit dielectrics such as hBN [11] and crystalline CaF_2 [49]. Furthermore, Li et al. [12] reported the native oxide high-κ dielectric bismuth selenite (Bi_2SeO_5), which can be obtained by layer-by-layer oxidation of the 2D semiconductor Bi_2O_2Se. The native oxidation method avoids any 2D/dielectric interface exposure and thus forms a high-quality interface. The challenge of achieving Ohmic contact is due to the existence of the vdW gap, which hinders the formation of high-quality alloy contacts, unlike silicide in silicon. Nonetheless, progress has been made using transferred electrodes to

realize the Schottky-Mott limit [50], low-temperature evaporated vdW contacts [13, 49, 51], and more recently, semimetallic Bi [52] and Sb contacts [14]. We have recently reported Sb (01$\bar{1}$2) contact technology and achieved a near-quantum-limit R_c of 42 $\Omega \cdot \mu$m, which was lower than that of Si CMOS [14]. In addition to the progress in single device performance, variation, and yield, the reliability of multiple devices is also critical for technology development, which attracts increasing attention particularly from the industry of semiconductor [13, 53].

Effective switching for channel lengths as small as sub-1 nm is shown by 2D transistors [16, 54, 55], demonstrating their potential toward end-of-roadmap scaling. IMEC and Intel have reported that the CGP of 2D semiconductor transistors can be reduced to ∼40 nm, meeting the requirements of sub-1 nm nodes [37, 45]. Stacked multibridge channels and vertically stacked complementary FETs (CFET) can be implemented to further increase device density while improving electrostatics [16, 17, 53, 55–58]. For ICs, recent breakthroughs include the 1-bit MoS_2 microprocessor unit [18], the first 2D MoS_2 analog amplifiers [19], and other logic circuits [59], demonstrating the possibility of 2D semiconductors in logic and analog circuits. Also, 2D semiconductor memory [17, 20, 60] and non-von Neumann architecture [18, 21, 61] have opened up exciting new avenues for computing, memory, and sensing applications. Furthermore, 2D materials can be integrated with mature technology through monolithic 3D integration. To this end, IMEC demonstrated the heterogeneous BEOL integration of 2D semiconductors with FinFETs on a 300-mm wafer [62]. A 2D semiconductor thin-film transistor matrix was also 3D-integrated with GaN to realize high-resolution micro-light emitting diode (LED) displays [22, 59, 63].

3 Challenges and future roadmap

3.1 Materials and equipment

For fab adoption of 2D semiconductors, single-crystal wafers approaching 12 inches are highly desirable. Commercial metal-organic chemical vapor deposition (MOCVD) can potentially meet the size requirement but still faces fundamental problems with organic sources that lead to carbon contamination, low growth rates, and small grain sizes. For CVD, solid sources are inherently less controllable. Thus, large-scale uniformity is the key issue that requires custom-designed equipment and precisely controlled growth processes beyond lab tube furnaces. To this end, combining the volatile inorganic precursors and the flow and temperature field designs of MOCVD can be an acceptable strategy. Meanwhile, engineering growth substrates to achieve unidirectionally aligned domains and subsequent seamless merging remain an important area of research [64]. We expect 6–8-inch single-crystal TMDC wafers (presumably n-type MoS_2) to be available by 2028 following the development of growth equipment as well as large-area sapphire wafers. To realize complementary devices and ICs, p-type TMDC (such as WSe_2) single-crystal wafers of the same size will also be required. Going further with the material library, we expect that wafer-scale 2D ferroelectrics, ferromagnetics, and even heterostructures will likely be developed for logic-memory-sensing multifunctional integration.

The transfer of TMDCs from the growth substrate to silicon circuitry is a crucial step for 3D integration given that direct growth under low thermal budgets still faces challenges in delivering high-quality materials. Existing transfer approaches rely on polymer or metal films as media which inevitably leave residues and have compatibility issues. Complete polymer-free, dry-transfer techniques are highly desirable and remain to be developed. The transfer needs to be compiled with a 12-inch wafer and deliver excellent uniformity, ideally under vacuum conditions to reduce surface contamination as much as possible. The dry transfer method proposed by IMEC, which realized a 300 mm wafer-scale uniform transfer with lase debonding and is highly compatible with commercial foundry processes, should be a milestone accepted by the industrial community [65].

It has been clear that the growth and transfer of 2D materials toward fab adoption require customized equipment that is not currently available. This is a vastly underdeveloped area that can set back the timetable from lab to fab. Thus, we call for more efforts in developing scaled tools to be integrated with silicon lines.

3.2 Device technology

For transistor building blocks, we emphasize that it is important to co-optimize performance, power, and area instead of just focusing on a singular aspect down the path. According to the international

roadmap for devices and systems (IRDS) roadmap, the drive current is estimated to be 3 mA/μm at $V_{\rm dd}$ = 0.5 V for the sub-1 nm node, which requires synergistic optimization of material quality, contact, channel length, EOT, and 3D multilayer stacking. Contact resistance is the key to high-performance FETs. Recent studies have already pushed the contact resistance close to the quantum limit using the semimetallic Sb (01$\bar{1}$2) [14] and Y-induced phase transition [66]; therefore, we suggest that contact uniformity and ultrascaled contact footprint should be focused on in future work. For the sub-1 nm node, the quantum-limited Rc should be achieved when the effective contact length is as small as 15 nm. Based on previous work, the transfer length of 2D TMD can be reduced to 2 nm or less [38, 45]. Recent contact technologies with semimetallic Sb and Y-doped phase transitions have further reduced the contact resistance close to the quantum limit, which will be the cornerstone for the extremely small-scale contact footprint. Moreover, similar to carbon nanotubes and graphene, 2D TMDs are expected to achieve efficient carrier injection through edge contacts, which is expected to be an ultrascaled footprint solution. Furthermore, doping-free contact technology with reduced parasitic resistance will be necessary for high-frequency operation. For power consumption, it is important to realize ultrathin EOT with low D_{it}. From the IRDS roadmap, the EOT is expected to be $<$ 0.5 nm with an optimal dielectric/2D material interface. Damage-free interface engineering (i.e., molecular seeding layers, low-energy nonALD evaporation, polymer-free dry transfer, and equipment providing an insert/vacuum environment) and vdW integration of high-κ dielectrics are promising solutions to obtain D_{it} comparable to silicon ($\sim 10^{10}$ cm$^{-2}\cdot$eV^{-1}).

CFET should be adopted as the basic building block of 2D ICs as it can further reduce the footprint. However, one of the bottlenecks of 2D CFET is the relatively weak performance of p-type transistors. It can be overcome by improving the performance of p-type transistors or adopting more stacking layers of p-type materials. Furthermore, the integration technology of CFET through multilayer stacking requires self-alignment, selective, self-limiting deposition and etching techniques, which are the key engineering challenges.

The key requirements of any commercial technology are wafer-scale variation, reliability, and yield; however, they have only received limited attention so far due to the relative immaturity of 2D technology [13, 23, 54]. IMEC proposed typical test vehicles for 2D devices for state-of-the-art process nodes [67]. A specific process flow of manufacturing technology with self-alignment processes and multibridge channels needs to be developed in the future. We suggest more joint efforts between academia and the better-equipped industry to evaluate these aspects before adopting 2D technology for large-scale fabrication.

3.3 Integration

Beyond a single device, the integration of 2D FETs poses stringent requirements on the number of FETs, chip architecture, design optimization, and EDA tools. While state-of-the-art demonstrations have integrated only 10^2–10^3 FETs on one chip, we expect an increase of several orders in magnitude by 2028. Currently, silicon-based FEOL is in optimal power, performance, area, cost (PPAC) balance, while the front-end process for ultrascaled 2D semiconductors still exhibits some issues. Therefore, we believe that BEOL heterogeneous integration will flourish in a relatively short term given the wide range of unique properties of 2D materials. However, vdW stacking of 2D semiconductors is inherently suitable for low-temperature integration, and back-end integration helps leverage the advantages of both technologies, improving the performance and functionality of front-end chips at a lower cost.

The design capability must also keep pace with 2D IC development. Design technology co-optimization (DTCO), a software-based methodology to accelerate process development with reduced cost and time has already become a routine in Si advanced technology nodes but is rarely explored in 2D materials. As a short-term goal, academia and industry should prioritize the development of manufacturing processes and accelerate the construction of DTCO and EDA platforms (i.e., TCAD, circuit design, and lithography mask design) for 2D materials. In the future, full process design kits specifically for 2D ICs, co-optimization of system and technology for 2.5D and 3D integration in more advanced nodes, and further material-to-system co-optimization to broaden the optimization space are expected to be developed.

High-performance computing is still an important application scenario for 2D ICs. With the potential of ultrascaled nodes and monolithic 3D, 2D ICs are expected to achieve high-performance computing and energy efficiency. Additionally, 2D ICs are also being used in advanced memory, in-memory computing,

novel display technologies, and other fields. The unique properties of 2D ICs make them promising candidates for a wide range of applications, and ongoing research is expected to lead to the development of innovative technologies.

3.4 Neuromorphic computing

AI has already become an integral part of our lives, but existing hardware (such as GPUs and ASICs) is based on the von Neumann architecture and is considerably energy-intensive. Neuromorphic computing, based on the non–von Neumann architecture, shows considerable promise in improving the energy efficiency of AI computation and 2D materials due to their rich properties in this area. Recently, we reported a tunable duplex device structure based on a MoS_2 ferroelectric FET [24], which exhibited excellent performance in both training and inference, leading to the development of a training-inference-in-one hardware architecture for in situ machine learning and edge intelligence. Although still in its early stages, neuromorphic computing based on 2D materials exhibits many exciting potentials, such as the 3D integration of physical stacking multilayer DNNs and sensitive response for in-sensor computing.

Acknowledgements This work was supported by National Key R&D Program of China (Grant Nos. 2022YFB4400100, 2020YFA0309600), National Natural Science Foundation of China (Grant Nos. T2221003, 61927808, 61734003, 61851401, 91964202, 62204124, 62204113, 12104330, 51861145202), Leading-Edge Technology Program of Jiangsu Natural Science Foundation (Grant No. BK20202005), Natural Science Foundation of Jiangsu Province (Grant No. BK20220773), Strategic Priority Research Program of the Chinese Academy of Sciences (Grant No. XDB30000000), Fundamental Research Funds for the Central Universities, China (Grant No. 2023300247), Key-Area Research and Development Program of Guangdong Province (Grant No. 2020B0101340001), Key Laboratory of Advanced Photonic and Electronic Materials, and Collaborative Innovation Center of Solid-State Lighting and Energy-Saving Electronics.

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