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Special Topic: Two-Dimensional Materials and Device Applications

A novel negative quantum capacitance field-effect transistor with molybdenum disulfide integrated gate stack and steep subthreshold swing for ultra-low power applications

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Abstract Various steep-slope devices based on novel structures and mechanisms garnered considerable attention for their potential in ultra-low power logic applications. In this work, a novel steep-slope negative quantum capacitance field-effect transistor (NQCFET) with molybdenum disulfide (MoS_2)-integrated gate stack was realized by theoretical analysis and experimental evaluation. By combining the MoS_2 equivalent capacitance model calibrated with experimental results, the NQCFET device model is further established. The results demonstrated that the optimized MoS_2-integrated NQCFET can achieve a subthreshold swing (SS) of sub-60 mV/dec over a current range of 5 decades, with the minimum SS reaching 29 mV/dec, indicating the remarkable potential of MoS_2-integrated NQCFETs for ultra-low power applications.

Keywords negative quantum capacitance, molybdenum disulfide, field-effect transistor, subthreshold swing, ultra-low power device

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1 Introduction

Power consumption is one of the biggest challenges in developing integrated circuits. Conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) are limited by the thermal tail of the Boltzmann distribution, resulting in a subthreshold swing (SS) theoretical limitation of 60 mV/dec at room temperature. This makes it difficult to effectively reduce the supply voltage [1–3]. Thus, considerable attention has been paid to ultra-low power devices with a sub-60 mV/dec SS. Numerous researchers have proposed several devices based on innovative structures and mechanisms, such as tunneling field-effect transistors (TFETs) [4–6] and negative capacitance field-effect transistors (NCFETs) [7–9]. TFETs operated via the band-to-band tunneling mechanism exhibit a low off-state current and steep SS. However, due to the low tunneling probability, the on-state current of a Si-based TFET is low [10, 11]. For an NCFET with a ferroelectric material integrated into the gate stack, the negative capacitance (NC) effect introduced by the gate stack can change the coupling relationship between gate voltage and surface potential, achieving ultra-steep SS. However, the physical origin of the NC effect remains controversial. Several explanations for the NC phenomenon, such as quasi-static NC theory [7], time-dependent multi-domain Landau-Ginzburg-Devonshire (LGD) theory [12], and domain-switching delay theory [13], have been proposed. Some of these theories are inconsistent with experimental results, while others lack direct experimental evidence. In addition, the hysteresis characteristics of NCFETs induced by the ferroelectric layer are not preferred and limit their logic applications [14, 15]. Some recent experimental studies on NCFETs have successfully achieved nearly hysteresis-free characteristics [16, 17], but attaining hysteresis-free characteristics under very high frequency operation remains difficult due to the frequency dependence of the NC

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effect [18]. Our previous work has also demonstrated that NCFET hysteresis cannot be fundamentally eliminated, and an optimization trade-off exists between SS and hysteresis [19].

To achieve a steep SS and high on-state current without hysteresis, the negative quantum capacitance (NQC) effect was investigated in this work. The gate capacitance characteristic is a critical component of SS optimization. Quantum effects often gain precedence with the scaling down of electronic devices. Therefore, utilizing these quantum effects to modulate gate capacitance may lead to optimizing the SS of the transistor. The capacitance of a material usually comprises two parts, namely, geometric capacitance (C_{geom}), which is directly related to the area and thickness of the material and always remains positive, and quantum capacitance (C_{q}), which mainly includes kinetic energy capacitance, exchange energy capacitance, and correlation energy capacitance [20]. In materials with strong spin-orbit coupling effects, such as two-dimensional (2D) transition metal disulfides and quasi-three-dimensional (3D) metals [21], a low carrier concentration results in the dominance of both exchange energy and correlation energy over the kinetic energy, resulting in a negative C_{q}. Hence, it is possible to integrate materials that can achieve an NQC effect into the device gate stack to modulate the gate capacitance characteristics for a steeper SS. Very recently, a graphene-based negative quantum capacitance field-effect transistor (NQCFET) with a steep SS has been developed [22].

In this work, a MoS_2 film with a strong spin-orbit coupling effect and low density of states (DOS) is integrated into the MOSFET gate stack, and its C_{geom} and C_{q} are theoretically analyzed and experimentally evaluated. The experimental results indicate that the MoS_2 film can achieve a considerable NQC effect. Furthermore, a MoS_2-integrated NQCFET is proposed, and the device physical model is established to evaluate and optimize its electric characteristics. Simulation results show that the MoS_2-integrated NQCFET can achieve an SS of less than 60 mV/dec over a current range of 5 decades and the minimum SS can reach 29 mV/dec after optimization. This work reveals the remarkable potential of MoS_2-integrated NQCFETs for ultra-low power applications.

2 Materials and methods

Compared with 3D quasi-metals, MoS_2 possesses certain advantages, such as simple chemical components, a mature preparation process, and excellent interface quality [23, 24]. In this work, a MoS_2-integrated metal-oxide-semiconductor capacitor (MOSCAP) was fabricated to analyze its equivalent capacitance and evaluate its potential for steep-slope devices. Its fabrication process is briefly outlined as follows: a 10 nm-thick aluminum oxide (Al_2O_3) dielectric layer was deposited on a silicon (Si) substrate via atomic layer deposition (ALD). Subsequently, chemical vapor deposition (CVD)-grown high-quality multilayered MoS_2 was transferred on the top of the Al_2O_3 layer, following which a 10 nm-thick Al_2O_3 dielectric layer was grown on the MoS_2 via ALD. Finally, a titanium/gold (Ti/Au) electrode was deposited via electron beam evaporation and patterned. A conventional MOSCAP without MoS_2 integration was also fabricated for comparative analysis.

3 Results and discussion

Figures 1(a) and (b) show the schematic diagram of the MoS_2-integrated MOSCAP structure and cross-sectional high-resolution transmission electron microscopy (HRTEM) images, respectively. The X-ray photoelectron spectrum (XPS) of the multi-layer MoS_2 by CVD is shown in Figure 1(c). It can be observed from Figure 1 that the MoS_2-integrated MOSCAP shows a "sandwich" structure (oxide-MoS_2-oxide) with excellent interface quality. Figure 2(a) shows the measured capacitance versus gate voltage (C-V_{g}) curves (1 kHz@300 K) of the MoS_2-integrated MOSCAP and conventional MOSCAP, observing that the total capacitance of the MoS_2-integrated MOSCAP is originally lower than that of conventional MOSCAP. However, as the gate voltage increases, the total capacitance of the MoS_2-integrated MOSCAP gradually exceeds that of the conventional MOSCAP. In other words, the total capacitance of the MoS_2-integrated MOSCAP increases abnormally from the accumulation state to the depletion/weak inversion status. Moreover, the rate of capacitance increment in the subthreshold region is extracted and shown in Figure 2(b). From Figure 2, it can be observed that the gate electrostatic control of the MoS_2-integrated MOSCAP is substantially superior to that of the conventional MOSCAP.

To better understand the phenomenon of anomalous increment of total capacitance for the MoS_2-integrated MOSCAP, theoretical analysis and calculation of MoS_2 equivalent capacitance are investigated.

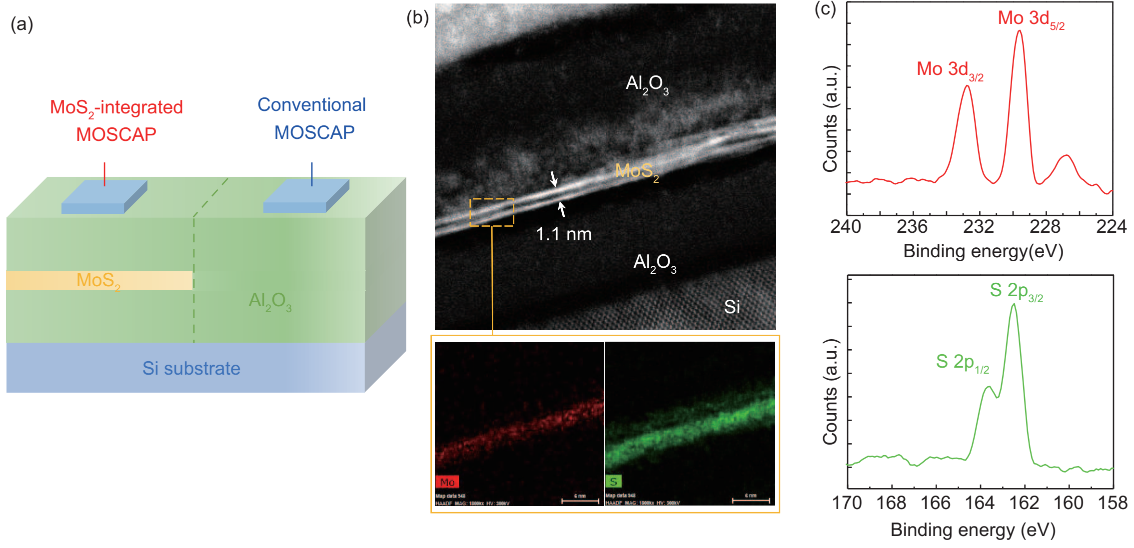

Figure 1 (Color online) (a) Schematic of the MoS_2-integrated MOSCAP and conventional MOSCAP; (b) cross-sectional TEM diagram of the MoS_2-integrated MOSCAP; (c) X-ray photoelectron spectrum (XPS) of the MoS_2 film.

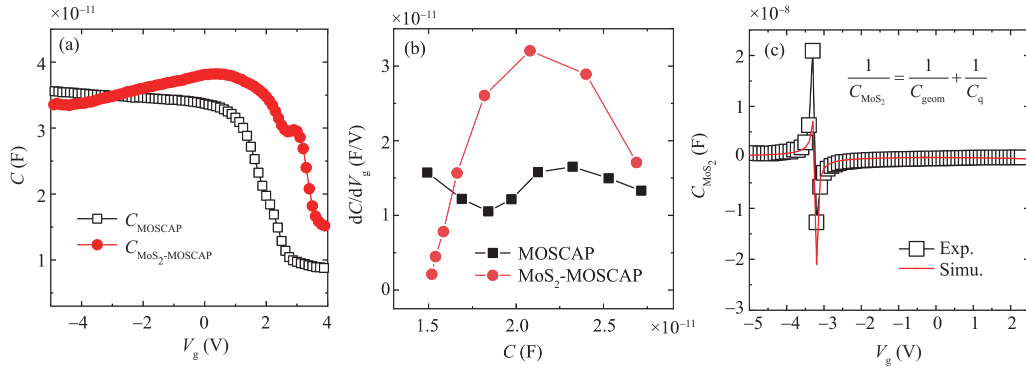

Figure 2 (Color online) (a) Capacitance versus gate voltage (C-V_g) curves of the MoS_2-integrated MOSCAP and conventional MOSCAP; (b) capacitance change rate versus capacitance (dC/dV_g-C) curves of the MoS_2-integrated MOSCAP and conventional MOSCAP; (c) developed MoS_2 equivalent capacitance model in good agreement with experimentally extracted C-V_g data.

For MoS_2, the total energy E can be expressed as [20]

$$E = E_{\mathrm{H}} + \sum_i E_{\mathrm{kin},i} + \sum_i E_{\mathrm{x},i} + \sum_i E_{\mathrm{c},i}, \tag{1}$$

where E_{H} denotes the Hartree energy, which reflects interparticle Coulomb interactions and is related to the classical geometric capacitance C_{geom}, $E_{\mathrm{kin},i}$ is the kinetic energy of the carriers, $E_{\mathrm{x},i}$ is the exchange energy between different carriers, and $E_{\mathrm{c},i}$ is the correlation energy between different carriers. The above three kinds of energy are related to the kinetic energy capacitor (C_{kin}), exchange energy capacitor (C_{x}), and correlation energy capacitor (C_{c}), respectively. C_{geom}, C_{kin}, C_{x}, and C_{c} can be expressed as [20]

$$C_{\mathrm{geom}} = \frac{\varepsilon}{d}, \tag{2}$$

$$C_{\mathrm{kin}} = \mathrm{e}^2\rho, \tag{3}$$

$$C_{\mathrm{x}} = -\varepsilon_0(2\pi)^3\varepsilon_{\mathrm{eff}}\sqrt{n}, \tag{4}$$

$$\frac{1}{C_{\mathrm{c}}} = \frac{a_0 a_{\mathrm{B}} r_{\mathrm{s}}^2}{4\varepsilon_0\varepsilon_{\mathrm{eff}} y}\left[-\frac{3}{32}u + \left(1+\frac{3}{4}u\right)\frac{x}{y} + (1+u)\left(\frac{x^2}{y^2} - \frac{z}{y}\right)\right], \tag{5}$$

$$\begin{aligned} \frac{1}{C_{\mathrm{MoS_2}}} &= \frac{1}{C_{\mathrm{geom}}} + \frac{1}{C_{\mathrm{kin}}} + \frac{1}{C_{\mathrm{x}}} + \frac{1}{C_{\mathrm{c}}} \\ &= \frac{\varepsilon_{\mathrm{eff}}\varepsilon_0}{d} + \frac{a_{\mathrm{B}}}{4m_0\varepsilon_0} - \frac{1}{(2\pi)^{2/3}\varepsilon_{\mathrm{eff}}\varepsilon_0\sqrt{n-n_0}} - \frac{a_{\mathrm{B}} a_0 r_{\mathrm{s}}}{4\varepsilon_{\mathrm{eff}}\varepsilon_0}, \end{aligned} \tag{6}$$

where ε, ε_0, ε_{eff} and d refer to the dielectric constant, vacuum dielectric constant, effective dielectric constant, and thickness of the material, respectively. e refers to the elementary charge, ρ is the DOS of the material, n_0 is the initial carrier concentration, m_0 is the effective mass of the carrier, n is the carrier concentration, r_{s} is the dimensionless number describing the interaction between particles, a_{B} is the Bohr radius, and u, x, y, and z are polynomial functions about r_{s}.

Thus, besides the conventional geometric capacitance, the MoS_2 capacitance includes kinetic energy capacitance, exchange energy capacitance, and correlation energy capacitor as shown in (6), and the quantum capacitance C_{q} is equal to the series value of these three capacitors. Moreover, from the above expression, the geometric capacitance and kinetic energy capacitance are always positive, and the exchange energy capacitance and correlation energy capacitance are always negative. This indicates that the quantum capacitance can be negative when exchange energy and correlation energy dominate, resulting in a possible negative MoS_2 capacitance. A large DOS and a high carrier concentration lead to dominant kinetic energy and the contribution of exchange energy and correlation energy to C_{q} can be negligible. However, a small DOS and a low carrier concentration result in kinetic energy decay, and the contribution of exchange energy and correlation energy to C_{q} becomes substantial in this case.

MoS_2 exhibits a strong spin-orbit coupling effect and large exchange and correlation energy contributions. Moreover, as a typical 2D material, it exhibits lower DOS than 3D materials. The capacitance of MoS_2 is experimentally extracted and compared with the theoretically equivalent capacitance model, as shown in Figure 2(c), illustrating that the simulated data are in good agreement with experimental data, indicating that the anomalous increment in total capacitance originated from the NQC effect of the MoS_2 layer.

Based on the experimental demonstration of the NQC effect in the MoS_2 film and the capacitance characteristics of the MoS_2-integrated MOSCAP, the MoS_2 film was further integrated into the MOSFET gate stack to construct the NQCFET device. Figure 3(a) shows the device structure diagram. It should be mentioned that the proposed NQCFET and floating-gate transistors are fundamentally different. Floating-gate transistors are generally used as flash memory, where the tunneling layer between the channel and the capture layer is generally thin for charge trapping [25, 26]. However, the NQCFET utilizes the NQC effect of the MoS_2 layer to achieve steeper SS for logic applications. In the NQCFET, the relationship between quantum capacitance C_{q} and chemical potential μ is as follows [27]:

$$k = \frac{1}{n^2} \cdot \frac{\partial n}{\partial \mu} = \frac{1}{n^2} \cdot \frac{C_{\text{q}}}{\text{e}^2}, \tag{7}$$

where k is the compressibility that reflects the change in chemical potential μ caused by the change in carrier concentration n, and the compressibility is determined by quantum capacitance. As an example, the energy band diagram of the N-type NQCFET is illustrated in Figure 3(b). When the gate voltage is small, the electron concentration in MoS_2 is low, the electron exchange energy and correlation energy dominate, and thus, the quantum capacitance C_{q} is negative. With the increase of gate voltage, the electron concentration in MoS_2 increases, and the decrease in the chemical potential of MoS_2 provides the channel with additional voltage to increase the surface potential. When the increment of the surface potential exceeds the increment of the gate voltage, the SS of the device can be below 60 mV/dec at room temperature.

To evaluate and optimize the characteristics of the MoS_2-integrated NQCFET, a physical device model was established. Figure 3(d) shows the device modeling framework, where the NQCFET can be regarded as a MoS_2 capacitor and a conventional MOSFET in series. The MoS_2 capacitance model is based on the calibrated MoS_2 equivalent capacitance model. The voltage on the gate of the underlying MOSFET is defined as the internal node voltage V_{int}. Based on the voltage-charge and voltage-current relationships of the MOSFET, the charge conservation relationship and the voltage division law are combined as constraints for simulation until the transfer characteristics of the NQCFET can be obtained in a self-consistent solution.

Here, the gate voltage amplification factor A_{V} is used to evaluate the SS optimization of the NQCFET (Eq. (8)). To achieve a higher SS of the NQCFET, A_{V} is expected to be large enough.

$$\text{SS}_{\text{NQCFET}} = \frac{\text{d}V_g}{\text{d}V_{\text{int}}} \cdot \left(\frac{\text{d}V_{\text{int}}}{\text{d}\psi_s} \frac{\text{d}\psi_s}{\text{dlog}I_d}\right) = \frac{1}{A_{\text{V}}} \cdot \text{SS}_{\text{MOSFET}}, \tag{8}$$

$$\text{SS}_{\text{NQCFET}} = \left[1 + C_{\text{s}}\left(\frac{1}{C_{\text{geom}}} + \frac{1}{C_{\text{q}}} + \frac{1}{C_{\text{Al}_2\text{O}_3}}\right)\right] \cdot 60 \text{ mV/dec}, \tag{9}$$

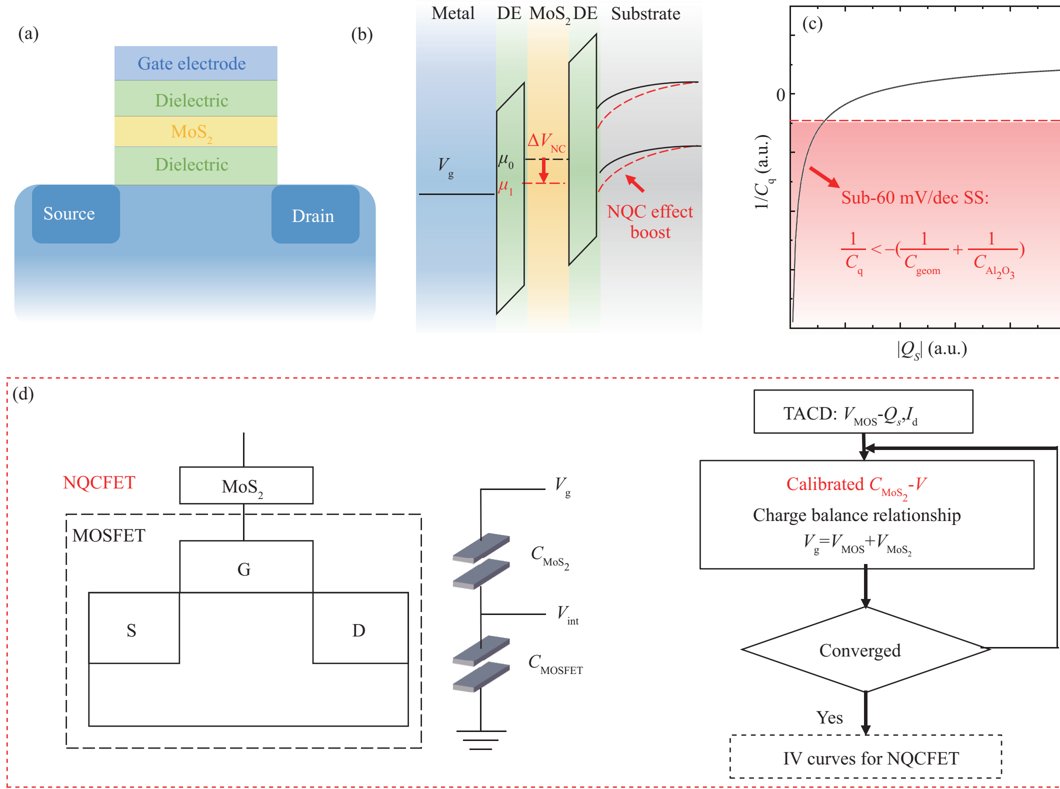

Figure 3 (Color online) (a) Schematic diagram of the NQCFET; (b) energy band diagram of the N-type NQCFET along the gate stack direction; (c) quantum capacitance matching condition for sub-60 mV/dec SS of the NQCFET (the red dashed line denotes the negative of the reciprocal of the total capacitance of MoS_2 geometric capacitor and alumina capacitor in series); (d) modeling framework of the NQCFET device.

$$C_{\rm q}^{-1} < -(C_{\rm geom}^{-1} + C_{\rm Al_2O_3}^{-1}). \tag{10}$$

To make the SS of the NQCFET less than 60 mV/dec (Eq. (9)), there exists an optimal region for the quantum capacitance $C_{\rm q}$ (Eq. (10)). From (10), to obtain an NQCFET with a steep sub-60 mV/dec SS, the absolute value of quantum capacitance $C_{\rm q}$ must be smaller than the series value of geometric capacitance $C_{\rm geom}$ and conventional gate dielectric (Al_2O_3) capacitance when the NQC effect occurs, as shown in Figure 3(c). From the material properties, it is an effective method to regulate the effective dielectric constant and the initial carrier concentration to regulate quantum capacitance $C_{\rm q}$. Figure 4 shows the transfer characteristic ($I_{\rm d}$-$V_{\rm g}$) curves and the gate voltage amplification factor characteristic ($A_{\rm V}$-$V_{\rm g}$) curves of the NQCFET with different effective dielectric constants and different initial carrier concentrations. It can be observed that the low effective dielectric constant and relatively high initial carrier concentration can improve the SS of the NQCFET.

Figures 5(a)–(c) show the transfer characteristics, gate voltage amplification factor characteristics, and the extracted SS of the NQCFET after parameter optimization, respectively. The optimized NQCFET can achieve a large gate voltage amplification factor of 4.54 with a high on-state current of 160 μA, while the on-state current of the conventional MOSFET is only 19 μA. Moreover, the NQCFET can reach a minimum SS of 29 mV/dec, which is 54% lower than the SS of the conventional MOSFET (63 mV/dec). The NQCFET can maintain an SS of less than 60 mV/dec over a current range of 5 decades. The results indicate that the NQCFET has great potential for ultra-low power applications. In addition, unlike ferroelectric materials, since the materials with the NQC effect only have one stable status under a zero-bias condition, the NQCFET can theoretically achieve hysteresis-free characteristics, which is very promising for ultra-low power logic applications.

4 Conclusion

Utilizing innovative structures and physical mechanisms to achieve a sub-60 mV/dec SS at room temperature for the device is one of the most effective means to solve the power consumption problem. In

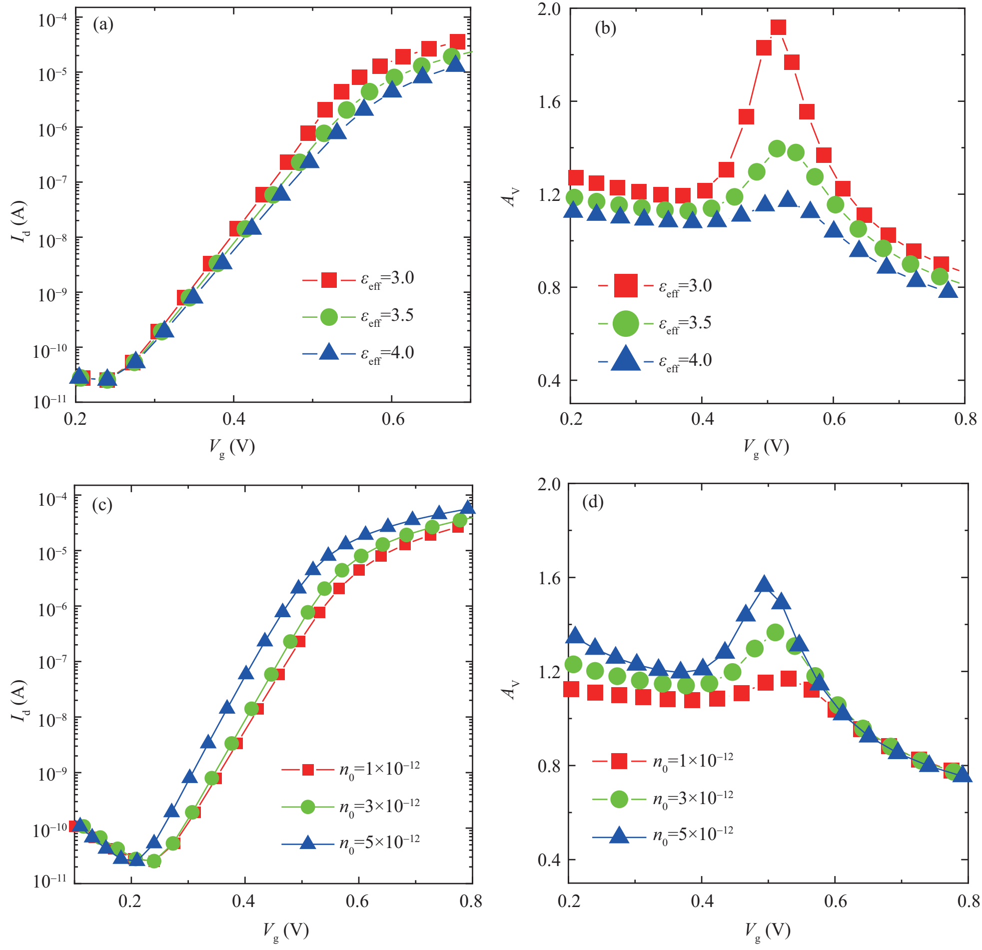

Figure 4 (Color online) (a) Transfer characteristics of NQCFETs with different effective dielectric constants; (b) gate voltage amplification characteristics of NQCFETs with different effective dielectric constants; (c) transfer characteristics of NQCFETs with different initial electron concentrations; (d) gate voltage amplification characteristics of NQCFETs with different initial electron concentrations.

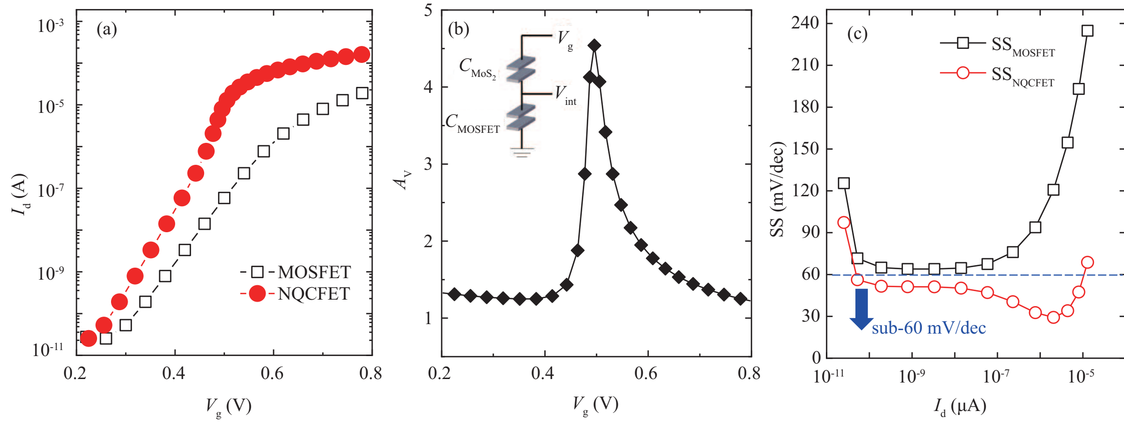

Figure 5 (Color online) (a) Transfer characteristics of the simulated MOSFET and NQCFET after optimization; (b) the gate voltage amplification characteristics extracted from the simulation; (c) simulated results of SS versus drain current in NQCFET.

this work, based on the NQC effect, a novel MoS_2-integrated steep-slope device, referred to as NQCFET, was proposed. A MoS_2-integrated MOSCAP was designed and experimentally fabricated to evaluate the NQC effect of the MoS_2 film. An abnormal increment of total capacitance in the depletion/weak inversion status indicated that the NQC effect is effective in modulating the gate capacitance characteristics for steep SS. Furthermore, by combining the calibrated MoS_2 capacitance model with the MOSFET model,

the NQCFET device model was established to evaluate and optimize the device properties. The simulation results showed that the SS of the NQCFET can be lower than 60 mV/dec over a current range of 5 decades, and the minimum SS can reach 29 mV/dec at room temperature. The steeper SS within the large drain current range and the high on-state current of the NQCFET have indicated its remarkable potential for ultra-low power applications.

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