SCIENCE CHINA
Information Sciences

June 2023, Vol. 66 160402:1–160402:10
https://doi.org/10.1007/s11432-023-3751-y

• REVIEW •
Special Topic: Two-Dimensional Materials and Device Applications

# Recent progress of layered memristors based on two-dimensional $MoS_2$

Wei TONG & Yuan LIU*

*Key Laboratory for Micro-Nano Optoelectronic Devices of Ministry of Education, School of Physics and Electronics, Hunan University, Changsha* 410082*, China*

Received 15 February 2023/Revised 25 March 2023/Accepted 24 April 2023/Published online 18 May 2023

**Abstract** Memristors are memory-capable electronic components that consist of two terminals and a switching layer, whose resistance can be adjusted by an applied bias voltage. Two-dimensional (2D) materials with ultrathin layered structures are used as switching layers to overcome the limitations of traditional resistive materials in reducing the memristor sizes, demonstrating their potential in memory, flexible electronics, neuromorphic computing, and other related fields. Particularly, $MoS_2$ is widely used as a representative 2D semiconductor, and the $MoS_2$-based memristors have been intensively studied. In this review article, we have summarized the recent progress of $MoS_2$-based memristors, including the fabrication process, device structure, device performance, switching mechanism, and synaptic applications. In addition, we also discussed the prospects and challenges for their future development.

**Keywords** memristor, switching mechanism, $MoS_2$, 2D materials

**Citation** Tong W, Liu Y. Recent progress of layered memristors based on two-dimensional $MoS_2$. Sci China Inf Sci, 2023, 66(6): 160402, https://doi.org/10.1007/s11432-023-3751-y

## 1 Introduction

Memristors have attracted considerable interest in the field of neuromorphic computing, because they have unique capabilities such as high-density integration, fast write and read speeds, and compatibility with the complementary metal oxide semiconductor process [1–12]. Particularly, the data can be input and output just by changing the high and low resistance states (HRS/LRS) of the device. Its original state remains unchanged after the bias voltage is removed, thus facilitating non-volatile memory [1]. Several material systems can exhibit memristive behavior, including conventional resistive materials ($HfO_2$, CuS, and $TiO_2$) and novel two-dimensional (2D) materials [13–15]. Compared to conventional resistive materials, 2D materials have superior electronic, optical, and mechanical properties even at an atomic level thickness [16,17], enabling 2D-materials-based memristors to have properties like low power switching [18–22], electrostatic gate tunability [23], and mechanical flexibility [16]. 2D memristors have also been used to emulate artificial synapses that can mimic basic synaptic functions such as short-term synaptic plasticity (STP), long-term synaptic plasticity (LTP), and spike-time-dependent plasticity (STDP) [18–22,24,25].

Although several 2D materials have been investigated as candidates for the memristive layer, including 2D semiconductors (SnSe, $MoS_2$, and $WSe_2$) and 2D insulators (BN) [14], $MoS_2$ is the most widely studied 2D material owing to its distinctive band structure, high environmental stability, high carrier mobility, and ease of exfoliation and fabrication. The band structure of $MoS_2$ can be tuned by varying its thickness. Its bandgap increases to 1.8 eV at single-layer thickness [26]. Recent reports have shown low leakage currents in $MoS_2$-based memristors with few layers, enabling the demonstration of sub-1 nm thickness of the switching layer [16] and a SET voltage less than 0.2 V [27]. Additionally, $MoS_2$ memristors exhibit excellent properties even at temperatures over 350°C [20], potentially expanding their applications to harsh environments.

In this review, we have first described the device structures and fabrication processes for $MoS_2$-based memristors. This is followed by a description of the working mechanisms and an analysis of its electrical

* Corresponding author (email: yuanliuhnu@hnu.edu.cn)

 

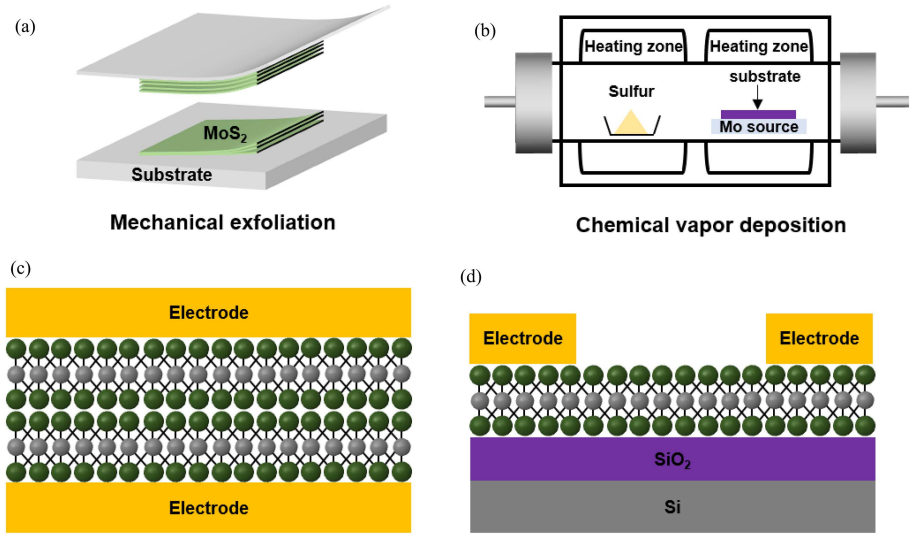


**Figure 1** (Color online) (a) Schematic of $MoS_2$ mechanical exfoliation process with the assist of tape; (b) schematic of CVD, where Mo source reacts with a sulfur source to deposit $MoS_2$ on the substrate; (c), (d) schematic illustration of vertical and lateral $MoS_2$ memristor.

properties. These devices can largely be classified into metallic-filament-based, vacancy-migration-based, Schottky-emission-and-direct-tunneling-modulation (SE&DT modulation)-based, and phase-transition-based memristors, depending on the conduction mechanisms involved in their operation. Finally, we concluded with an overview of the current challenges and prospects of $MoS_2$-based memristors and noted that the device structures and working mechanisms also applied to other 2D materials other than $MoS_2$.

## 2 Device structures and fabrication processes

Various methods have been used to synthesize $MoS_2$, including mechanical exfoliation [28–30], liquid phase exfoliation (LPE) [21, 31, 32], and chemical vapor deposition (CVD) [16, 17, 20, 27]. Generally, mechanical exfoliation and CVD growth are the two most widely used approaches for fabricating $MoS_2$-based transistors (Figures 1(a) and (b)) due to the high material quality achieved with minimal defects. However, given that unlike in transistors, the existence of defects or vacancies could also enhance the performance of memristors by facilitating filament formation and resistance switching, high-performance $MoS_2$ memristors can also be achieved using the LPE approach [32].

From the structural point of view, $MoS_2$-based memristors can be classified into two major categories, vertically and laterally structured memristors, as illustrated in Figures 1(c) and (d), respectively. In vertically structured devices, the $MoS_2$ layers are sandwiched between a top electrode (TE) and a bottom electrode (BE), with the vertical distance determined by the thickness of $MoS_2$ layer (in the range of nanometers). Hence, the switching voltage could be reduced significantly by thinning $MoS_2$ layer [16, 20, 21, 27]. Although the vertical structure offers the potential for high-density integration, the atomically thin channels being completely encapsulated between TE and BE during device operation makes it relatively difficult to observe the switching dynamics. Therefore, irreversible damage due to the use of a focused ion beam (FIB) is usually necessary to adequately prepare the sample for characterization using a transmission electron microscope (TEM), which then can only provide the cross-sectional information [20, 29]. In the laterally structured memristors, the switching layer is defined by the lateral metal electrodes, just like in field-effect transistors [33]. Furthermore, given that the $MoS_2$ channels are exposed owing to the lateral structure, the switching dynamics can be directly observed without any appreciable damage to the device. An example of such a study is the one by Sangwan et al. [23], which demonstrated sulfur vacancy migration along grain boundaries (GBs) in the $MoS_2$ memristive layer. Direct examination of the lateral device under TEM [34] can help to build a physical model of the memristor operation. However, the size of laterally structured devices is typically larger than that of vertically structured memristors, leading to large switching voltages.

## 3 Electrical properties and conduction mechanism

Based on their respective device structures, electrodes, and fabrication technologies, $MoS_2$ memristors exhibit different switching mechanisms. These can be largely divided into metallic-filament-based, vacancy-migration-based, SE&DT-modulation-based, phase-transition-based, and other mechanism-based memristors.

### 3.1 Metallic-filament-based $MoS_2$ memristors

Metallic filament formation is one of the major mechanisms involved in the switching behavior of $MoS_2$ memristors. These memristors usually use active metals (Cu and Ag) as electrodes, and their resistance is modulated by metallic filament formation and rupture [20, 21, 27, 35, 36]. For example, Xu et al. [27] reported a vertical device using a bilayer of $MoS_2$ as the memristor layer, with Cu and Au as the TE and BE, respectively, as shown in Figure 2(a). The device could operate under an ultra-low SET voltage ($V_{\rm SET}$) of 0.2 V and an ultra-low RESET voltage ($V_{\rm RESET}$) of −0.15 V (Figure 2(b)) due to the ultrathin switching layer and the low Cu ion migration barrier. The switching mechanism is initiated by the formation of a Cu filament shown in Figure 2(c). When a sufficiently positive bias is applied to the Cu electrode, an oxidation reaction occurs at the Cu/$MoS_2$ interface, where the Cu atoms are oxidized, and the resulting Cu ions migrate into the $MoS_2$ layer. With a sufficient accumulation of Cu in the switching layer, Cu filaments eventually connect the TE and BE, resulting in a "switch" from the HRS to the LRS. Alternatively, if a negative bias is applied, the conductive filament cross-sectional area decreases, and the resistance switches back to HRS. Furthermore, the device has been shown to emulate the STDP function at switching voltages below 0.2 V, indicating its potential in future low-power neuromorphic computing.

Ranganathan et al. [20] reported a device with high thermal stability that brings us closer to potential applications of $MoS_2$ memristors in high-temperature electronics, such as in aerospace, automotive, oil, and gas industries. Their memristor was composed of a large-scale $MoS_2$ sandwiched between Ag and heavily doped Si as shown in Figure 2(d). Bipolar switching was demonstrated at a high working temperature of 350°C, with low $V_{\rm SET}$ and $V_{\rm RESET}$ (Figure 2(e)). Additionally, both the LRS and HRS values exhibited thermostable retention performance, reaching $2 \times 10^4$ s without degradation (Figure 2(f)). However, the operation voltage is affected by the temperature, which decreases with increasing temperatures due to the phenomena involving the diffusion of Ag ions. Scanning TEM characterization reveals that resistive switching can be explained by Ag ion migration and filament formation, similar to Cu/$MoS_2$/Au devices [27]. Moreover, the memristive device also demonstrated LTP behavior with a low power consumption of 7 nW. Feng et al. [21] reported a vertical $MoS_2$ memristor using Ag as electrodes, which exhibits an ultra-low standby power consumption of 1 fW. Additionally, due to the photosensitivity of $MoS_2$, the resistance can be modulated by the laser power variation, which provides the possibility for future application of optical-stimulation integration [20].

### 3.2 Vacancy-migration based $MoS_2$ memristors

In addition to metallic filament formation, vacancy migration is another major mechanism for $MoS_2$-based memristors. These memristors usually use graphene (Gr), inert metals (Au and Pt), and relatively active metals (Ti and Ta) as electrodes. For example, Wang et al. [29] reported a van der Waals (vdW) heterojunction-based memristor, using Gr as the electrode and $MoS_{2-x}O_x$ as the switching layer. As compared to the metal electrodes mentioned earlier, graphene is significantly chemically inert, and the covalently bonded carbon atoms cannot diffuse into the $MoS_{2-x}O_x$ layer [37, 38]. Therefore, the observed resistance switching behavior is primarily based on sulfur vacancy migration and concentration [29]. These devices demonstrated excellent performance with an endurance of $10^7$ cycles, a retention time of $10^5$ s, and switching speeds of less than 100 ns. Moreover, these devices also show lower cycle-to-cycle variation as compared to metallic-filament-based memristors [20, 29], which could be largely attributed to the vdW contact between the $MoS_{2-x}O_x$ switching layer and the Gr electrode. Recent research has demonstrated that the vdW metal integration process could avoid the damage from conventional high-energy metal deposition processes, and improve the interface quality with minimum defects and metal diffusion, which is critical for the device endurance and reducing cycle-to-cycle variation [39–43].

$MoS_2$ memristor arrays based on vacancy migration can also be fabricated at wafer-scale [32]. To fabricate this device, uniform $MoS_2$ films are deposited by spin-coating, which results in several defects along the edges of the $MoS_2$ nanosheets due to it being a solution-based process. The electron energy

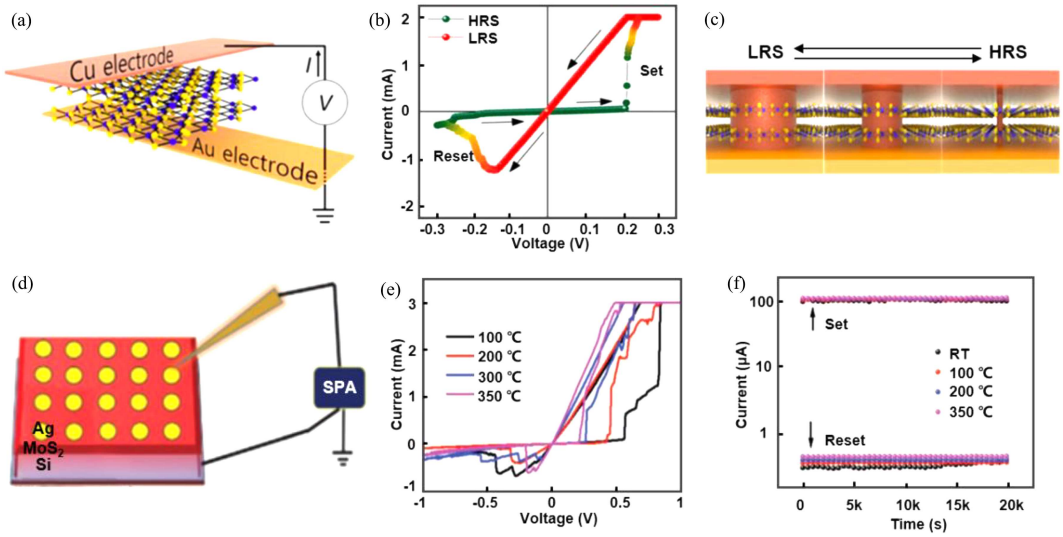


**Figure 2** (Color online) (a) Device structure of Cu/bilayer $MoS_2$/Au memristor [27]; (b) *I*-*V* output curve of a typical memristor with a low $V_{SET}/V_{RESET}$ of 0.2/−0.15 V [27]; (c) schematics of the Cu filament formation and rupture during the operation process [27] Copyright 2019 American Chemical Society. (d), (e) Schematic of Ag/$MoS_2$/Si memristor and the corresponding *I*-*V* switching characteristics under different temperatures [20]; (f) retention tests of the LRS and HRS under different temperatures, demonstrating non-affected retention time of $2 \times 10^4$ s [20] Copyright 2020 Wiley.

loss spectroscopy shows that the switching behavior can be explained by sulfur vacancy diffusion assisted by the edge defects, as shown in Figure 3(a). In the SET process, sulfur vacancies migrate toward the BE (Pt), eventually forming conductive vacancy filaments in the edge region of the nanosheet, resulting in the resistance switching to LRS (Figure 3(b)). In the RESET process, conductive filaments rupture as S vacancies migrate toward the top contact (Ti), and the resistance switches back to HRS (Figure 3(b)). Because the filaments are confined to the edge of the nanosheet, more uniform conductive paths could be realized with smaller $MoS_2$ nanosheets. Therefore, devices with small $MoS_2$ nanosheets exhibit low cycle-to-cycle and device-to-device variations. Moreover, the devices demonstrate a high endurance of $10^7$ cycles, fast switching speeds of 40 ns, and an excellent retention time of 10 years. Particularly, the device conductance can achieve a high degree of linear symmetry by applying enhanced and suppressed pulses (Figure 3(c)), which is beneficial to map the weight of the algorithm to the device conductance. This helps achieve a high image recognition accuracy of 96%, as was demonstrated in $MoS_2$ memristor arrays, shown in Figure 3(d).

### 3.3 SE&DT-modulation-based $MoS_2$ memristors

The previous $MoS_2$ memristors (metallic filament and vacancy) were all based on few or multi-layer $MoS_2$. Recently, Ge et al. [16] reported an atomic level memristor with vertical Au/single-layer $MoS_2$/Au structure (Figure 4(a)). The memristive layer of this device is a monolayer $MoS_2$ with an ultimate thickness of 0.7 nm; hence, low operation voltage could be realized (1 V for $V_{SET}$ and −1.25 V for $V_{RESET}$, Figure 4(b)). Based on the *I*-*V* characteristics at different temperatures, the switching behavior can be attributed to modulation between the SE and DT. At LRS, the current is linear with voltage and increases with decreasing temperature (Figure 4(c)) in agreement with the DT model [44]. At HRS, the current is nonlinear with voltage and increases with increasing temperature (Figure 4(d)), which is consistent with the SE model [44]. Additionally, the SE&DT modulation-based memristor exhibits good mechanical flexibility by maintaining a resistive switching behavior over 1000 bending cycles (Figure 4(e)), which is essential to future flexible and wearable electronics.

Apart from high flexibility, Kim et al. [17] demonstrated that monolayer $MoS_2$ memristors are also suitable for energy-efficient radio-frequency switching. Due to the ultrathin thickness of the memristive layer (monolayer), $MoS_2$ memristors show low resistance and a high cutoff frequency of about 10 THz for sub-$\mu m^2$ switches (Figure 4(f)). However, the endurance of the monolayer $MoS_2$ devices is only about 150 cycles, which may not be enough for practical applications. The poor endurance could be attributed to the electrode evaporation process being directly performed on the memristive layer, which causes considerable damage to the interface as well as metal diffusion into the channel [41–43]. This interface

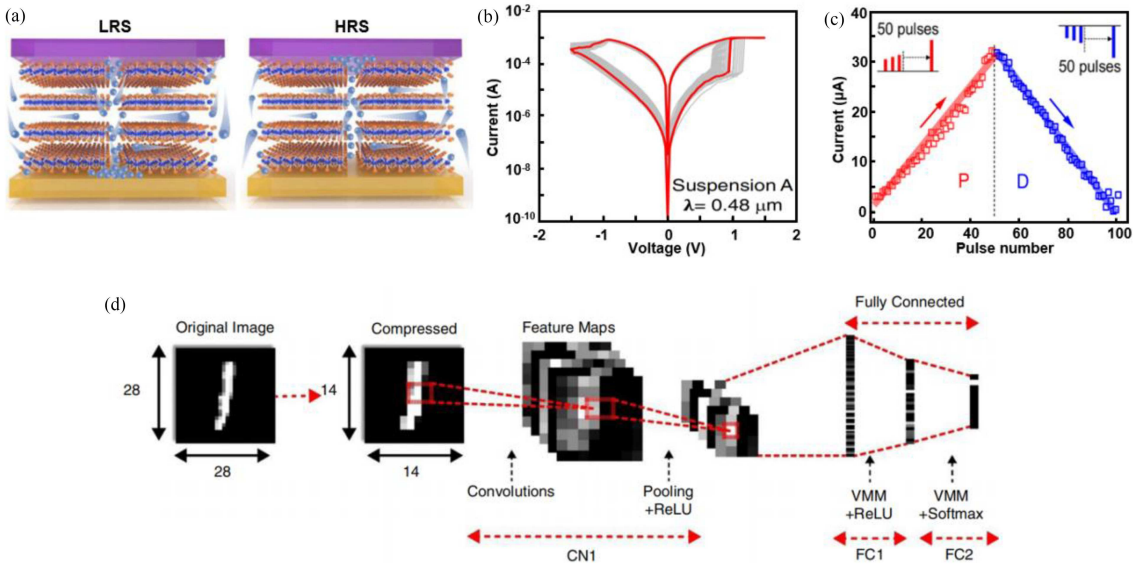


**Figure 3** (Color online) (a) Schematics of the SET (left) and RESET process (right), where S vacancy filament forms and ruptures along the $MoS_2$ edges [32]; (b) 200 representative *I-V* curves of the corresponding $MoS_2$ memristors, demonstrating small cycle-to-cycle variations [32]; (c) synaptic function of potentiation and depression [32]; (d) convolutional neural network simulation, consisting of 1 convolution layer and 2 fully connected layers [32] Copyright 2022 Springer Nature.

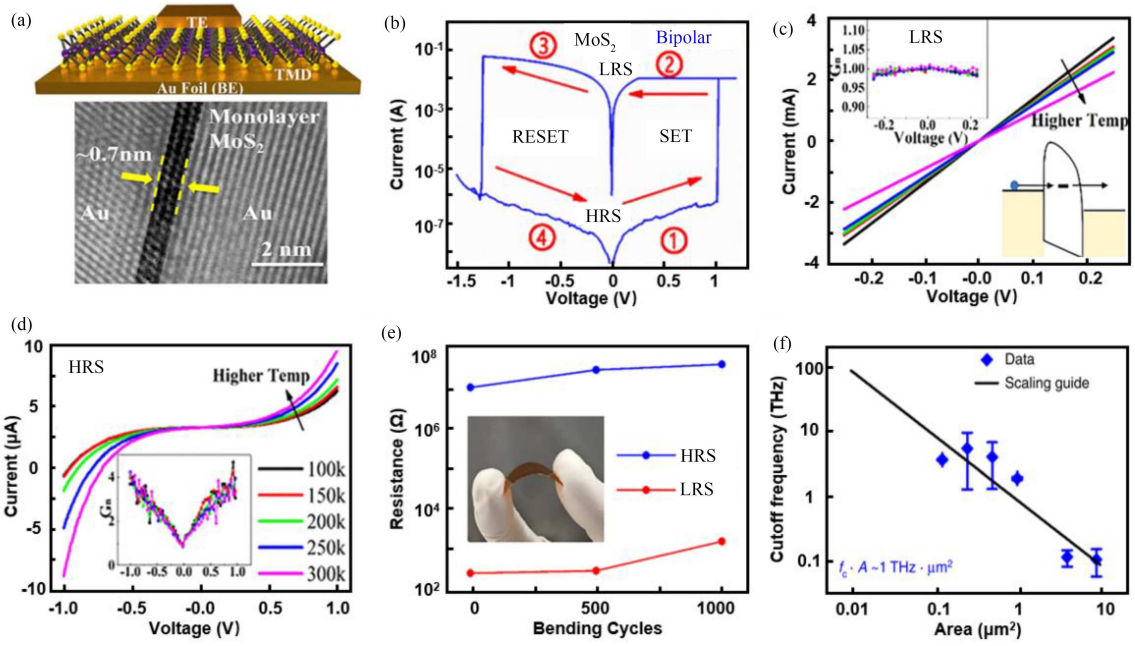


**Figure 4** (Color online) (a) Schematic and TEM image of Au/single-layer $MoS_2$/Au memristor [16]; (b) *I-V* curve of typical monolayer $MoS_2$ devices with a $V_{SET}/V_{RESET}$ of 1/−1.25 V [16]; (c), (d) *I-V* characteristics of LRS and HRS at different temperatures, the current linearly decreases as the temperature increases at LRS (c) and nonlinearly increases as the temperature increases at HRS (d) [16]; (e) HRS and LRS values after repeated mechanical bending at 1% strain for 1000 times [16] Copyright 2018 American Chemical Society. (f) Cutoff frequency of the memristors in different sizes [17] Copyright 2018 Springer Nature.

damage could be critical for monolayer $MoS_2$ memristor, where the interface is the entire device.

### 3.4 Phase-transition-based $MoS_2$ memristors

In addition to the conventional 2H phase (semiconducting phase) $MoS_2$, 1T phase (metallic phase) $MoS_2$ has also been explored for memristors. Cheng et al. [31] reported a phase-transition-based $MoS_2$ memristor using Ag electrodes, as shown in Figure 5(a). 1T phase $MoS_2$ nanosheets were fabricated by LPE [45], consisting of 92.5% 1T phase and 7.5% 2H phase $MoS_2$, as shown in Figure 5(b). The structure of the

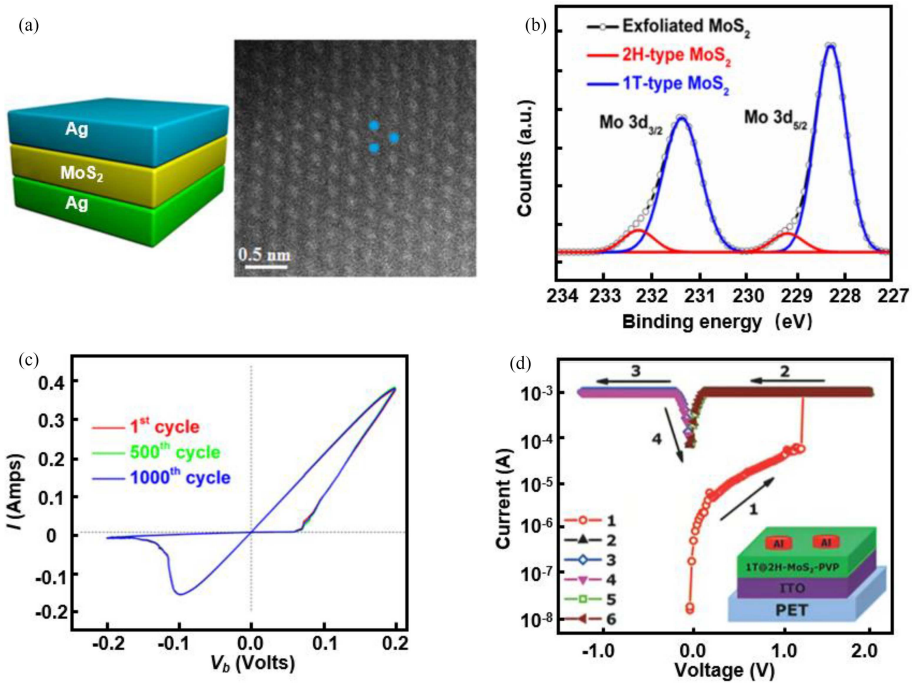


**Figure 5** (Color online) (a) Schematic of Ag/$MoS_2$/Ag structure memristor (left) and high-angle annular dark field scanning TEM (HAADF-STEM) image of $MoS_2$ with 1T phase (right) [31]; (b) X-ray photoelectron spectroscopy for the exfoliated, 2H-phase and 1T-phase $MoS_2$ nanosheets [31]; (c) typical *I*-*V* characteristic of the Ag/1T $MoS_2$/Ag device, with ultra-low $V_{SET}$/$V_{RESET}$ of 0.1/−0.1 V [31] Copyright 2016 American Chemical Society. (d) Schematic of Al/$MoS_2$-PVP/ITO memristor and its typical *I*-*V* characteristic [47] Copyright 2016 Wiley.

1T phase was subject to change under an external electric field. By applying a positive voltage, the lattice structure is distorted, and the conduction band overlaps the valence band, leading to increased conductivity. In contrast, the application of negative voltage causes a gap to be generated between the conduction and valence bands, decreasing the conductivity of the $MoS_2$ layer, and the device is reset to HRS. Owing to the unique conducting nature of 1T $MoS_2$ [46], the devices exhibit lower $V_{SET}$ and $V_{RESET}$ (0.1 V for $V_{SET}$ and −0.1 V for $V_{RESET}$) compared to previous devices based on 2H phase $MoS_2$ and excellent memristive behavior with small fluctuation of the $V_{SET}$ and $V_{RESET}$ during 1000 sweep cycles, as shown in Figure 5(c). Moreover, Zhang et al. [47] also reported a vertical $MoS_2$ memristor based on the phase transition, which is fabricated on a flexible substrate as shown in Figure 5(d). The device exhibits higher endurance over $10^4$ cycles and greater mechanical flexibility than Ag/$MoS_2$/Ag memristors.

Although vertical phase-transition-based memristors have been reported, there is a lack of directly observed characterization data for the switching dynamics. Zhu et al. [30] overcame this limitation with lateral $MoS_2$ memristors, where phase transition behavior could be confirmed by atomic force microscope (AFM). The memristor was composed of horizontally lithiated 1T′ phase $MoS_2$ and Au electrodes, exhibiting a large endurance of 1000 cycles and a retention time of over 7000 s. After immersing in n-butyl lithium solution, $MoS_2$ was maintained in the 1T′ phase with a resistance three orders of magnitude lower than that of the 2H phase [48]. The switching mechanism is attributed to the phase transition induced by Li ions migration. In the forming process, by applying a negative voltage, Li ions diffuse toward the left electrode, leading to a transition from the 1T′ to the 2H phase (LRS to HRS). In the following SET and RESET processes, $MoS_2$ film underneath the right electrode reversibly switches between the 1T′ and 2H phases, and the thickness of the $MoS_2$ film also changes. Moreover, synaptic cooperation and synaptic competition behavior are also demonstrated in this phase transition device. For adjacent synaptic devices, the potentiation of one synaptic device will activate the adjacent device. The synaptic competition can prevent an infinite potentiation of synaptic, in which an increase in the degree of potentiation in one synapse leads to the reduction of the other. The cooperation and synaptic competition mechanisms of synapses could stabilize the balance between potentiation and depression, which are important for future biological networks.

**Table 1** Summary of key device parameter of different $MoS_2$ memristors

| Structure | TE/BE | Mechanism | $V_{SET}/_{RESET}$ (V) | Endurance (cycle) | Retention (s) | $I_{ON}/I_{OFF}$ | Synaptic | Ref. |
|---|---|---|---|---|---|---|---|---|
| Vertical | Au/Au | SE&DT | 1/−1.25 | $1.5\times10^2$ | $10^6$ | $10^4$ | – | [16, 17] |
| Vertical | Ag/Si | Metallic filament | 0.3/−0.3 | $10^2$ | $2\times10^4$ | 10 | LTP | [20] |
| Vertical | Ag/Ag | Metallic filament | 0.18/−0.3 | $10^2$ | $4\times10^4$ | $10^7$ | STP, LTP | [21] |
| Lateral | Au/Au | GB | 8.3/−10 | – | – | $10^3$ | – | [23] |
| vertical | Cu/Au | Metallic filament | 0.2/−0.15 | 20 | $1.8\times10^4$ | 10 | LTP, STDP | [27] |
| Vertical | Gr/Gr | Vacancy migration | 1/−1 | $2\times10^7$ | $10^5$ | $10^2$ | – | [29] |
| Lateral | Au/Au | Phase transition | 6/−6 | $10^3$ | $7\times10^3$ | 10 | LTP | [30] |
| Vertical | Ag/Ag | Phase transition | 0.1/−0.1 | $10^3$ | – | $10^3$ | – | [31] |
| Vertical | Ti/Pt | Vacancy migration | 1/−1 | $10^7$ | 10 years | $10^2$ | LTP | [32] |
| Vertical | Al/ITO | Phase transition | 1.24/– | $10^4$ | $6\times10^2$ | $10^2$ | – | [47] |
| Lateral | Cr/Cr | Charge trapping | 8/−8 | $8\times10^3$ | $10^3$ | $10^3$ | – | [50] |
| Vertical | Ti/Au | Interface mediation | 2.5/−3 | $10^3$ | $3\times10^2$ | 10 | LTP | [54] |

### 3.5 Other $MoS_2$ memristors

In addition to the above mechanisms, the resistance switching behavior is also related to many other factors, such as GB [23,49], charge trapping [50–52], and interface mediation [53,54]. In 2015, Sangwan et al. [23] reported a lateral memristor using single-layer $MoS_2$ as a memristive layer and Au as electrodes. The switching mechanism is based on the migration and accumulation of S vacancies near the GB, resulting in a resistance change. GB could be classified into three types, which include intersecting, bridging, and bisecting. Among them, intersecting GB-based memristor exhibits a higher on/off ratio of about $10^3$ and lower $V_{SET}$ less than 10 V, compared to other types of GB. Moreover, these lateral devices allow the *I-V* characteristics to be controlled by the gate. Therefore, the $V_{SET}$ and $V_{RESET}$ can be adjusted, which provides new capabilities for memristor applications.

In addition to the back-gate structure mentioned above, floating-gate memristors have also been reported by Vu et al. [50]. These devices exhibit larger on/off ratios of over $10^3$ than the lateral $MoS_2$ memristors mentioned earlier, a higher switching speed of 0.5 ms, and a more reliable endurance of over 8000 cycles. The switching performances could be explained by the charge-trapping-based mechanism. In the RESET process, by applying a negative voltage, electrons are trapped to Gr with the formation of a negative field, driving out the majority carriers from the $MoS_2$ channel. In the SET process, holes are trapped in Gr by a positive voltage, leading to an increase in the electron concentration in the $MoS_2$ channel. These devices also could be fabricated on flexible substrates with the on/off ratio maintained under a large strain of up to 1%.

Krishnaprasad et al. [54] reported a vertical $MoS_2$ device with Ti and Au as BE and TE, respectively. The devices exhibited low cycle-to-cycle and device-to-device variability, with a coefficient of variation of 0.32 and 1.7%, respectively. The high switching uniformity observed in $MoS_2$ devices is attributed to the interface mediation between the $MoS_2$ and Ti. Due to the presence of Ti contact metal, the Ti/$MoS_2$ interface acts as a reservoir of O vacancies, which promotes the ion migration and the formation of conductive paths in the SET/RESET process. Moreover, the control samples with Au electrodes showed high variability, which further confirmed that Ti/$MoS_2$ interface is critical for switching uniformity.

Finally, here we summarize the characteristics of $MoS_2$ memristors discussed above, as shown in the summary Table 1.

## 4 Challenges and prospects

Although significant research has been achieved, challenges still exist. From the performance point of view, increasing the endurance is highly desirable. Currently, most $MoS_2$ memristors can only demonstrate a limited number of switching cycles (in the range of hundreds of cycles) [16, 17, 20, 21, 27, 51], which is not large enough for practical application. Additionally, relatively large cycle-to-cycle and device-to-device variations are also observed in $MoS_2$ memristors [16, 49]. The poor endurance and large variability could originate from the stochastic nature of ion transport [55]. Switching behavior is usually attributed to ion motion, where uncontrollable ions expand the active area by migrating to new locations during each cycle, leading to inevitable device damage and ultimate device failure. Therefore, new methods are needed to

control the ion motion, such as confining ions in defined paths by threading dislocations of SiGe [56] or nanopore Gr layer [57]. Additionally, a non-ideal interface between metal electrodes and $MoS_2$ memristive layer is also a critical factor affecting device endurance and variability [29,41–43]. The non-ideal interface is due to the destruction of the delicate 2D lattice that was damaged during the high-energy evaporation process [39–42]. Moreover, by reducing the $MoS_2$ thickness, this non-ideal interface could be increasingly more critical and eventually leads to device failure due to the short circuit between TE and BE [41]. On the other hand, vdW metal integration, in which metal electrodes are physically laminated onto 2D surfaces, has demonstrated atomically clean interfaces with minimized surface disorder [40]. Therefore, the vdW metal lamination technique could maintain the intrinsic properties of a 2D delicate lattice and is expected to reduce the variation and improve the endurance. Recently, Li et al. [41] have demonstrated InSe memristors using double side vdW lamination technique, exhibiting longer endurance and smaller switching variations compared to the evaporation-based memristors. Although $MoS_2$-based memristors using double-sided vdW metals are not demonstrated, similar performance improvement is expected.

From the mechanism point of view, understanding the operating process of the memristor's switching mechanism is critical to the research field. For example, although filament formation (both metallic or vacancy) is proposed as the major work mechanism for $MoS_2$-based memristors [20,27,29,32], the direct visualization of the filament formation is very challenging because memristors typically have a vertical sandwich structure and the filament is fully encapsulated between the TE and BE during operation process [55]. To overcome this limitation, FIB has been utilized to cut the sample and exposes the filament cross-section, and the memristor can be further observed under TEM [20,29]. However, cross-sectional TEM only provides one-dimensional line information in a limited area, and crucial filament regions may be largely missed during the sample thinning process [55,58]. Recently, scanning tunneling microscope and AFM tip have been used as the TE, and the filament formation or rupture can be simultaneously observed with larger area [23,30,59]. However, with this method, only the tip region is biased, which is far from the real situation of device operation. Therefore, there is currently a pressing need for the characterization of filament formation in practical devices.

From the application point of view, some progress has also been made in simulating artificial synapses by $MoS_2$ memristors, which can realize the basic synaptic functions such as LTP, STP, and STDP [27,30,32,60]. High-performance neuromorphic computational simulation based on the small-scale $MoS_2$ memristor arrays has been demonstrated [32], indicating low power consumption and high speed of the devices. However, the small-scale $MoS_2$ memristor arrays can only realize the linear classification of simple data, which is far from the complex and varied practical application requirements. To further increase the integration scale of memristors, it is critical to improve the uniformity, stability, and large-scale fabrication process. For example, there is still a lack of a method to achieve controlled preparation of $MoS_2$ with high film quality, desired thickness, and uniform surface over large areas, and the performance of $MoS_2$ devices is largely influenced by the number of layers and crystallinity. Additionally, the crosstalk in memristor arrays also restricts its scalable integration. Given the short history of $MoS_2$ and memristors, we believe the high-performance device and application demonstrations will continue to expand in breadth and depth.

**Acknowledgements** This work was supported by National Key R&D Program of China (Grant No. 2021YFA1200503) and National Natural Science Foundation of China (Grant Nos. 51991340, 51991341, 52221001, U22A2074).

**References**

1 Strukov D B, Snider G S, Stewart D R, et al. The missing memristor found. Nature, 2008, 453: 80–83
2 Xia Q, Yang J J. Memristive crossbar arrays for brain-inspired computing. Nat Mater, 2019, 18: 309–323
3 Lee M J, Lee C B, Lee D, et al. A fast, high-endurance and scalable non-volatile memory device made from asymmetric $Ta_2O_{5-x}/TaO_{2-x}$ bilayer structures. Nat Mater, 2011, 10: 625–630
4 Yao P, Wu H, Gao B, et al. Fully hardware-implemented memristor convolutional neural network. Nature, 2020, 577: 641–646
5 Yang J J, Strukov D B, Stewart D R. Memristive devices for computing. Nat Nanotech, 2013, 8: 13–24
6 Prezioso M, Merrikh-Bayat F, Hoskins B D, et al. Training and operation of an integrated neuromorphic network based on metal-oxide memristors. Nature, 2015, 521: 61–64
7 Zidan M A, Strachan J P, Lu W D. The future of electronics based on memristive systems. Nat Electron, 2018, 1: 22–29
8 Ielmini D, Wong H S P. In-memory computing with resistive switching devices. Nat Electron, 2018, 1: 333–343
9 Lastras-Montaño M A, Cheng K T. Resistive random-access memory based on ratioed memristors. Nat Electron, 2018, 1: 466–472
10 Kumar S, Strachan J P, Williams R S. Chaotic dynamics in nanoscale $NbO_2$ Mott memristors for analogue computing. Nature, 2017, 548: 318–321
11 Rehn D A, Reed E J. Memristors with distorted structures. Nat Mater, 2019, 18: 8–9

12 Wang Z, Joshi S, Savel'ev S E, et al. Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. Nat Mater, 2017, 16: 101–108
13 Sun K, Chen J, Yan X. The future of memristors: materials engineering and neural networks. Adv Funct Mater, 2017, 31: 2006773
14 Huh W, Lee D, Lee C H. Memristors based on 2D materials as an artificial synapse for neuromorphic electronics. Adv Mater, 2020, 32: 2002092
15 Shi T, Wang R, Wu Z, et al. A review of resistive switching devices: performance improvement, characterization, and applications. Small Struct, 2021, 2: 2000109
16 Ge R, Wu X, Kim M, et al. Atomristor: nonvolatile resistance switching in atomic sheets of transition metal dichalcogenides. Nano Lett, 2018, 18: 434–441
17 Kim M, Ge R, Wu X, et al. Zero-static power radio-frequency switches based on $MoS_2$ atomristors. Nat Commun, 2018, 9: 2524
18 Lu X F, Zhang Y, Wang N, et al. Exploring low power and ultrafast memristor on p-type van der Waals SnS. Nano Lett, 2021, 21: 8800–8807
19 Li S, Pam M E, Li Y, et al. Wafer-scale 2D hafnium diselenide based memristor crossbar array for energy-efficient neural network hardware. Adv Mater, 2022, 34: 2103376
20 Ranganathan K, Fiegenbaum-Raz M, Ismach A. Large-scale and robust multifunctional vertically aligned $MoS_2$ photomemristors. Adv Funct Mater, 2020, 30: 2005718
21 Feng X, Li Y, Wang L, et al. A fully printed flexible $MoS_2$ memristive artificial synapse with femtojoule switching energy. Adv Electron Mater, 2019, 5: 1900740
22 Yan X, Zhao Q, Chen A P, et al. Vacancy-induced synaptic behavior in 2D $WS_2$ nanosheet-based memristor for low-power neuromorphic computing. Small, 2019, 15: 1901423
23 Sangwan V K, Jariwala D, Kim I S, et al. Gate-tunable memristive phenomena mediated by grain boundaries in single-layer $MoS_2$. Nat Nanotech, 2015, 10: 403–406
24 Shi Y, Liang X, Yuan B, et al. Electronic synapses made of layered two-dimensional materials. Nat Electron, 2018, 1: 458–465
25 Lei P, Duan H, Qin L, et al. High-performance memristor based on 2D layered BiOI nanosheet for low-power artificial optoelectronic synapses. Adv Funct Mater, 2022, 32: 2201276
26 Splendiani A, Sun L, Zhang Y, et al. Emerging photoluminescence in monolayer $MoS_2$. Nano Lett, 2010, 10: 1271–1275
27 Xu R, Jang H, Lee M H, et al. Vertical $MoS_2$ double-layer memristor with electrochemical metallization as an atomic-scale synapse with switching thresholds approaching 100 mV. Nano Lett, 2019, 19: 2411–2417
28 Abnavi A, Ahmadi R, Hasani A, et al. Free-standing multilayer molybdenum disulfide memristor for brain-inspired neuromorphic applications. ACS Appl Mater Interfaces, 2021, 13: 45843–45853
29 Wang M, Cai S, Pan C, et al. Robust memristors based on layered two-dimensional materials. Nat Electron, 2018, 1: 130–136
30 Zhu X, Li D, Liang X, et al. Ionic modulation and ionic coupling effects in $MoS_2$ devices for neuromorphic computing. Nat Mater, 2019, 18: 141–148
31 Cheng P, Sun K, Hu Y H. Memristive behavior and ideal memristor of 1T Phase $MoS_2$ nanosheets. Nano Lett, 2016, 16: 572–576
32 Tang B, Veluri H, Li Y, et al. Wafer-scale solution-processed 2D material analog resistive memory array for memory-based computing. Nat Commun, 2022, 13: 3037
33 Desai S B, Madhvapathy S R, Sachid A B, et al. $MoS_2$ transistors with 1-nanometer gate lengths. Science, 2016, 354: 99–102
34 Yang Y, Gao P, Li L, et al. Electrochemical dynamics of nanoscale metallic inclusions in dielectrics. Nat Commun, 2014, 5: 4232
35 Naqi M, Kang M S, liu N, et al. Multilevel artificial electronic synaptic device of direct grown robust $MoS_2$ based memristor array for in-memory deep neural network. npj 2D Mater Appl, 2022, 6: 53
36 Zhao X, Fan Z, Xu H, et al. Reversible alternation between bipolar and unipolar resistive switching in $Ag/MoS_2/Au$ structure for multilevel flexible memory. J Mater Chem C, 2018, 6: 7195–7200
37 Geim A K. Graphene: status and prospects. Science, 2009, 324: 1530–1534
38 Liu S, Lu N, Zhao X, et al. Eliminating negative-SET behavior by suppressing nanofilament overgrowth in cation-based memory. Adv Mater, 2016, 28: 10623–10629
39 Liu L, Kong L, Li Q, et al. Transferred van der Waals metal electrodes for sub-1-nm $MoS_2$ vertical transistors. Nat Electron, 2021, 4: 342–347
40 Liu Y, Guo J, Zhu E, et al. Approaching the Schottky-Mott limit in van der Waals metal-semiconductor junctions. Nature, 2018, 557: 696–700
41 Li Q, Tao Q, Chen Y, et al. Low voltage and robust InSe memristor using van der Waals electrodes integration. Int J Extrem Manuf, 2021, 3: 045103
42 Mao J, Wu S, Ding G, et al. A van der Waals integrated damage-free memristor based on layered 2D hexagonal boron nitride. Small, 2022, 18: 2106253
43 Guo J, Wang L, Liu Y, et al. Highly reliable low-voltage memristive switching and artificial synapse enabled by van der Waals integration. Matter, 2020, 2: 965–976
44 Chiu F C. A review on conduction mechanisms in dielectric films. Adv Mater Sci Eng, 2014, 2014: 1–18
45 Miremadi B K, Cowan T, Morrison S R. New structures from exfoliated $MoS_2$. J Appl Phys, 1991, 69: 6373–6379
46 Acerce M, Voiry D, Chhowalla M. Metallic 1T phase $MoS_2$ nanosheets as supercapacitor electrode materials. Nat Nanotech, 2015, 10: 313–318

47 Zhang P, Gao C, Xu B, et al. Structural phase transition effect on resistive switching behavior of $MoS_2$-polyvinylpyrrolidone nanocomposites films for flexible memory devices. Small, 2016, 12: 2077–2084

48 Wang L, Xu Z, Wang W, et al. Atomic mechanism of dynamic electrochemical lithiation processes of $MoS_2$ nanosheets. J Am Chem Soc, 2014, 136: 6693–6697

49 Sangwan V K, Lee H S, Bergeron H, et al. Multi-terminal memtransistors from polycrystalline monolayer molybdenum disulfide. Nature, 2018, 554: 500–504

50 Vu Q A, Kim H, Nguyen V L, et al. A high-on/off-ratio floating-gate memristor array on a flexible substrate via CVD-grown large-area 2D layer stacking. Adv Mater, 2017, 29: 1703363

51 Zhai Y, Yang X, Wang F, et al. Infrared-sensitive memory based on direct-grown $MoS_2$-upconversion-nanoparticle heterostructure. Adv Mater, 2018, 30: 1803563

52 Lee J, Pak S, Lee Y W, et al. Monolayer optical memory cells based on artificial trap-mediated charge storage and release. Nat Commun, 2017, 8: 14734

53 Wang X F, Tian H, Zhao H M, et al. Interface engineering with $MoS_2$-Pd nanoparticles hybrid structure for a low voltage resistive switching memory. Small, 2018, 14: 1702525

54 Krishnaprasad A, Dev D, Han S S, et al. $MoS_2$ synapses with ultra-low variability and their implementation in Boolean logic. ACS Nano, 2022, 16: 2866–2876

55 Sun W, Gao B, Chi M, et al. Understanding memristive switching via in situ characterization and device modeling. Nat Commun, 2019, 10: 3453

56 Choi S, Tan S H, Li Z, et al. SiGe epitaxial memory for neuromorphic computing with reproducible high performance based on engineered dislocations. Nat Mater, 2018, 17: 335–340

57 Zhao X, Liu S, Niu J, et al. Confining cation injection to enhance CBRAM performance by nanopore graphene layer. Small, 2017, 13: 1603948

58 Mayer J, Giannuzzi L A, Kamino T, et al. TEM sample preparation and FIB-induced damage. MRS Bull, 2007, 32: 400–407

59 Hus S M, Ge R, Chen P A, et al. Observation of single-defect memristor in an $MoS_2$ atomic sheet. Nat Nanotechnol, 2021, 16: 58–62

60 Bessonov A A, Kirikova M N, Petukhov D I, et al. Layered memristive and memcapacitive switches for printable electronics. Nat Mater, 2015, 14: 199–204