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• REVIEW •
Special Topic: Two-Dimensional Materials and Device Applications

Two-dimensional materials-based integrated hardware

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Abstract In recent years, two-dimensional (2D) materials-based fundamental preparing process such as high-quality wafer-level single crystal thin film synthesis technology and high-performance electrode preparing technology has developed rapidly. In addition, the integrated application prospect of 2D materials has been preliminarily verified, owing to the flat and clean interface between 2D materials and substrates. From the perspective of electronics and optoelectronics based on 2D materials, this paper will summarize the recent studies of integrated circuit hardware, integrated optoelectronic hardware, and hetero-integrated hardware, showing their advantages and potential application.

Keywords two-dimensional materials, integrated circuit, integrated sensor, integrated optoelectronics

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1 Introduction

In the past, the development of integrated circuits (ICs) followed Moore's law, whereby the size of devices and the power consumption shrank by half every 18 months [1]. However, when the thickness of traditional silicon-based semiconductor materials is reduced to a few nanometers, the carrier mobility will decline sharply due to the large amount of scattering phenomenon caused by the rough surface, resulting in degradation to device functionality and hindering the continuation of Moore's law [2,3]. Recently, many researchers have made efforts to find new materials to overcome the above problems. Two-dimensional (2D) materials, whose carrier mobility decline is not obvious within a few nanometers of material thickness due to their flat, smooth surface and absence of dangling bonds, are considered strong candidates for channel materials at the nanoscale to overcome short-channel effect and break the bottleneck of Moore's law [4–10].

2D materials are formed by interlayer van der Waals force, which means they can be heterogeneously integrated easily and stably even with monolayer thickness. The atomic-level thickness of 2D materials allows their physical properties to be easily modulated by external physical fields (such as electric [11], light [12], magnetic field [13], and strain [14]), thus enabling them to achieve richer functions. Combining the two characteristics above, a sensory chip [15–18] can be realized by heterogeneous integration of 2D materials-based sensors and traditional CMOS (complementary metal oxide semiconductor) IC, making full use of the unique advantages of each part to achieve more advanced functions.

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On the other hand, various 2D materials can cover a very wide electromagnetic spectrum due to different optoelectronic properties [19]. For example, graphene is a bandgap-free semi-metallic material that can interact with light from microwave to ultraviolet, therefore becomes a potential candidate for light detection, modulation, and manipulation applications across a wide spectral range. The direct bandgap structure and high carrier mobility of black phosphorus make it the preferred material for mid and far-infrared detection. Transition metal chalcogenides (TMDs) are semiconductor materials with very peculiar optoelectronic properties in the near-infrared wavelength range. The breaking of inverse symmetry and strong spin-orbit coupling leads to the circular dichroism of energy valley selection. Hexagonal boron nitride (hBN) has a large band gap of about 6 eV and is a good insulating dielectric widely used for electrostatic control of other 2D materials. Unlike bulk materials, the band gap of 2D materials is the thickness (number of layers) dependent, which generally decreases by 1–2 eV as the thickness increases [20] and further expands the photoelectric detection range. Due to atom-scale thickness, carrier concentration and Fermi energy level of 2D materials are easily regulated by an external field, giving them tunable photoelectric properties [21]. At the same time, 2D materials can build a clean heterogeneous interface with optical structures (waveguides, resonators) without considering lattice mismatch, and realize high-performance on-chip photodetector, optical modulator and other integrated optoelectronic chip applications [22–26].

To realize the integrated hardware of 2D materials, it is first necessary to develop a mature process for high-quality wafer-level 2D material synthesis. Based on the preparation method of chemical vapor deposition (CVD, including MOCVD (metal-organic CVD) and LPCVD (low pressure CVD)), graphene has successfully achieved the preparation of wafer-level single crystal films on hydrogen-end Ge(100) [27], Cu foil [28, 29]; h-BN has been prepared into multi-layer or single-layer single crystal films over 2-inch on sapphire [30], Cu(110) [31], Cu(111) [32]; TMD materials such as MoS_2 achieve 2-inch high-quality single-oriented single-crystal films on Au(111) [33] and sapphire A-axis (C/A) [34, 35]. Secondly, non-destructive transfer methods for large-scale 2D materials must be developed. Organic film-assisted (including PDMS/PMMA [36–38], rosin [39], and cellulose [40]) and wafer bonding [41] have been verified to be suitable, automated material exfoliation and transfer systems [42,43] have been successfully developed. Different from the traditional silicon-based semiconductor process that improves metal-semiconductor contact by heavy doping, the atomic-level thickness of 2D materials is no longer suitable for traditional doping methods and a new electrode contact process needs to be developed. Methods such as metal work function match [44–46], evaporation process improvement [47, 48], and electrode transfer [49–53] were proposed, all of which are suitable for electrode preparation of large-scale ICs. In summary, 2D material initially has the basis for integrated manufacturing.

The development of 2D materials integration hardware has begun to appear. In this review, we first start with the IC of 2D materials, show the potential of 2D materials replacing traditional silicon-based semiconductors as channels to realize ICs, the research status of 2D materials in emerging memristor arrays and the related applications of integrated sensors through heterogeneous integration with mature silicon-based circuits. Then, the integrated optoelectronic applications of 2D materials are summarized, including the related work of heterogeneous integration with optical structures to realize on-chip optoelectronic devices and the integrated application of photoelectric sensing-memory-computing based on non-von Neumann architecture, showing the unique advantages of 2D materials in the field of integrated optoelectronics. Finally, the development prospects of 2D materials integrated hardware are proposed. The scope of this review is shown in Figure 1.

2 2D material electronic hardware

2.1 2D material IC

2D materials can be obtained by mechanical exfoliation (ME), but the channel size is often at the level of tens of microns, which cannot meet the preparation needs of large-scale ICs. Grown by CVD, 2D materials can achieve the wafer-level size and be used to prepare large-scale conventional ICs and memristor arrays (Table 1) [34, 54–69].

2.1.1 *Conventional IC*

The field-effect transistor (FET) is the unit device of the traditional IC, and wafer-level 2D materials are often prepared into FETs to test their material quality and integration effects. Rahimi et al. [54]

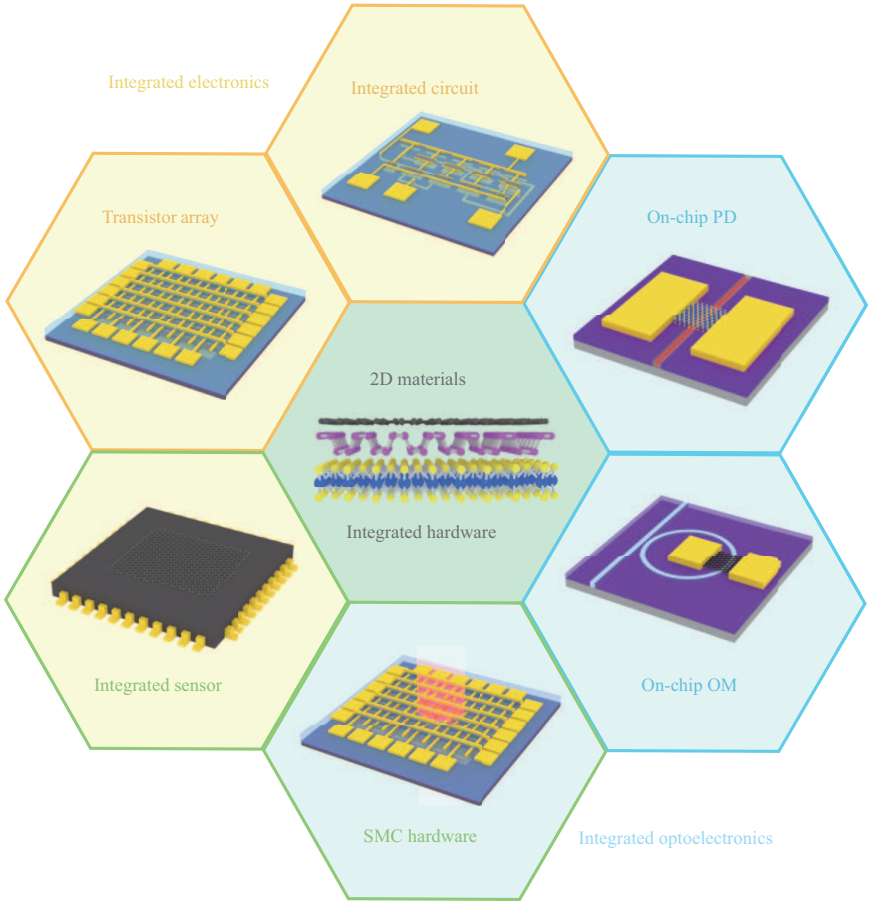

Figure 1 (Color online) Overview of 2D materials-based integrated hardware. PD: photodetector; OM: optical modulator; SMC: sensor-memory-computing.

reported polycrystalline graphene with a diameter of 300 mm grown on copper foil by CVD, about 26000 graphene FETs were prepared by wet transfer to silicon wafer substrate, with a device yield of 74%, 18% of devices' mobility of > 3000 $cm^2 \cdot V^{-1} \cdot s^{-1}$, frequency doubler and amplifier were demonstrated on this basis. Li et al. [34] grew a 2-inch monolayer MoS_2 single crystal film on a C/A-oriented sapphire substrate, then fabricated 160 FETs with device yield of $> 94\%$, device-to-device mobility deviation of only 15%, mobility of 102.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and saturation current of 450 $\mu A \cdot \mu m^{-1}$, demonstrating the potential of the high-quality MoS_2 single crystal film prepared by this most advanced method for the large-scale IC. Kang et al. [55] directly grew a monolayer MoS_2 film on a 4-inch insulating SiO_2 wafer by MOCVD, by which the batch-prepared FET yield was as high as 99% with mobility of 20 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature. They also realized a multilayer stacked MoS_2 FET by continuing to deposit SiO_2 and grow MoS_2 film on it, the underlying device performance was not significantly affected by the upper process. It provides a practical technical solution for the development of a three-dimensional stacked IC based on 2D materials.

The ICs can be divided into analog circuits and digital circuits according to the type of signal processed. Analog ICs take an operational amplifier (op-amp) as a functional unit, combined with feedback circuits to build more complex circuit systems such as adders, integrators, differentiators, buffers, and filters. Digital ICs are built on various logic gates to form arithmetic logic circuits such as adder, subtraction, combinatorial logic, or sequential logic circuits including latch and flip-flop. The implementation of circuit-level applications relies on the synthesis and preparation of large-area and high-quality 2D materials, to reduce the performance differences between devices to stably realize the overall circuit function. Polyushkin et al. [56] used 46 MoS_2 NMOS transistors to implement an op-amp (Figure 2(a)) for the first time, with an open-loop gain of 36 dB, a unity-gain transition frequency of 0.3 MHz, a threshold voltage of 11 mV, high device consistency and a maximum standard deviation of $\sigma V_{\rm th}$ at 0.365 V. Based on this, the circuit structure functions of inverting amplifiers, integrators, log amplifiers and trans-impedance

Table 1 Summary of typical 2D materials IC

	Materials	Synthetic methods	Circuit size	Circuit type	Ref.
Integrated circuit	MoS_2	CVD	6 mm × 6 mm; 46 FETs	Inverting/log op-amp integrator/TIA	[56]
	$MoTe_2$	ME	–	p-n junction/BJT array	[57]
	MoS_2	CVD	50 mm^2; 115 FETs	1-bit uP/ ALU/D-Latch	[58]
	MoS_2	CVD	4-inch; 1518 FETs	Logic gate/ SRAM/5-stage RO	[59]
	MoS_2	CVD	2-inch; 1296 TG-FETs	DFF/(1-bit) FA/5-stage RO/ 1T1C dynamic memory	[62]
	MoS_2	CVD	2-inch	Voltage divider/logic gate/ inverting op-amp/ TI	[63]
	MoS_2	CVD	2-inch; 160 FETs	FET	[34]
	MoS_2; WS_2	MOCVD	4-inch	FET	[55]
	Graphene	CVD	300 mm; 26000 FETs	FET	[54]
	MoS_2	Spin-coating	100 mm	Logic gate/HA	[60]
	Te	Thermal evaporation	4-inch	Logic gate/FA 2-bit multiplier/ 3D inverter	[61]
Transistor array	hBN/graphene/hBN	ME	12 × 12	Memristor array	[64]
	hBN	CVD	2-inch; 10 × 10	Memristor array	[65]
	hBN	CVD	4 × 4/100 × 100	Memristor array	[66]
	MoS_2	CVD	10 × 9	Memtransistor array	[67]
	MoS_2	CVD	10 × 10	Memtransistor array (1T1R)	[68]
	MoS_2	CVD	2-inch	Memtransistor array (2T1C)	[69]

amplifiers (TIA) were demonstrated. Seo et al. [57] used laser irradiation doped 2H-$MoTe_2$ to realize the transition from N-type semiconductors to P-type semiconductors, the programmable doping method quickly, simply, and accurately realized the preparation of n-p-n (p-n-p) bipolar junction transistor (BJT) amplifiers and p-n photovoltaic device arrays. The common emitter amplification coefficient of the BJT exceeded 150 and the external quantum efficiency (EQE) of the diode was 10%–16%. It provides a feasible scheme for the preparation of large-scale 2D materials-based circuits.

Wachter et al. [58] used 115 MoS_2 FETs to implement a 1-bit microprocessor (uP) (including arithmetic and logic unit (ALU) and D-Latch) (Figure 2(b)) for the first time, the devices operated at 2–20 kHz, executed user-defined programs stored in the external memory and performed logic operations and communicating with peripheral devices, thus preliminarily verifying the feasibility of 2D materials for the ICs which can be optimized through more elaborate fabrication processes. Li et al. [59] grew a single layer MoS_2 film on a 4-inch sapphire wafer substrate by CVD and then transferred it to other substrates by a wet process to prepare 1518 transistors, with contact resistance of < 2.9 k$\Omega\cdot\mu m^{-1}$, device yield of 97%, on/off switching ratio of 10^{10}, the current density of 35 $\mu A\cdot\mu m^{-1}$, the carrier mobility of 55 $cm^2\cdot V^{-1}\cdot s^{-1}$. Based on them, logic gate circuits such as inverter, NOR, NAND, AND, static random-access memory (SRAM), and five-stage ring oscillator (RO) circuit (stable oscillation frequency of 13.12 MHz) were prepared to demonstrate the feasibility of 2D materials integration. More conveniently, Lin et al. [60] prepared logic gates and computing circuits such as inverters, NAND, NOR, AND, XOR, and half-adder (HA). By spin coating the dispersive liquid of MoS_2 into films, with on/off switching ratio of 10^6 and carrier mobility of 10 $cm^2\cdot V^{-1}\cdot s^{-1}$. It can meet the performance requirements of most integrated chip applications with simple processes and low costs. Also, a polycrystalline material, Zhao et al. [61] deposited Te thin film by thermal evaporation and produced P-type FETs on a wafer-scale film with hole carrier mobility of 35 $cm^2\cdot V^{-1}\cdot s^{-1}$, on/off switching ratio of 10^4 and subthreshold swing of 108 $mV\cdot decade^{-1}$. A full adder (FA) circuit composed of 35 transistors and a multiplier circuit composed of 39 transistors were fabricated at the same time, and an inverter circuit with a vertical stack structure was shown. Systematically, Chen et al. [62] used a machine learning algorithm to evaluate the key process parameters that affect the performance of MoS_2 transistors and optimized the device performance by using a wafer-level manufacturing process to conduct 62-level SPICE modeling. Besides, they proposed a standard industry design flow and process to manufacture the FET array or 4-bit adder. The FET carrier mobility can reach 46.7 $cm^2\cdot V^{-1}\cdot s^{-1}$, the yield of 144 1-bit FAs was 50%, which can be improved by optimizing the synthesis method of MoS_2 film. With novel functions, Zheng et al. [63] manufactured the Bayesian network hardware consisting of 29 memtransistors using a single layer MoS_2 thin film grown by CVD. The S-bit generator was realized based on the voltage divider, inverting amplifier, and thresholding inverter (TI) of six memtransistors, cascaded with a 2 × 1 multiplexer. It took only 1.2 nJ to realize the

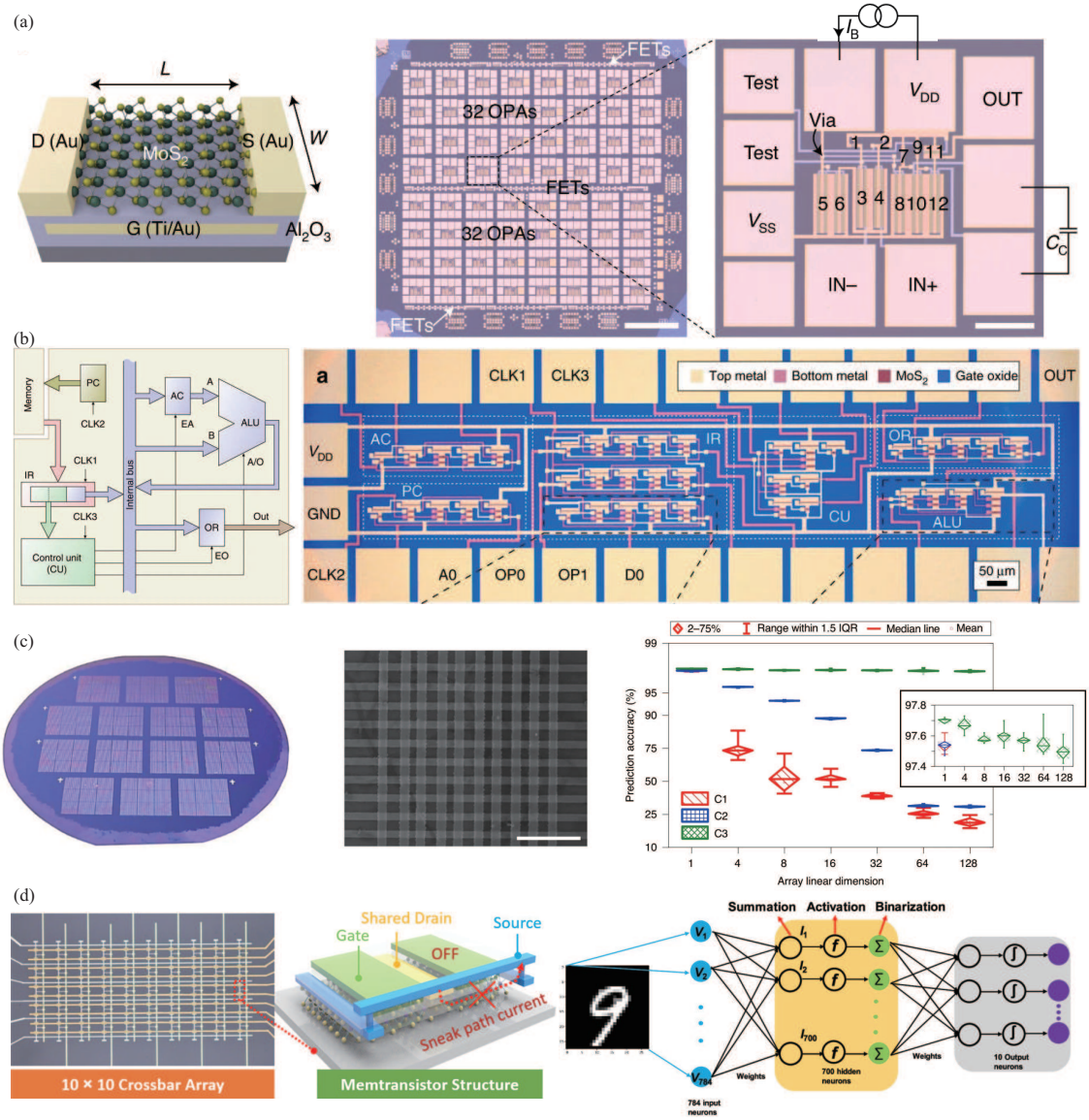

Figure 2 (Color online) (a) Schematic of a MoS_2 back-gate transistor (left) and its composition of 64 op-amps (enlarged view) and test transistors (right) [56] Copyright 2020 Springer Nature. (b) Flow diagram of a 1-bit microprocessor (left) and actual chip diagram (right) [58] Copyright 2017 Springer Nature. (c) 2-inch wafer with hBN memristor crossbar array (left), SEM image of a memristor crossbar array (center; scale bar, 4.5 μm), MNIST dataset simulation results of an ex situ-trained multilayer perceptron (right) [65] Copyright 2020 Springer Nature. (d) Optical image of a molybdenum sulfide memtransistor crossbar array (left), 3D schematic illustration of two neighboring memtransistor cells (middle), a three-layer neural network scheme (right) [68] Copyright 2021 American Chemical Society.

Bayesian network calculation.

In summary, through the preparation of high-quality wafer-scale, 2D materials have the potential to build large-scale ICs. However, limited by the fineness of the available process, their integration feasibility has only been verified at the micron-level channel size. Only when the wafer-scale synthesis and transfer technique is mature, will 2D material ICs be used widely. Whether it can truly replace traditional silicon-based semiconductors as channel materials, overcome the short channel effect, and continue the development of Moore's law remains to be further verified by semiconductor manufacturing companies.

2.1.2 *Transistor array*

As the fourth type of electronic component, the memristor with two-terminal memory characteristics can provide a natural matrix multiplication function in its compact vertical crossbar array structure, which is suitable for simulating the parallel computing of neural networks, and realizes more efficient algorithmic

function hardware implementation through the non-von Neumann architecture of neuromorphic computing. Performance uniformity and multi-stage linear conductance between devices of memristor array elements are the basis for high-performance neuromorphic computing. 2D materials are used to fabricate memristor arrays because of their flat material interfaces, homogeneous crystal structures, and wafer-level fabrication capabilities. As a wide-bandgap 2D material, h-BN provides peculiar memristor characteristics due to the tunneling mechanism under atomic layer thickness. Sun et al. [64] used mechanically exfoliated hBN and graphene to construct hBN/graphene/hBN heterostructure as a memristor functional layer, the graphene layer effectively blocked the diffusion of volatile silver wires, and the heterostructure provided self-selective storage characteristics that solved current-voltage matching integration problems and destructive read operation problems of complementary resistance switches, with self-selectivity of $> 10^{10}$, on/off resistance ratio of $> 10^3$, open current of 0.3 mA. At the same time, the sneak current was greatly reduced, and the letter code was programmed utilizing a 12×12 crossbar array. Chen et al. [65] grew multilayer hBN films on copper foil by CVD and wet transferred them to a 2-inch pre-laid bottom electrode wafer and prepared a top electrode to obtain multiple 10×10 crossbar arrays (Figure 2(c)) with a device yield of $> 98\%$, cycle-to-cycle variation of 1.53%, device-to-device variation 5.74% and dynamic switching conductance of 200 nS–40 mS, which achieved MNIST handwritten digit recognition with an accuracy of up to 98.02%. Shen et al. [66] prepared 100×100 scale memristor arrays by CVD hBN with a yield of up to 100%, the influence of local defects on device yield and variation was studied, proving that most defects in 2D materials do not affect the quality of memristor array cells and the variation between devices, and the preparation process was simpler by using 2D materials for memristor arrays.

Memtransistors are different from two-terminal memristors, which can get better linear conductance through the modulation of gate voltage. 2D semiconductor TMD materials (mainly MoS_2) are usually used in the research of memtransistors. Lee et al. [67] used a CVD-grown single layer to build a compact upper and lower dual-gate memtransistor array with an active channel size of < 1 μm and the energy consumption of < 2 pJ in a single switching cycle. Dual-gate not only provided conductance modulation but also further controlled the device's switching state to suppress sneak current and crosstalk between nodes. The artificial neural network was simulated by 10×9 crossbar array, and 94% recognition rate of the handwritten digit was achieved by the linear-weight update controlled by the gate. Feng et al. [68] used a CVD-grown single-layer polycrystalline MoS_2 film to construct a memtransistor array (1T1R) (Figure 2(d)). The transistor connected to the memtransistor realized the selector function through independent gate control, with only 0.1 nA sneak current, 3–4.5 F^2 dense cell size, and 20 fJ bit^{-1} switching energy at an operating voltage of 0.42 V. By the multiplication and sum operation of 10×10 crossbar array, a high MNIST recognition accuracy of 96.87% was simulated. Wang et al. [69] used CVD-grown MoS_2 to build 2T1C cells, where 1T1C acted as dynamic random access memory (DRAM), and another transistor performed multiplication operations through gate bias and drain voltage. Current summation was achieved by cascading multiple cells. 8-bit multiply-accumulate (MAC) composed of 32 2T1C cells acts as a neuron, by using 400×20 neurons for handwritten digit recognition, the accuracy was up to 90.3%.

Therefore, 2D materials can be widely used in the research of memristor/memtransistor arrays due to their uniform structure and highly adjustable electrical properties, contributing to data-centric artificial intelligence and Internet of Things applications [70, 71]. However, whether 2D materials can perform the task of neural networks based on crossbar arrays still depends on the stability of devices, which is up to the process problem.

Furthermore, the synthesis of high-quality wafer-scale 2D materials has laid the foundation for the realization of arrays. Taking full advantage of its easily heterogeneous integration, compact arrays of transistors or circuits can be constructed to drive LED for display applications. Meng et al. [72] prepared a transistor array based on high-quality MoS_2 single crystal thin film prepared on the 2-inch sapphire, and connected with micro-LED pixel unit one by one through via holes to realize independent driving of each pixel unit (Figures 3(a) and (b)). The new process improved the performance of thin film transistors by more than 200%, reduced the difference by 67%, and the maximum drive current exceeded 200 μA/μm, which is better than indium gallium zinc oxide (IGZO), low temperature poly-silicon (LTPS), and other commercial materials, demonstrating the huge application potential of 2D materials in the display drive industry. Choi et al. [73] used an 18×18 molybdenum disulfide thin film transistor array as the backplane and driver circuit, achieved a wearable, full-color OLED display through the integration of RGB organic light-emitting diodes (Figure 3(c)). The on-state current did not fluctuate, and the variation was below 8% which was acceptable for active-matrix display operation. In addition, due to the relaxation of

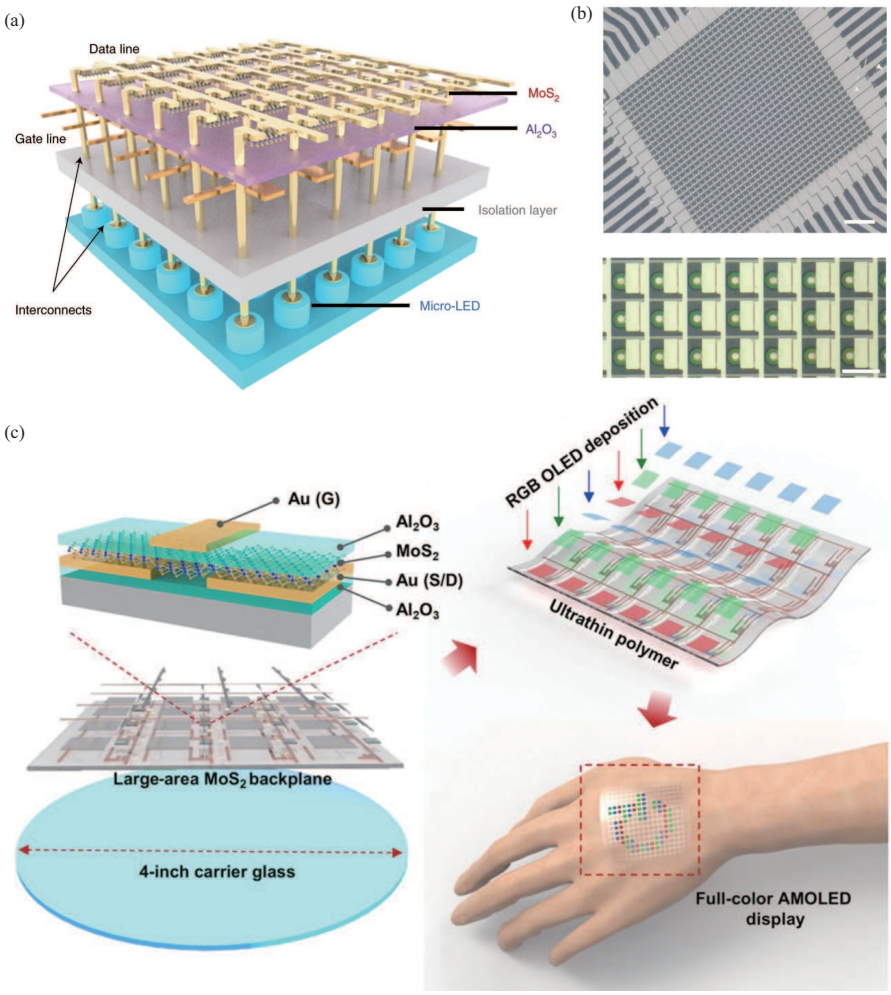

Figure 3 (Color online) Schematic illustration (a) and optical micrographs (b) of the AM micro-LED display (scale bar, 100 μm (top right), 20 μm (bottom right)) [72] Copyright 2021 Springer Nature. (c) Schematic illustration of the high-performance MoS_2-based backplane on a 4-inch carrier glass substrate, where an Al_2O_3 capping layer was applied for n-doping effects on the MoS_2 film (top left), an active-matrix full-color display was applied to the ultrathin polymer substrate (top right), and the large-area full-color display was tested on a human hand (bottom right) [73] Copyright 2020 AAAS.

epitaxial strain on slippery 2D surfaces, single-crystalline red AlGaAs LED and green/blue InGaN LED can be grown and transferred easily with wafer-scale graphene and hBN as assistance, respectively [74]. The advantages of 2D materials, such as high drive current, flexibility, optical transparency, and easily heterogeneous integration, create great opportunities in advanced display applications.

2.2 2D material heterogeneous integrated sensor

Due to the adjustability of its rich physical properties, 2D material can be used to detect physical information by building a variety of sensors such as gas sensors, magnetic sensors, thermal-sensor, and bio-sensor, which even have more excellent sensory functions than traditional sensors in some aspects. Although available commercial 2D materials IC chip pipeline and mature manufacturing process are lacking, the capability of defect-free heterogeneous integration still makes it a promising candidate for the next-generation sensors. Through the heterogeneous integration of 2D materials-based sensors and silicon-based chips to receive the sensory signal of 2D materials and process useful information, it is promising to realize more sensitive and portable integrated sensor applications.

As the most widely studied 2D material, graphene can achieve high-quality large-area synthesis, has a simple structure, clear physical mechanism, and high carrier mobility, and is mainly used for integrated sensor research. Since large-area graphene is often required, efficient and reliable CVD-grown graphene films are commonly used as functional materials. Zanjani et al. [15] used the unique sensitivity of graphene

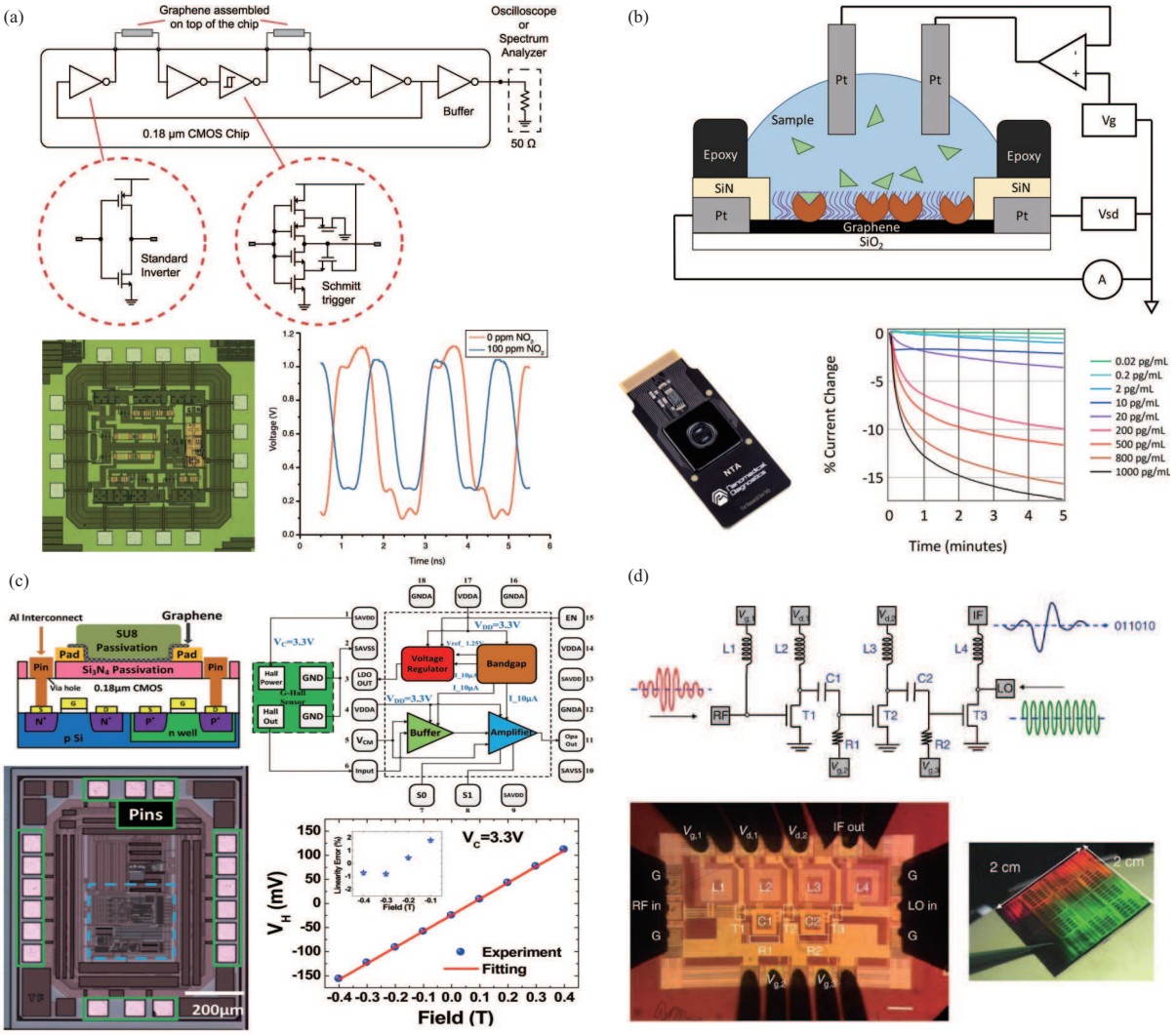

Figure 4 (Color online) (a) Circuit diagram of monolithic integrated CMOS-graphene sensor (top), diagram and measured output (res curve, 491 MHz; blue curve, 685 MHz) of the integration of monolayer graphene and Si CMOS (bottom) [15] Copyright 2017 Springer Nature. (b) Schematic of the graphene digital biosensor chip (top), the optical image of the completed biosensor, and the test results under different antibody concentrations (bottom) [16] Copyright 2019 Springer Nature. (c) Cross-section diagram and optical image of the graphene/silicon hybrid chip (left), circuit diagram of the hybrid chip, and Hall voltage changes with the magnetic field in voltage mode (right) [17] Copyright 2014 Springer Nature. (d) Circuit diagram of a 3-stage graphene receiver integrated chip containing 11 active and passive components (top), optical microscope image of the chip under test and fabricated edition (bottom) [18] Copyright 2014 Springer Nature.

to NO_2 gas to achieve NO_2/NH_3 gas concentration detection by integrating CVD single-layer graphene and 2.5 mm × 2.5 mm silicon-based CMOS readout circuit (Figure 4(a)), and 52% of the optimized device can successfully generate a measurement signal. Using the RO readout circuit as a frequency shift signal output, the gas concentration information was obtained by analyzing the frequency change, which combined the superior gas sensitivity of single-layer graphene with the low power consumption and low-cost advantages of silicon-based CMOS. Goldsmith et al. [16] used CVD-grown graphene film as a functional layer of biosensors to detect PH, protein, and other information. Biomolecules were fixed on 15 graphene sensors on the surface to reduce the possibility of local mechanical damage (such as pipette tips), which can destroy the sensing channel. By comparing and encapsulating the reference electrode and graphene signal through the PCB board, a digital biosensor based on a graphene field effect transistor was realized (Figure 4(b)). Huang et al. [17] integrated CVD-grown graphene and silicon CMOS ICs for Hall signal measurements (Figure 4(c)), by combing the ultra-high carrier mobility of graphene and the complex functionality of silicon CMOS ICs, the sensitivity of graphene Hall elements was improved to 200 $V{\cdot}A^{-1}{\cdot}T^{-1}$ (silicon-based Hall element sensitivity is typically about 100 $V{\cdot}A^{-1}{\cdot}T^{-1}$) and can operate normally at a low supply voltage of 3.3 V. Moreover, the graphene Hall element was manufactured on the

passivation layer of the CMOS chip by a low-temperature microfabrication process, which could provide a feasible process for the heterogeneous integration of 2D materials and silicon-based CMOS ICs. Han et al. [18] used a graphene transistor prepared by CVD to build a 3-stage graphene IC (Figure 4(d)) as RF receivers, performing signal amplification, filtering, and downconversion mixing functions within a circuit consisting of 3 GFETs, 4 inductors, 2 capacitors, and 2 resistors. It can receive digital text transmitted on a 4.3 GHz carrier signal. The entire IC manufacturing process was below 400°C, making it ideal for monolithic 3D integration with silicon-based CMOS IC, providing process support for realizing more feature-rich and complex graphene RF receiving 3D ICs.

By taking full advantage of the highly sensitive characteristics of 2D materials and combining the silicon-based CMOS IC with mature technology and rich functions, the integrated sensory chip with better sensing performance can be realized through heterogeneous integration. 2D materials complement high-value applications in silicon-based integrated chips with new function additions or performance optimizations.

3 2D material optoelectronic hardware

3.1 On-chip photodetector

According to the relaxation process in the photon-electric conversion process, the working mechanism of the on-chip photodetector can be divided into the light-relaxation type and the thermal-relaxation type. Light-relaxation mechanism includes extracting the light response by collecting photoexcited carriers, including the photovoltaic effect (PV), the thermo-electron emission effect (IPE), the direct tunneling (DT), the Fowler-Nordheim tunneling (FN), or detecting the change of conductivity of the channel, namely the photoconductivity effect (PC). The thermal-relaxation mechanism mainly includes two types: the bolometric (BOL) effect and the photo-thermoelectric (PTE) effect. On-chip photodetectors (Table 2) [75–112], which are widely used in the field of optical communications, generally realize the reception of optical signals through photo-electron conversion and have a high demand for device response bandwidth and responsivity.

Graphene is a zero-bandgap semi-metallic material with a response bandwidth of over 100 GHz due to its high carrier concentration. Due to its simple atomic composition, CVD-grown or mechanically exfoliated graphene is of high quality and can be used to build on-chip photodetectors. Devices with a metal-graphene-metal structure were constructed by wet-transferring CVD-grown graphene films, and some studies were carried out based on PVs [75–79]. Ma et al. [75] prepared a metal slot waveguide above graphene on an SOI substrate, the responsivity to 1350 nm light reached 0.7 $A{\cdot}W^{-1}$ with a device length of 5 μm, and the ultra-narrow slot width (15 nm) made the theoretical value of its response bandwidth as high as 276 GHz. Ding et al. [76] built a graphene plasmonic photodetector by preparing a metal slot waveguide on graphene, achieving a photoresponsivity of 360 $mA{\cdot}W^{-1}$ and a response bandwidth of 110 GHz under 19 μm light. Ma et al. [79] developed a plasmonically enhanced waveguide-integrated graphene photodetector with a 6-micron long graphene layer combined with a nanometallic structure, showing a responsivity of 0.5 $A{\cdot}W^{-1}$ and a response bandwidth of 11 GHz. Wang et al. [80,81] transferred CVD-grown graphene to a metal slot waveguide to construct an on-chip photodetector, achieving a response bandwidth of 70 GHz and a responsivity of not less than 0.1 $A{\cdot}W^{-1}$, to realize a more complex polarization division multiplexing optical receiving chip and optical coherent receiver (Figure 5(a)).

Also, there are studies based on PTE effects by modulating carrier type with split-gate structure [82–85]. Muench et al. [82] built a graphene photosensitive layer on the silicon nitride plasmonic slot waveguide, and symmetrically fabricated the split-gate dielectric (Al_2O_3) and the electrode on it. The independent electrostatic modulation of the double gates made the channel form different types of conductive regions arranged horizontally, thus the barrier of the p-n junction resulted in a steeper temperature gradient and faster thermal diffusion capacity, achieving a response bandwidth of 42 GHz under 1550 nm light and a photoresponsivity of up to 12.2 $V{\cdot}W^{-1}$. Marconi et al. [83] also utilized the split-gate structure based on silicon planar waveguide, which has a response bandwidth of up to 65 GHz. Mišeikis et al. [84] transferred graphene onto a silicon nitride straight waveguide, using polyvinyl alcohol (PVA) as the gate dielectric and combining with the split-gate structure to increase the Seebeck coefficient to 140 $\mu V{\cdot}K^{-1}$, they significantly enhanced the PTE effect and achieved a response bandwidth of up to 67 GHz with zero dark current.

Table 2 2D material on-chip photodetector

Materials	Synthetic methods	Structure	Principle	Bandwidth (GHz)	Responsivity ($A \cdot W^{-1}$)	Ref.
Graphene	CVD	M-S-M	PB/PV	276 (theory)	0.67/0.2	[75]
Graphene	CVD	M-S-M	PV	110	0.36	[76]
Graphene	CVD	M-S-M	PV	41	0.016	[77]
Graphene	CVD	M-S-M	PV	30	0.015	[78]
Graphene	CVD	M-S-M	PV	110	0.5	[79]
Graphene	CVD	M-S-M	PB/PC	20/>40	0.07/0.4	[112]
Graphene	CVD	M-S-M	PC	67	0.1	[80]
Graphene	CVD	M-S-M	PC	70	0.1	[81]
Graphene	CVD	Split-gate	PTE	42	12.2 $V \cdot W^{-1}$	[82]
Graphene	CVD	Split-gate	PTE	65	3.5 $V \cdot W^{-1}$	[83]
Graphene	CVD	Split-gate	PTE	67	6 $V \cdot W^{-1}$	[84]
Graphene	CVD	Split-gate	PTE	1	1.5 $V \cdot W^{-1}$	[85]
Graphene	ME	M-S-M	PV	18	0.03–0.05	[86]
Graphene	ME	M-S-M	PV	20	0.1	[87]
Graphene	ME	M-S-M	PTE	42	0.36	[88]
Graphene	ME	Split-gate	PTE	65	0.035	[91]
Graphene	ME	Split-gate	PTE	18	0.17	[89]
Graphene	ME	Split-gate	PTE	12	90 $V \cdot W^{-1}$	[90]
BP	ME	Top-gate	PV	3	0.657	[92]
BP	ME	Top-gate	PC	0.15	10	[93]
BP	ME	Top-gate	PC	–	23/2	[94]
BP	ME	M-S-M	PC	1	11.31	[95]
BP	ME	M-S-M	PC	1.33	0.3067	[96]
$PtSe_2$	CVD	M-S-M	PC	35	0.012	[97]
MoS_2	ME	M-S-M	PC	–	1000	[98]
WS_2	ME	M-S-M	–	–	–	[108]
$MoSe_2$	ME	M-S-M	PC	–	30	[109]
$MoTe_2$	ME	Split-gate	PV	34	0.4	[110]
$MoTe_2$	ME	Split-gate	PV	1.1	0.156	[99]
$MoTe_2$	ME/CVD	Split-gate	PV	0.2	0.0048	[100]
$MoTe_2$	ME	M-S-M	PC	0.035	0.5	[101]
$MoTe_2$	ME	M-S-M	PC	1	0.023	[102]
$MoTe_2$/Gr	ME	M-S-M	PC	24	0.2	[103]
$MoTe_2$/BP	ME	M-S-M	PV	1	0.709	[111]
MoS_2-Gr-hBN-Gr	CVD	M-S-M	PC (DT)	28	0.24	[104]
Graphene/Si	ME	M-S-M	PV/PC	–	0.13	[105]
Graphene/Si	CVD	M-S-M	IPE	–	0.37	[106]
Graphene/Si	CVD	Split-gate	PV/PTI	40	0.01	[107]

In addition, some on-chip photodetectors used mechanically exfoliated graphene [86–90]. Shiue et al. [88] built an in-plane metal junction barrier by constructing an asymmetric electrode structure on a silicon planar waveguide encapsulated by boron nitride (BN), achieving a photoresponsivity of 0.36 $A \cdot W^{-1}$ and a response bandwidth of 42 GHz at 1550 nm based on PTE effect. Schuler et al. [91] used two silicon strips of the silicon slot waveguide as local split-gate electrodes to create an adjustable p-n junction in the absorption region of graphene, through accurate absorption between p-doped and n-doped regions, the photoelectric response was maximized due to the PTE effect, and the response bandwidth at 1560 nm reached 65 GHz. Although graphene-based on-chip photodetectors can achieve high response bandwidth, the semi-metallic band structure of graphene leads to a high dark current. Black phosphorus, which has a moderate band gap and high carrier mobility, is considered a better photosensitive material [92–96]. Youngblood et al. [92] laid a small layer of black phosphorus on a silicon planar waveguide. By using ALD-deposited alumina as the gate dielectric and protective layer, graphene as the top electrode, and gate voltage to control the black phosphorus photodetector (Figure 5(b)), the device operated at a very low dark current, obtaining a responsivity of 0.657 $A \cdot W^{-1}$ and a response bandwidth of 3 GHz. Although black phosphorus can effectively reduce dark current, it is easily oxidized in the air, which limits its further

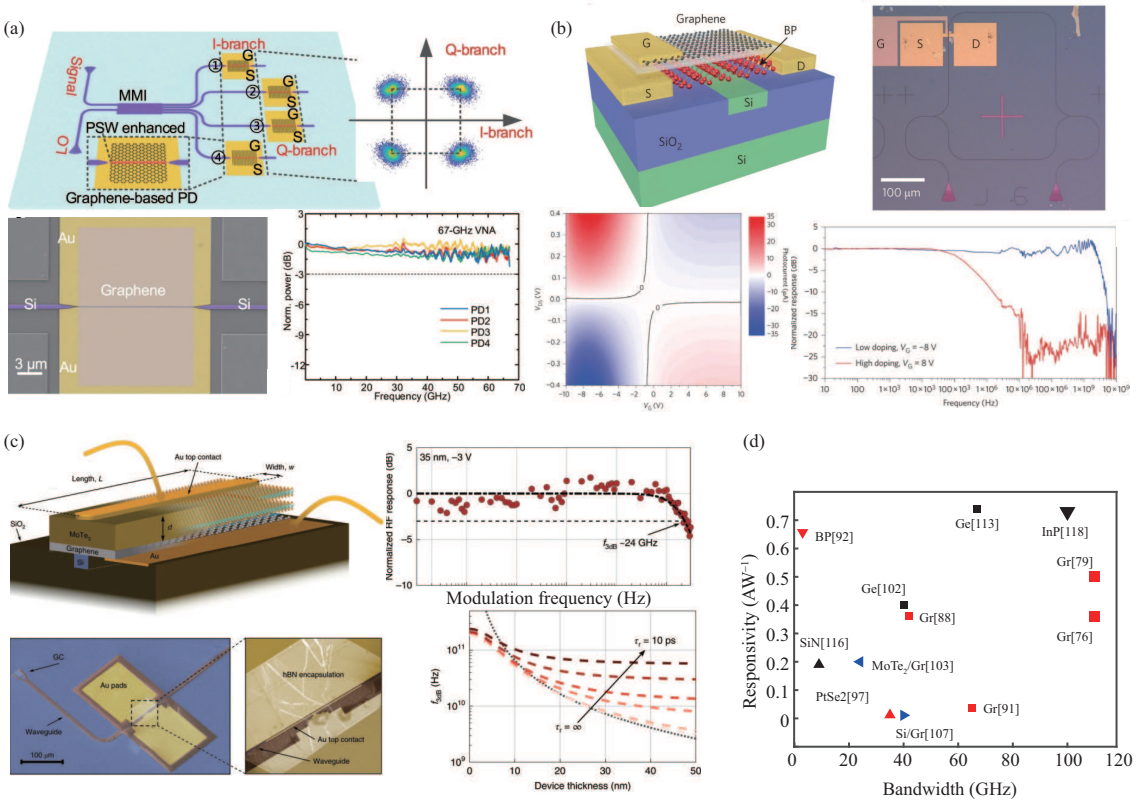

Figure 5 (Color online) (a) Schematic of a graphene optical coherent receiver (top), false-color SEM image and frequency response test results of a graphene photodetector on a slot waveguide (bottom) [80] Copyright 2021 Springer Nature. (b) 3D schematic of a top-gate modulating on-chip black phosphorus photodetector and optical microscope image of the device (top), 2D photocurrent diagram of gate voltage and bias correlation and frequency response results at high and low doping (bottom) [92] Copyright 2015 Springer Nature. (c) Schematic and false-color SEM image of an on-chip integrated vertical $MoTe_2$/graphene heterojunction photodetector (left), RF response results and thickness predictions for cut-off frequency (right) [103] Copyright 2020 Springer Nature. (d) Comparison of the responsivity and bandwidth between 2D material on-chip photodetectors and traditional on-chip photodetectors.

application.

TMD-like semiconductor materials, with low dark current and peculiar photoelectric properties, are also used as photosensitive materials [97–102]. Wang et al. [97] integrated a CVD-grown $PtSe_2$ film on a silicon nitride planar waveguide to achieve a response bandwidth of 35 GHz at 1550 nm based on the PC. Li et al. [99] used silicon on both sides of the silicon slot waveguide as the gate electrode, the split-gates modulated mechanically exfoliated few layers $MoTe_2$ to realize a p-n junction, achieving a responsivity of 156 mA·W^{-1} and a response bandwidth of 1.1 GHz at 1353.7 nm based on PV. However, due to the low carrier mobility, TMD materials are difficult to meet the ultra-high bandwidth demands.

The construction of heterojunctions by graphene and other semiconductor materials can effectively reduce dark current and ensure high response bandwidth [103–107]. Flöry et al. [103] integrated a vertically structured $MoTe_2$/graphene heterojunction on a silicon planar waveguide (Figure 5(c)) to minimize the carrier transport path length in $MoTe_2$, achieving a response bandwidth of at least 24 GHz at a bias voltage of −3 V and increasing bandwidth to 50 GHz by applying a higher bias voltage or using a thinner $MoTe_2$. Li et al. [107] constructed graphene-silicon p-i-n photodiodes by placing graphene on the intrinsic, p-doped, and n-doped region of silicon of a subwavelength silicon photonic crystal waveguide at the same time. Based on photo-thermionic (PTI), the ultrafast out-of-plane interface carrier transport and built-in electric-field-assisted carrier collection significantly improved the speed of the device, achieving a response bandwidth of 40 GHz at 1550 nm.

On-chip photodetector based on 2D materials can currently achieve a response bandwidth of up to 110 GHz at the communication band (1500 nm), and the responsivity can reach up to 1000 A·W^{-1}, which is comparable to or even higher than traditional on-chip photodetectors based on germanium [113–115], SiN [116], InP [117,118], and III-V group materials [119] (Figure 5(d)). Meanwhile, the on-chip integration method [120] of 2D materials is simple, can also effectively overcome the problems of lattice mismatch,

and is expected to realize more advanced on-chip optoelectronic device applications.

3.2 On-chip optical modulator

The on-chip optical modulator (Table 3) [121–133] is another key device in the integrated optoelectronic chip, which is responsible for modulating the phase and amplitude of the optical signal to realize the basic function of optical computing. Actual optical calculations require that the optical modulator not only have a good modulation effect (i.e., modulation depth), but also minimize the signal loss caused by modulation (i.e., insertion loss), and the modulation speed (bandwidth) needs to be fast enough to meet the overall operating frequency demands of the chip.

According to the working principle, the on-chip optical modulator of 2D materials mainly contains two categories: electro-optical modulator (EOM) and thermo-optical modulator (TOM). The carrier concentration of the EOMs is adjusted through the electric field and indirectly modulates the absorption effect of 2D materials on the light in the waveguide. TOMs are based on refractive index modulation, utilizing the characteristics of the refractive index of the material as a function of temperature, but due to the inherent slow thermal diffusion, TOMs are slower and are mainly used for optical routing and switching applications. Because the large carrier mobility and the refractive index can be adjusted by the gate, graphene is widely used to construct on-chip EOMs [121–131]. Phare et al. [124] laid CVD-grown graphene on a silicon nitride ring resonator (Figure 6(a)), and the critical coupling effect of graphene and the resonator greatly improved its performance, achieving a modulation depth of 22 dB and a modulation bandwidth of 30 GHz. It is theoretically predicted that through the optimization of high-quality graphene, device structure, and manufacturing process, it could achieve an operating speed of more than 100 GHz and energy consumption below 1 fJ·bit^{-1}. Koestera et al. [125] proposed a concept of an electrically absorbed optical modulator with double graphene layers on the silicon planar waveguide, separated by an insulating medium. The lower graphene acted as a tunable absorption layer and the upper one as a gate electrode. The light absorption effect was modulated by the gate to achieve a modulation bandwidth of more than 120 GHz. Ye et al. [127] designed an electrically absorbed optical modulator with dual graphene-graphene configuration through model calculation, which can achieve a modulation bandwidth of 100 GHz. A high-speed optical phase modulator in a single graphene-graphene configuration [128] was embedded between the two waveguides to enhance the interaction between graphene and light. By applying a bias on the graphene sheet, a π phase shift was achieved in a 75.6 μm-long waveguide structure with a modulation bandwidth of up to 119.5 GHz.

Due to its inherent high thermal conductivity, graphene exists in a variety of thermal applications and can be used in heaters or heat-conductors to build on-chip thermo-optic modulators. Yu et al. [132] used a graphene heat conductor to transfer heat from the metal end to the waveguide, to achieve Mach-Zehnder interferometer (MZI) (Figure 6(b)) and micro-disk relying on its efficient thermal tuning effect. Similarly, Gan et al. [133] also used graphene coatings to improve thermal modulation efficiency on micro-ring resonators, achieving a modulation depth of 7 dB.

Building on-chip optical modulators using 2D materials has obvious advantages due to their wide operating bandwidth, compact size, low operating voltage, ultra-fast modulation speed, and CMOS compatibility. Graphene-based optical modulators can achieve a modulation bandwidth of more than 120 GHz and an insertion loss of 2.5 dB, comparable to traditional InP [134], InGaAsP [135], Ge [136], GeSi [137], and $LiNbO_3$ [138,139] on-chip optical modulators (Figure 6(c)). Graphene-based optical modulators have certain development prospects in the field of optical computing with high-speed modulation requirements and optical routing with high energy efficiency.

3.3 2D material optoelectronic sensing-memory-computing hardware

As an excellent sort of optoelectronic sensing material, 2D material can be used to make a CMOS pixel array by taking advantage of their characteristics of high-quality wafer-level synthesis. Hong et al. [140] used a bilayer MoS_2 film prepared by CVD to construct an 8×8 active pixel image sensor (APS) array, each pixel was composed of a MoS_2 switching transistor and a MoS_2 phototransistor, with a photoresponsivity of up to 119.16 A·W^{-1}. The imaging function of red, green, and blue is successfully realized by using light template projection. Dodda et al. [141] reported a 2D APS technology based on a single-layer MoS_2 phototransistor array (Figure 7(a)), they used only one programmable phototransistor per pixel to drastically reduce pixel cell size (0.09 cm^2 by 900 pixels) and energy consumption (100 fJ·pixel^{-1}),

Table 3 2D material on-chip optical modulator

Materials	Synthetic methods	Mechanism	Modulation depth (dB)	Insertion loss (dB)	Bandwidth (GHz)	Ref.
Graphene	CVD	EOM	4	–	1	[121]
Graphene	CVD	EOM	6.5	4	1	[122]
Graphene	CVD	EOM	2	0.9	35	[123]
Graphene	CVD	EOM	22	8.5	30	[124]
Graphene	CVD	EOM	2.9	2.5	120	[125]
Graphene	CVD	EOM	16	3.3	1.8	[126]
Graphene	Calculation	EOM	34	–	100	[127]
Graphene	CVD	EOM	π	–	119.5	[128]
Graphene	CVD	EOM	5	3.8	6	[129]
Graphene	CVD	EOM	2.2	–	80	[130]
Graphene	CVD	EOM	6.8	18	–	[131]
Graphene	CVD	TOM	–	–	10–6	[132]
Graphene	CVD	TOM	7	–	1.5 μs	[133]

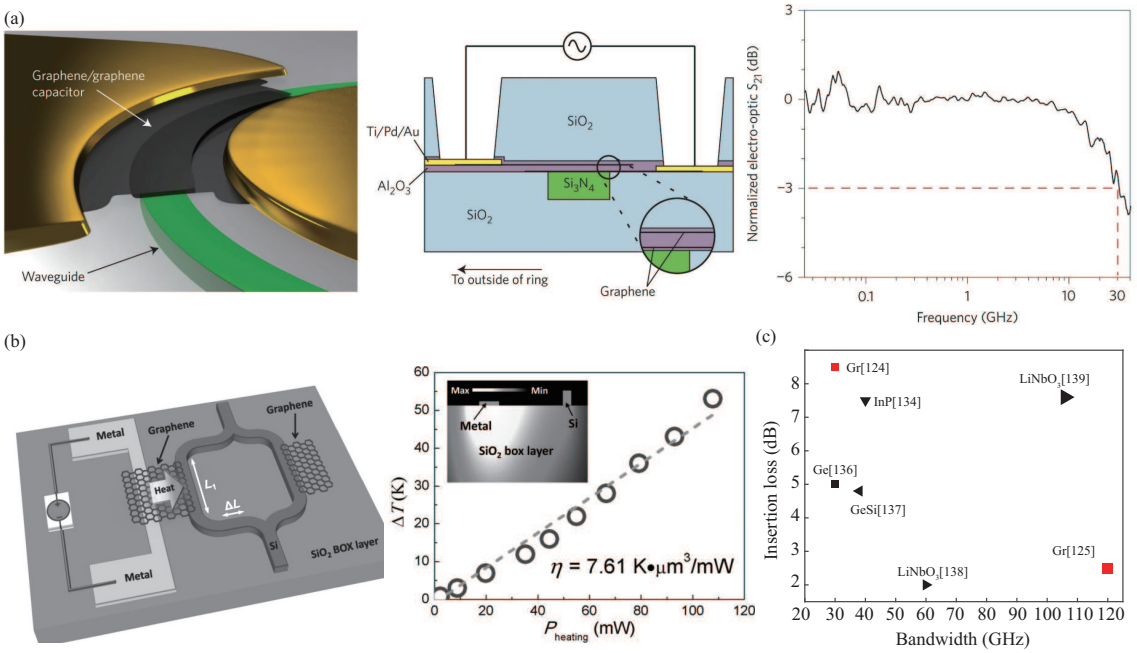

Figure 6 (Color online) (a) 3D diagram and cross-section diagram of graphene optical modulator integrated with ring resonator (left and middle), frequency response results of electro-optical coefficient (right) [124] Copyright 2015 Springer Nature. (b) Three-dimensional schematic illustration of a thermally tuning MZI with a non-local traditional metal heater and a graphene-based transparent flexible heat conductor (left) and temperature change ΔT for the core of the SOI nanowire with varying heating powers (right) [132] Copyright 2014 AIP Publishing. (c) Comparison of modulation bandwidth and insertion loss between graphene-based optical modulators and conventional optical modulators.

providing near-ideal device yield and uniformity. Using gate-tunable persistent photoconductivity, a responsivity of 3.6 × 10^7 A·W^{-1} was demonstrated with a high dynamic range of 80 dB and in-sensor de-noising capability.

As a part of the system, 2D materials can realize monolithically integrated optoelectronic sensing-memory-computing hardware. Goossens et al. [142] monolithically integrated graphene and Si-based CMOS circuit, and then laid PbS quantum dots onto graphene to form a photodetector unit, realizing a 388 × 288 image sensor array (Figure 7(b)). Based on graphene's heterogeneous integration ability, high mobility, and wide spectrum detection range, together with a mature CMOS signal readout and pre-processing circuit, a high-resolution broadband-sensitive digital camera was realized. Taking advantage of the tunability of 2D materials can also simplify the pixel processing circuit. Zeng et al. [143] used a WSe_2 transistor with dual gates upon and beneath to implement drain-source voltage control of AND and XNOR logic switching, performing image intersection and image comparison tasks through a 3 × 3 array (Figure 7(c)) with 16% of the energy consumption less than conventional circuits. Dodda et al. [144]

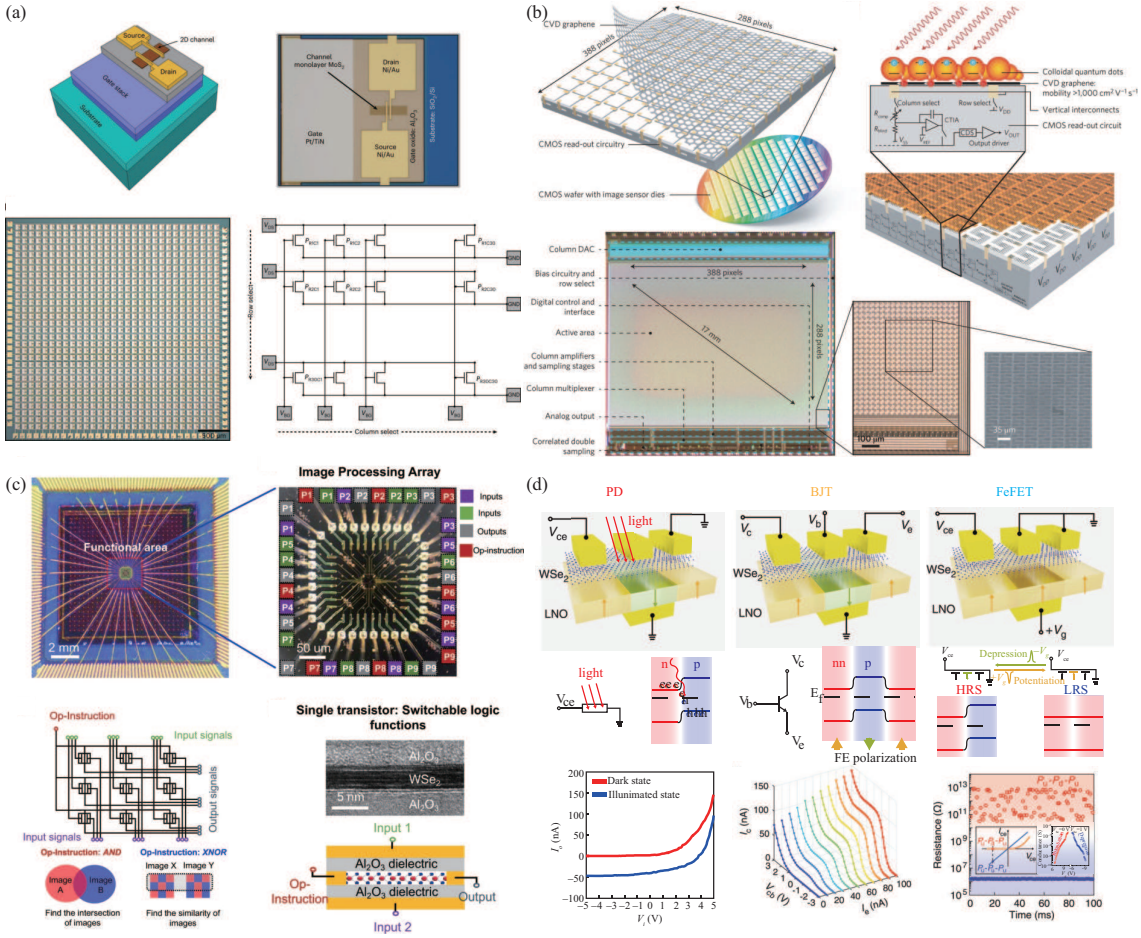

Figure 7 (Color online) (a) 3D schematic and optical image of a monolayer MoS_2 phototransistor integrated with a programmable gate stack (top), the optical image of a 900-pixel 2D APS sensor fabricated in a crossbar architecture and the corresponding circuit diagram showing the row and column select lines (bottom) [141] Copyright 2022 Springer Nature. (b) Schematic diagram (top) and physical diagram (bottom) of photoelectric sensor chip integrated with PbS quantum dot, graphene, and silicon-based CMOS readout circuit [142] Copyright 2017 Springer Nature. (c) Macroscopic and detailed image of the bonded device on the carrier, which consists of 3 × 3 pixels (top), schematic circuit diagram of the pixel processing array and single-pixel processing unit with its cross-sectional high-resolution TEM image (bottom) [143] Copyright 2022 Springer Nature. (d) The device structure diagram, band structure diagram, and test result diagram of the photodetector, BJT, and ferroelectric FET based on $LiNbO_3$ modulated WSe_2 homogeneous architecture [145] Copyright 2021 AAAS.

used CVD-grown single-layer MoS_2 to build a memtransistor, which combines computing, storage, and photoelectric sensing capabilities, and used the light-induced subthreshold mechanism of the memtransistor to realize a low-energy encryption engine of several hundred picojoules. Tong et al. [145] proposed a homogeneous architecture based on the structure of the ferroelectric lithium niobite (LNO)-modulated bipolar WSe_2, which can function as analog signal preprocessing cells such as BJTs and non-volatile memory cells (Figure 7(d)). It simplified the matching circuit requirements between each module and demonstrated the binary classification function of letter images, which would facilitate further research on neuromorphic hardware.

By imitating the structure and function of the biological vision system, designing and preparing 2D materials-based optoelectronic sensing-memory-computing integrated hardware to perform visual neuromorphic functions is the main idea of realizing an intelligent vision system [146–148]. At present, artificial vision systems based on 2D materials have been extensively studied, and the corresponding structures and methods for device realization are found by analyzing the functions of biological visual systems. For light and dark vision, the cones and rods in the human retina have a strong perception of strong light and weak light, respectively, and form a neural circuit through horizontal cells to regulate the dominance of the two in different environments, to realize the adaptive function of light intensity. Liao et al. [149] used a MoS_2 phototransistor that introduces a charge trap state to dynamically adjust the photosensitivity, time-varying excitation, and inhibition characteristics of the device under different lighting conditions,

which can simulate the adaptive perception adjustment of the human eye to strong and weak light (Figure 8(a)), creating an effective perception range of up to 199 dB. An 8 × 8 transistor array combined with neural network algorithms achieved an image recognition accuracy of about 97%.

For color vision, only cones are distributed in the fovea of the human retina to distinguish and recognize red, green, and blue light, and color recognition can be achieved by superimposing the biological currents of three different light-sensitive cones. Seo et al. [150] proposed a pixel unit (Figure 8(b)) based on a WSe_2 photoelectric transistor in series with an hBN/WSe_2 memtransistor, which had an order of magnitude difference in response currents under RGB light and an adjustable conductance weight, respectively. Through online training of optical neural networks based on a 28 × 28 array, it achieved a mixed color recognition rate of up to 90% based on reducing the complexity of peripheral circuits.

For motion vision, each cone cell at the fovea of the retina is connected to a bipolar cell, which is used to adjust the strength of the sensed signal to realize pixel-level responsivity control. Visual information is pre-processed through the signal differential action between adjacent pixels, thereby accelerating the extraction speed of features for object edge detection. Wang et al. [151] used the gate voltage to adjust the interface charge between hBN and Al_2O_3 to achieve the positive and negative photoconductivity response of the WSe_2 device. The structure of the OFF-state unit surrounded by the ON-state cell was adopted on the array, and the significant extraction of light and dark information was realized through signal difference, to detect the edge of the object (Figure 8(c)). Similarly, the object-tracking ability also depends on the bipolar cells modulating the cones. The time-related light and dark information of the object will be contrasted before and after (the background is subtracted without responding in this process), and the moving area will generate bioelectric pulses due to significant changes in light and dark information, thereby realizing the detection of moving objects [152, 153]; Zhang et al. [154] used a black phosphorus floating-gate FET with WSe_2 as floating gate layer, which can sense optical stimulation, to generate a progressively adjustable positive/negative photoconductivity response. It achieved 100% separation detection combined with inter-frame differential calculation (Figure 8(d)). Input the detected moving image into the conductance mapping neural network, cart recognition was realized in just 4 epochs at a noise level of 10%.

For image recognition, not only the retina needs to perceive and preprocess the information, but also the parallel structure of the visual cortex needs to be used to achieve rapid recognition. Mennel et al. [155] proposed a WSe_2 split-gate modulated photodiode, by using gate-voltage modulated responsivity as weight, a 3 × 3 pixel array combined with a single-layer neural network algorithm (Figure 8(e)) was used to achieve effective and rapid recognition and automatic encoding of letter information.

In summary, to deeply simulate the structure and function of a biological visual system, biological effects such as parallel image processing, fast accurate recognition, and low power consumption must be obtained. The bio-inspired vision system of 2D materials [156, 157] is being developed in the direction of device function integration, large-scale hardware, and application diversification.

4 Conclusion and outlook

High-quality wafer-level material synthesis, transfer, and device fabrication techniques for 2D materials are becoming increasingly mature, thus a large number of integrated hardware based on them have been demonstrated. Thanks to the flat surface without dangling bonds, atomic-thick 2D materials can still maintain high carrier mobility. They can meet the performance requirements when the device is scaled to the atomic level, and continue the development of high integration and high performance of semiconductor ICs. Their interlayer van der Waals force and single-layer stability promise heterogeneous integration. The physical characteristics are rich due to atomic thickness and easily adjustable by an external field, providing more diverse device functions and application scenarios. They can be used as the sensitive layer to achieve the improvement of sensor performance by hetero-integration with mature silicon-based CMOS technology. Combined with optical structure, the on-chip photoelectric conversion device can surpass the traditional ones in better performance. Therefore, the hetero-integration of 2D materials becomes a colorful link in the future information technology field. For the emerging field of brain-like neuromorphic hardware, the integration of photoelectric sensing, logical computing, and signal storage functions based on 2D materials is also no less important, which is one of the good platforms to realize the next generation of information technology applications. However, preparing methods of a variety of high-quality 2D materials single-crystal films, non-destructive material transfer methods,

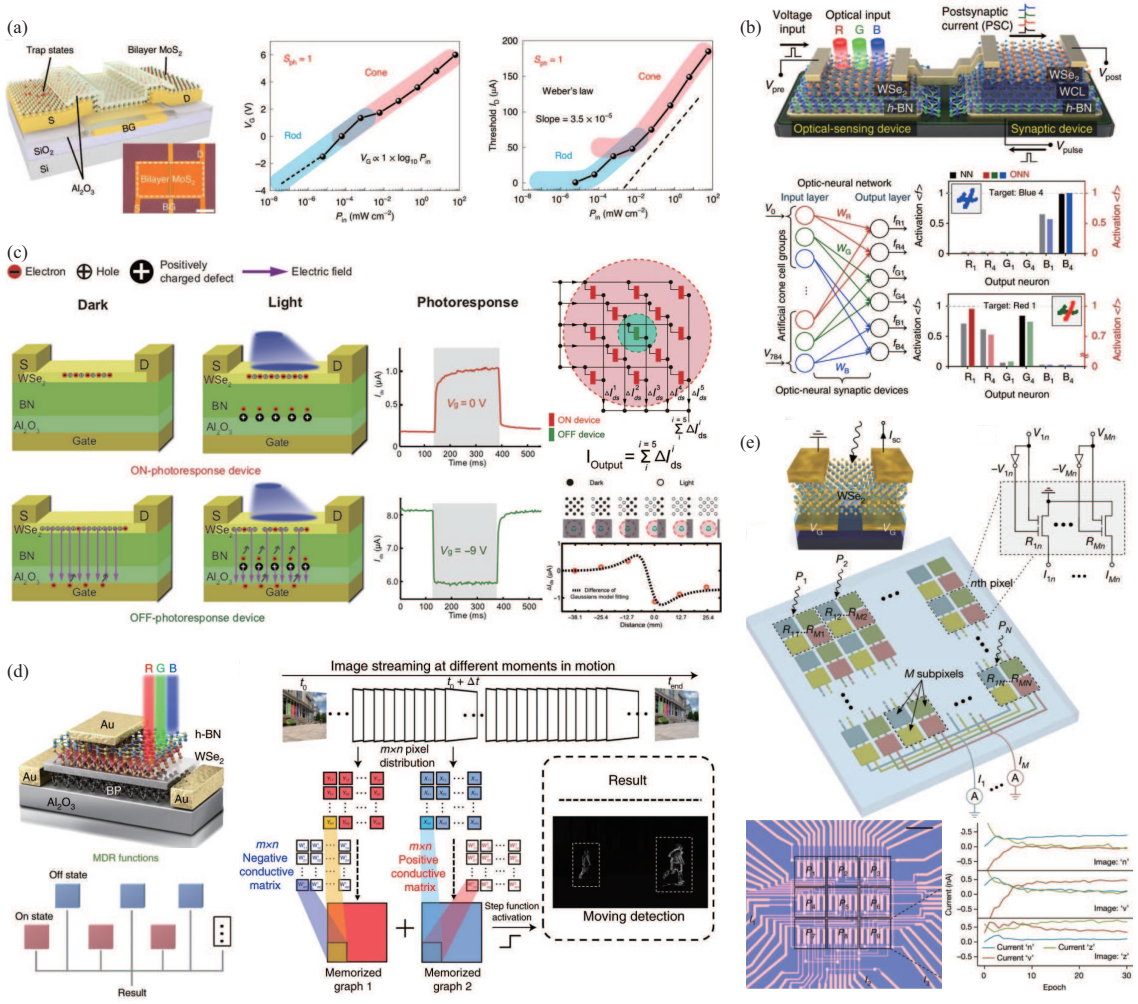

Figure 8 (Color online) (a) 3D diagram of molybdenum sulfide phototransistor and the test results of incident light intensity correlation (scale bar, 100 μm) [149] Copyright 2022 Springer Nature. (b) 3D schematic of the photoelectric synaptic device (top) and its neural network and mixed color training test results [150] Copyright 2018 Springer Nature. (c) Schematic diagram and response results of positive and negative photoconductance responses of retinal morphologic devices (left), array configuration, and current test results of simulated foveal structure (right) [151] Copyright 2020 AAAS. (d) 3D schematic diagram and motion detection and recognition schematic diagram of the retinal morphological device (left) and motion detection and recognition scheme (right) [154] Copyright 2022 Springer Nature. (e) Schematic diagram of the ultrafast vision sensor array (including unit device), circuit diagram (top), physical diagram (scale bar, 15 μm) and letter training recognition results (bottom) [155] Copyright 2020 Springer Nature.

interface and electrode contact schemes to ensure material properties, and the design of novel non-von Neumann architecture circuit systems are still challenging.

For the synthesis of wafer-scale 2D materials, there is a lot of work showing the preparation technology of high-quality single-crystal thin films (graphene [27–29], BN [30–32], and TMD [33–35]). It has been verified to prepare single crystal materials which meet the performance requirements through the laboratory. However, integration applications have much stricter requirements on the stability and difference of devices as well as preparation costs to meet commercialization conditions. For the transfer method, manual wet transfer [36–38] is usually adopted in the lab. Some advanced ones [39–41] will rely on some simple auxiliary tools or optimize the process parameters (such as the thickness of the organic film and spin coating speed and time). However, the success rate is often not high enough, and wrinkles and organic residues are inevitably introduced in the transfer process, which will seriously affect the large-scale preparation of 2D material devices and hinder the further improvement of hardware functions. For the electrode contact, many special methods have been proposed, including transfer electrode [49–53] and evaporation of semi-metallic materials [45], which can effectively reduce the role of gold semi-contact resistor. However, the success rate and accuracy of the transfer electrode need to be further improved, and the supporting process instruments need to be developed. At present, the integration schemes of

2D materials are mostly based on traditional ones. High cost and low economic benefits from process adaptability hinder their development path.

To further promote the application of 2D materials integrated hardware, it is necessary to make full use of the advantages of existing mature CMOS technology by combing it with the commercial environment. It is preferred to link the functions of 2D materials with new semiconductor information devices, systems, and applications to create unique applications. For electronic devices (including ICs and transistor arrays), scale application is the key, so the preparation of high-quality wafer-scale 2D materials is the primary focus. We do believe that growing 2D materials directly on the substrate will be more suitable for its application than transfer. It will be mainly considered to select the proper metal and adjust the evaporation process for electrode contact. As the transfer electrode technology needs to be further optimized to meet the requirements of high-precision large-scale preparation. And optoelectronic devices (including on-chip photodetector and optical modulator), the preparation of unit devices with high-quality materials is the key. Therefore, we think it is more suitable to transfer 2D materials grown on the optimal substrate. Direct growth will greatly affect other optical structures. The electrode transfer method is more effective to choose without considering scale.

2D materials are promising to be a candidate for new non-von architecture hardware due to their rich semiconductor properties. Through the collaborative design of hardware and algorithm structure, the development of application-oriented special neuromorphic computing hardware will be the mainstream direction of 2D material integration in the future. Back to reality, 2D material synthesis, transfer, electrode evaporation, other process manufacturing equipment, and production lines need to be set up, as well as the design of new architecture circuits to achieve this vision.

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