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• **Supplementary File** •

Modelling and physical mechanism analysis of the effect of polycrystalline-ferroelectric gate on FE-FinFETs

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Appendix A Multi-Grain Ferroelectric Model

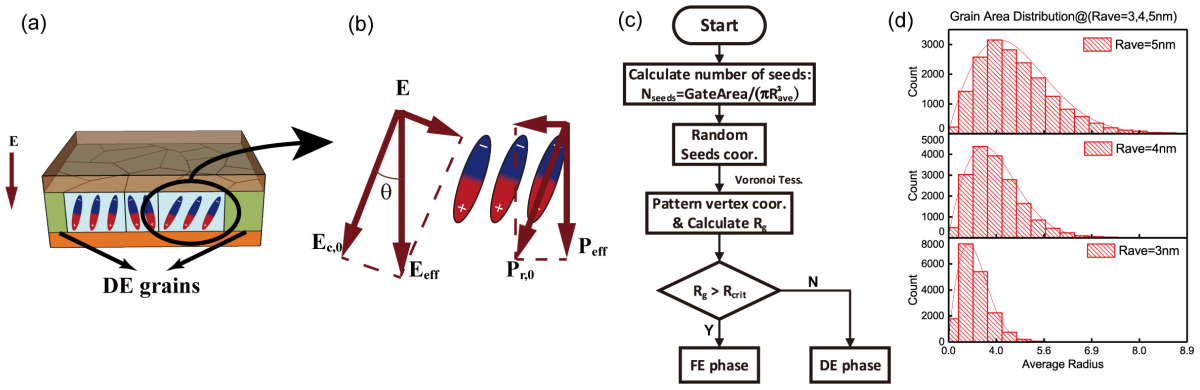

Figure A1 (a) Schematic of MG FE film including different grain shape, phases and orientations. (b) Detail schematic of the electric field and polarization of a FE grain with an angle (θ) between grain orientation and electric field. (c) The flow of data process and grain phase judgement. (d) Grain size distribution with different R_{ave}, observed from the simulation of MGFE model.

According to the microstructure of HfO_2-based FE film observed in experiments [1], a textured film reveals the grain variation in phases and orientations. Therefore, a MG FE film model is established, considering irregular grain shapes, different grain phases and grain orientations, illustrated in Figure. A1(a). redPrimarily, in order to generate irregular grains, the site saturation nucleation kinetics is referred to describe the crystallization process of a MG film [2–4] and Voronoi tessellation is utilized to generate irregular polygons, where the Voronoi tessellation is a common algorithm for plane segmentation [5] and was validated with the help of earlier reported Monte Carlo simulation [6]. Voronoi diagram is composed of a set of continuous polygons, whose boundary is delimited by the vertical bisectors connecting two adjacent seed points. Here, the random seeds follow uniform distribution in both X and Y directions. The modeling process is carried out in Matlab, and then a Bash Shell script is used to stitch the MGFE model into TCAD for simulations. As shown in Figure. A1(c), the flow of data process and split can be described as follow. Firstly, by fixing the average radius (R_{ave}) of grains, the amount of grains in a finite area FE film can be calculated. Secondly, a set of random seeds coordinates are determined on the gate FE layer of the FinFET according to the number of grains, and then the tessellation is done to generate the pattern of FE layer containing vertex coordinates. Figure A1(d) shows the statistical distribution of grain size with different R_{ave}, which is similar to the experimental data [7]. Thirdly, the area of each grain is calculated, and its grain radius (R_g) is denoted by calculating the effective radius of a circle with the same area (S_g) as this grain:

$$R_g = \sqrt{\frac{S_g}{\pi}} \tag{A1}$$

Referring to the results of theoretical calculation and experimental data, the film thickness and grain size can affect the formation of FE phase due to the surface or grain boundary effect [7], the orthorhombic (O) phase is stabilized in a specific film thickness and grain size region [8–10]. According to the computing results of Tang et al. [9] in a 2nm $Hf_{1-x}Zr_xO_2$ film (used in this work), there are mainly O and tetragonal (T, equivalent to DE pahse, under the gate voltage in this work) phase grains, and the grain

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size of T phase is slightly smaller than that of O-phase. To reflect this phenomenon, in this work, the grain phase is judged by a critical radius (R_{crit}), when R_g is smaller than R_{crit}, the grain is DE (T) phase, otherwise, the grain is FE (O) phase. Thus, the ratio of FE and DE phase in the model can be adjusted by the relationship between R_{crit} and R_{ave}. Considering the existence of DE phase, the total capacitance of MG FE film (C_{Total}) should be calculated as a parallel circuit of DE capacitance (C_{DE}) and FE capacitance (C_{FE}):

$$C_{Total} = \sum_i C_{DE,i} + \sum_j C_{FE,j} \tag{A2}$$

$$C_{DE,i} = \epsilon_{DE} \cdot \frac{S_{DE,i}}{T_{FE}} \tag{A3}$$

where ϵ_{DE} is the permittivity of DE phase, T_{FE} is the thickness of FE film and $S_{DE,i}$ is the area of a DE grain, C_{FE} will be expressed later.

Regarding the grain (domain) orientation, it is characterized by an angle θ between the grain orientation and the out-of-plane direction in the MGFE model. The spatial distribution of θ is set to Gaussian distribution [1], which is the most common distribution mode. The difference between grain (domain) orientation and external electric field vector causes the distinguished ferroelectric properties (remnant polarization P_r and coercive electric field E_C) from grain to grain [11, 12]. As described in Figure. A1(b), with an angle θ between polarization and applied electric field, the intrinsic P-E characteristics have to be adjusted. According to the Parallelogram Law (PL), only the part of the external electric field (E_{eff}) along polarization works, and the vertical polar component (P_{eff}) is essentially effective in terms of MOS potential [13]. Therefore, the observed E_{eff} and P_{eff} can be obtained:

$$P_{eff} = P_{r,0} \cdot \cos\theta, \quad E_{eff} = \frac{E_{C,0}}{\cos\theta} \tag{A4}$$

where $E_{c,0}$ and $P_{r,0}$ is the intrinsic coercive field and intrinsic remnant polarization, respectively.

In order to apply the MGFE model in FE-FinFETs, simplified Landau-Khalatnikov (L-K) model is employed:

$$E_{fe} = 2\alpha P + 4\beta P^3 \tag{A5}$$

$$\alpha = -\frac{3\sqrt{3}}{4} \cdot \frac{E_C}{P_r}, \quad \beta = \frac{3\sqrt{3}}{8} \cdot \frac{E_C}{P_r^3} \tag{A6}$$

α and β are FE material parameters [14]. Combined with MGFE model, the L-K model can be modified as equation (A7) to describe the MG effect and C_{FE} can be expressed as equation (A8), $S_{FE,j}$ is the area of a FE grain.

$$\alpha = -\frac{3\sqrt{3}}{4} \cdot \frac{E_{C,eff}}{P_{r,eff}}, \quad \beta = \frac{3\sqrt{3}}{8} \cdot \frac{E_{C,eff}}{P_{r,eff}^3} \tag{A7}$$

$$C_{FE,j} \approx \frac{S_{FE,j}}{2 \cdot \alpha \cdot T_{FE}} = -\frac{2\sqrt{3} P_{r,0} \cdot \cos^2\theta}{9 \cdot E_{C,0} \cdot T_{FE}} \cdot S_{FE,j} \tag{A8}$$

In the previous work, we developed a 7-nm n-channel FinFET simulation deck [15], demonstrating its current-voltage characteristics calibrated against the experimental data of 7-nm FinFET CMOS technology of GlobalFoundries and Samsung [16, 17]. Based on this 7-nm FinFET platform and L-K model, we developed a 7-nm n-type FE-FinFET TCAD model. Figure. A2(a) shows the structure of an ideal single grain (SG) FE-FinFET for simulations, the parameters of FE gate layer are assignable and the P_r and E_C in this work are set as $15\mu C/cm^2$ and 1MV/cm referred to the related reports of state-of-the-art FE-FinFET [18–20], the detailed parameters of baseline-FinFET and FE layer are described in Table A1. For the less advanced nodes that already have experimental data of FE-FETs, the model can be calibrated against the experimental data of FEFETs directly. The inset of Figure. A2(a) shows the cross-section schematic of FE-Fin where metal-ferroelectric-insulator-Si (MFIS) structure is used in this work. The interface layer in this work is considered as an ideal layer, nevertheless, the uncontrolled thickness and permittivity in practical devices would introduce a new variability source, which deserves further detailed research. Figure. A2(b) shows the I_{DS}-V_{GS} curves of baseline-FinFET and SG FE-FinFET. The FE gate exhibits NC effect at subthreshold region leading to the amplification of gate voltage (V_G), the SS of FE-FinFET at room temperature is smaller than that of baseline-FinFET, and it is lower than 60mV/dec at low drain-voltage (V_{DS}). The emergence of NC effect is due to the matching of C_{FE} and C_{MOS}, which can be explained by Landau theory [21, 22]. In addition, the short channel effect is improved obviously, the drain-induced barrier lowering (DIBL) of FE-FinFET is suppressed and the off-state current of FE-FinFET is nearly an order of magnitude lower than that of baseline device. Figure. A2(c) exhibits the output characteristic of SG FE-FinFET with an obvious negative differential resistance (NDR) phenomenon. According to the previous research, the inhibition on DIBL and the existence of NDR are caused by the coupling between ferroelectric negative capacitance and intrinsic capacitance of FinFET [23].

Appendix B MGFE-Induced Statistical Variabilty of FE-FinFET

In the following, as shown in Figure. B1(a), the MGFE microstructure patterns and modified L-K model are introduced into the FE-FinFET to investigate the effect of polycrystalline FE gate. Figure. B1(b) shows two typical MG FE layers with different patterns, generated for simulations using the above method. As described in the MGFE model, R_{ave} determines the number of grains of the FE film, and R_{crit} is the critical condition judging which grains are FE phase. In addition, Referring to the experimental data, in HfO_2-based film the average grain size is comparable or slightly larger than the film thickness [8, 10, 24]. Thus R_{ave} is set to 3nm (the thickness of FE layer in our simulation device is 2nm), and to achieve an opportune FE/DE ratio, R_{crit} is set to 1.5nm (the ratio of FE/DE can be changed by the value of R_{crit}). R_g and grain orientation (θ) both follow Gaussian distributions. Figure. B1(c) displays 100 simulation results of transfer characteristic curves of MG FE-FinFETs with distinct FE layer patterns, and the MG effect induces the variation of FE-FinFET transfer characteristics in both electrostatics and drive-currents obviously. Compared with the SG FE-FinFET, the SS in the most MG FE-FinFETs is steeper, and the on current (I_{on}) is larger. Then, the individual effects of FE/DE ratio and FE grain orientation on the key electrical FoM fluctuations of MG FE-FinFETs are investigated, respectively. The variation introduced by FE/DE ratio is investigated at first, assuming the vertical angle of polarization to avoid the influence of grain orientation. The electrical transfer characteristics of I_{DS}-V_{GS} curves of

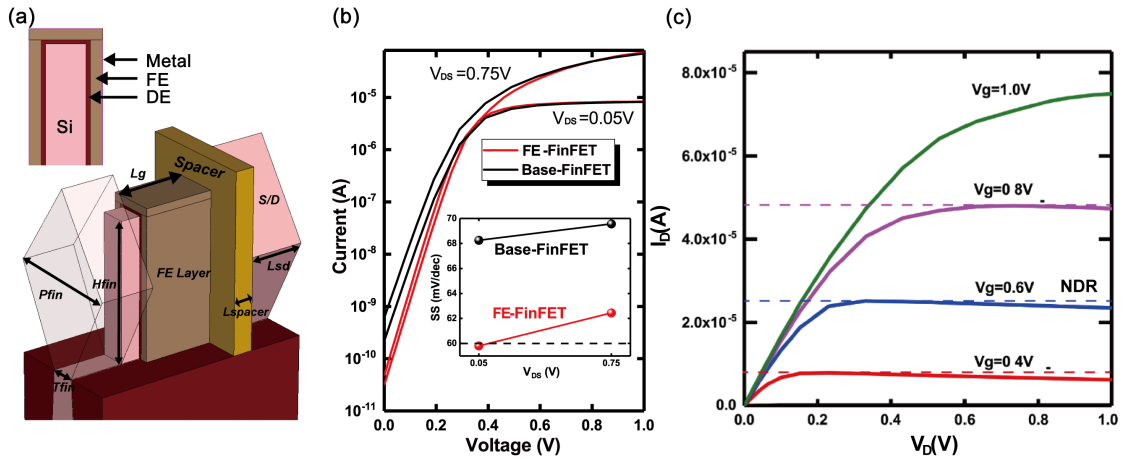

Figure A2 (a) The structure of FE-FinFET for simulation. The inset is the cross-section schematic of FE-Fin. (b) The comparison of transfer characteristic between baseline-FinFET and SG FE-FinFET at different V_{DS}. The inset is the comparison of SS. (c) Output characteristic of SG FE-FinFET.

Table A1 Device Structure and Ferroelectric Parameters

Parameter	Description	Value
L_g	Gate Length	16nm
H_{fin}	Fin Height	35nm
L_{sd}	Rasied S/D length	14nm
L_{spacer}	Spacer Length	5nm
L_{ov}	Gate Overlap Length	1nm
EOT	Equivalent Oxide Thickness	1nm
N_{epi}	Raised S/D n-Type Doping Concentration	1E20(cm^{-3})
N_{ch}	Channel p-Type Doping Concentration	5E17(cm^{-3})
N_{sub}	Substrate p-Type Doping Concentration	1E18(cm^{-3})
N_{ext}	Extension Region Doping Profile	Gaussian Profile
T_{fin}	Fin Thickness	7nm
T_{fe}	Ferroelectric Layer Thickness	2nm
$P_{r,0}$	Intrinsic Remnant Polarization	15$\mu C/cm^2$
$E_{C,0}$	Intrinsic Coercive Field	1MV/cm

statistically generated 100 samples with different grain patterns upon the uniform FinFET are simulated following the simulation framework in Figure.A1(c), respectively for MG NC-FinFETs with R_{crit}=1.5, 2 and 3 nm. Figure. B2 presents the histogram distributions of the device FoM including SS, V_{th}, I_{on} and I_{off} with different R_{crit}. The increased proportion of DE grains boosts the variability of MG FE-FinFETs simultaneously, when the R_{crit} is large enough (R_{crit}=3nm) to be comparable to the average FE grain size, the proportion of DE phase significantly increases, as a result dramatically deteriorating the variation of device performance.

Similarly, excluding the influence of FE/DE ratio (average R_g is set to 3nm and R_{crit} is set to 1.5nm) the grain orientation variation is highlighted. The standard deviation of θ (σ_θ) of FE grains orientation is adopted to indicate the variation magnitude. A wide range of statistical TCAD samples are investigated, and each 100 samples respectively with σ_θ=0°, 15°, 20° and 25° are generated and their electrical characteristics are simulated. Figure. B3 describes the statistical simulation results of SS, V_{th}, I_{on} and I_{off} with different grain orientation distributions. It is evident that the larger standard-deviation brings better overall performance of MG FE-FinFETs in terms of I_{on}, I_{off}, I_{on}/I_{off}, SS, and V_{th}, but it obviously worsens variations of almost all FoMs. This phenomenon is due to that a better FE/DE capacitance matching can be achieved with the decrease of P_r and E_C derived from θ varying, which enhances the NC effect. However, A larger σ_θ renders a more random distribution of L-K coefficients ($P_{r,eff}$ and $E_{c,eff}$), and greater variations of electrical characteristics in MG FE-FinFETs. Noticeably, when σ_θ exceeds 15°, the σV_{th} will increase sharply and in the same order of magnitude as the influence of traditional variability sources.

Appendix C Physical Mechanism Analysis

In order to investigate the physical mechanism about how the MG FE gate layer introduces the device-to-device variation into FE-FinFET performance, the electrostatic potential distribution of channel surface and the polarization distribution of FE gate are analyzed. Figure. C1 shows the polarization distribution of FE layers on both sides of a fin which are extracted from one of a case in different MG FE-FinFET devices. In the simulation, the two face-to-face FE layers deposited on both sides of a fin, upon applied the field, exhibit the opposite polarization direction in the same coordinate system, giving the positive and negative polarization-signs of two FE layers. Meanwhile, the FE polarization magnitude of FE layer due to the varying orientation exhibits irregular distribution, and particularly the green spots at gate represent the DE grains, with non-FE properties. Since the DE phase does not provide voltage amplification effect, the DE grains together with weak FE ones with large θ will generate potential

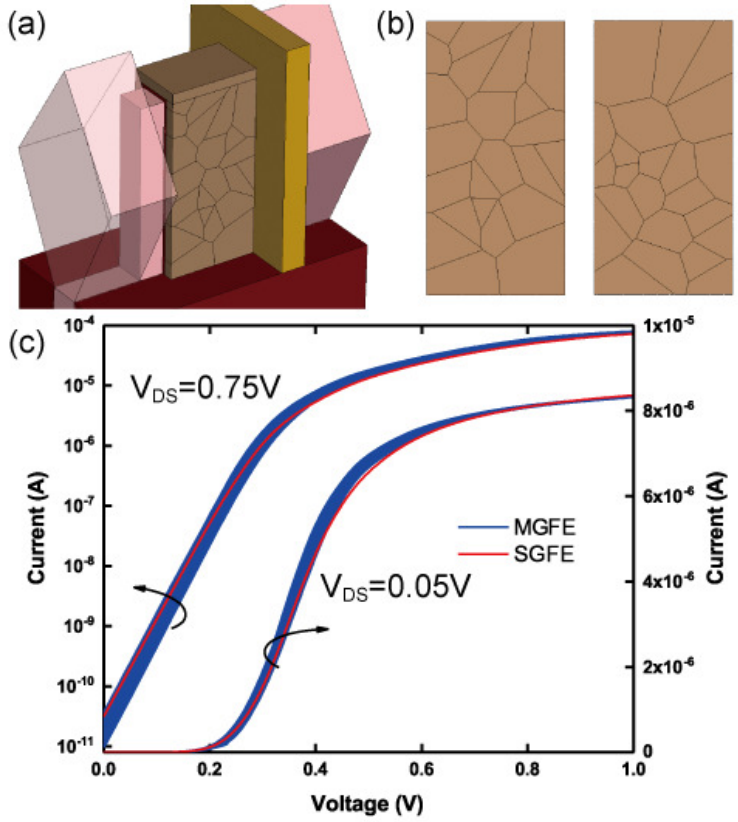

Figure B1 (a) The structure of MG FE-FinFET. (b) Grain patterns of MG FE layer on the both side of fin in a MG FE-FinFET. (c) The transfer characteristic of SG FE-FinFET and that of 100 MG FE-FinFETs with different FE layer patterns.

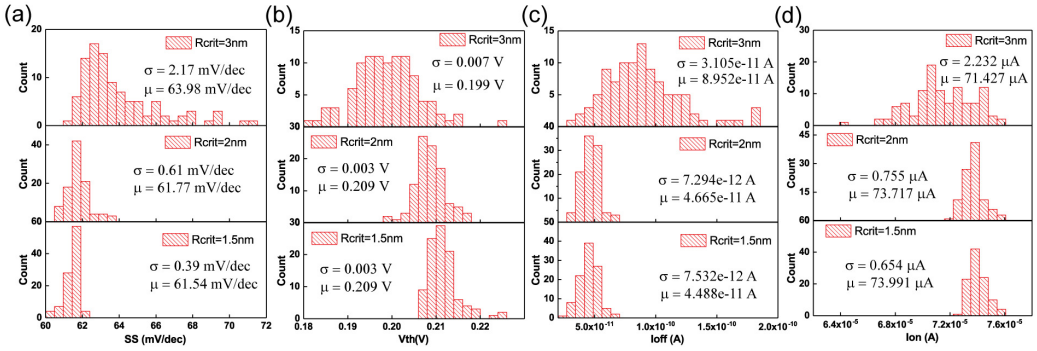

Figure B2 Distributions of the FoM with different critical radius, R_{ave}=3nm and all grain orientations are perpendicular to the channel surface.

valleys on the silicon surface-potential landscape, constituting the original variation sources introduced by polycrystalline FE gate. Generally, the irregular grains' distribution of FE film will weaken variation by averaging over the large dimensions.

Devices with extreme electrical parameters induced by polycrystalline FE gate are captured from the statistical simulation. Figure. C2(a) and (b) exhibit the electrostatic potential of MG FE-FinFETs with minimum I_{on} and maximum I_{on}, introduced by the different ratio of FE/DE grains. Interestingly, except for the ratio of FE and DE grains, the position of FE and DE grains are also influential to the device-to-device variation. For the device with the largest I_{on}, the most FE grains are close to the source and DE grains are mostly close to the drain. A larger FE polarization is obtained than that most FE grains are close to the drain, leading to the larger voltage amplification and higher channel potential. On the contrary, when the DE grains occupy the position at the source end and FE grains close to the drain, the FE gate layer will lose part of the voltage amplification ability. Meanwhile, the electrostatic potentials of extreme devices induced by grain orientation are analyzed as in Figure. C2(c) and (d), while FE grains with the strong out-plane polarization approximate the source terminal and FE grains with weak out-plane polarization locate near the drain, the MG FE-FinFET can acquire the largest I_{on}. In summary, the coupling of the ratio of FE/DE and the orientation of FE grains with the space distribution of grains leads to the statistical variability of MG FE-FinFETs. In particular, the extreme grain-distribution would result in the extreme electrical characteristics.

In fact, for the small dimension FinFETs, not only the average effect will decrease, but also the coupled voltage of V_D on the

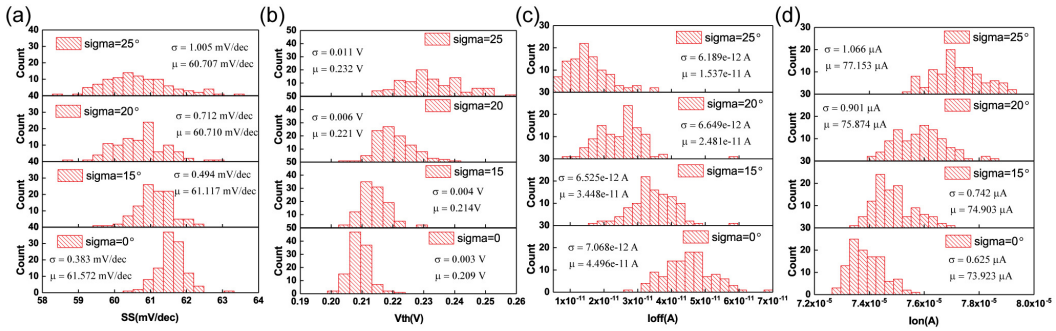

Figure B3 Distributions of SS, V_{th}, I_{off} and I_{on} with different grain orientations, R_{ave}=3nm and R_{crit}=1.5nm.

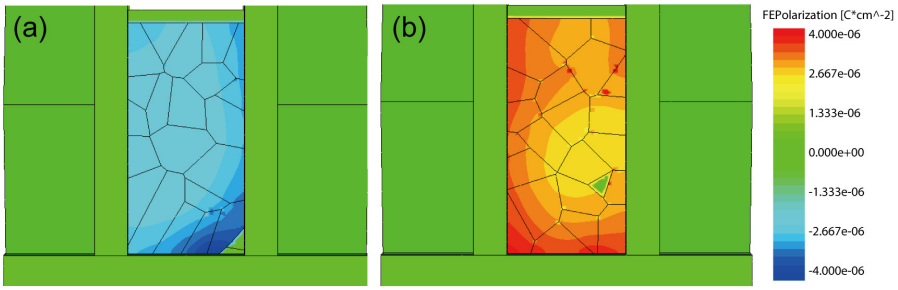

Figure C1 The porlarization profiles of FE layers on both sides of the fin. Green regions represent the DE-phase grain, while the nonuniform FE polarization results from FE-grain orientation variation. The FE layers on both sides is polarized towards or outwards the fin.

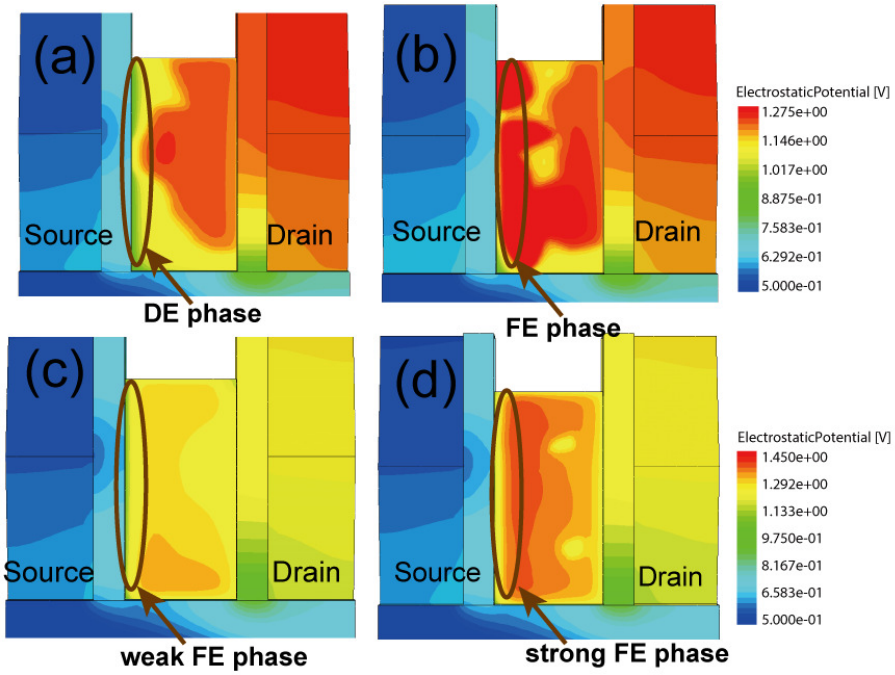

Figure C2 The electrostatic potential of devices with extreme electrical parameters induced by FE/DE ratio, (a) device with minimum I_{on}, and (b) device with maximum I_{on}. The electrostatic potential of devices with extreme electrical parameters induced by grain orientation, (c) device with minimum I_{on}, and (d) device with maximum I_{on}.

FE gate layer will further exacerbate the variability induced by polycrystalline FE gate. Figure. C3(a) schematically illustrates the local capacitance net of FE-Fin close to the drain terminal, including outer fringe capacitance (C_{of}), FE layer capacitance (C_{fe}) and gate oxide capacitance (C_{ox}). Drain potential will be coupled to the interface between FE and oxide layer through C_{of} and C_{ox}, enhancing the internal voltage (V_{int}). Thus, even with well electrostatic isolation, the channel potential close to the drain terminal will be raised by the parasitic capacitance. As shown in Figure. C3(b), due to the asymmetry channel electrostatic

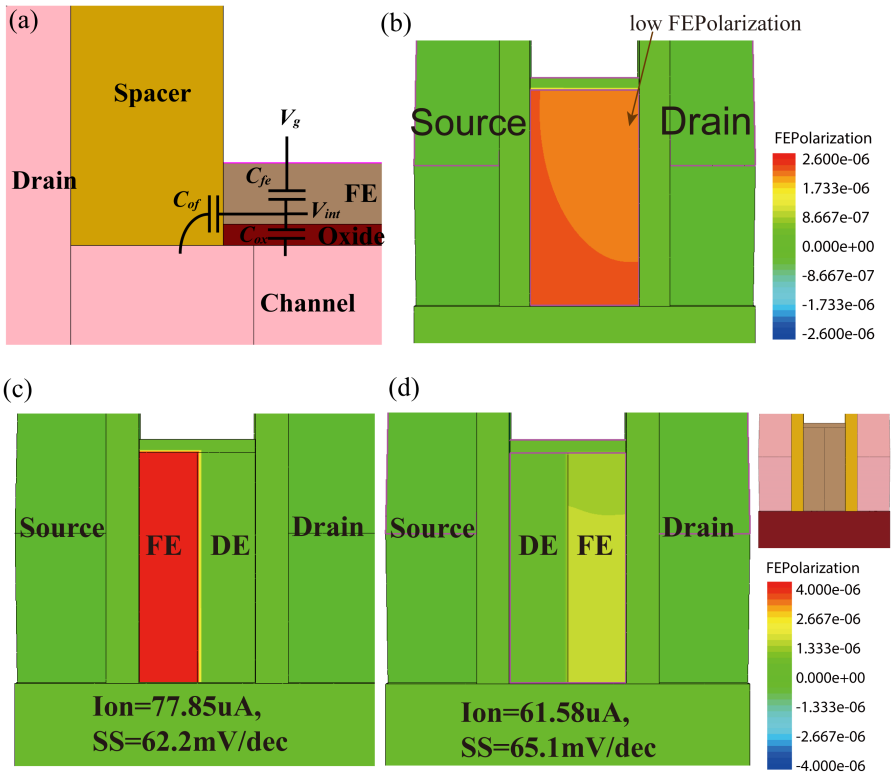

Figure C3 (a) The schematic of local capacitance net of FE-Fin close to the drain terminal. (b) The FE polarization of SG FE-FinFET with VDS=0.75V. Two extreme cases of FE polarization with only two grains of FE/DE in opposite positions, with VDS=0.75V, (c) FE grain is located close to the source, while (d) the FE grain is located close to the drain.

potential, the FE polarization in the SG FE-Fin near the drain is weakened. This phenomenon indicates that the FE polarization is affected by the spatially distributed potential difference, varying rather than a fixed value transversely, even for the SG FE gate. Therefore, for the MG NC-FinFETs, because of the asymmetric electrostatic potential distribution as mentioned above, the location of DE grains or large angle FE grains will also affect the performance of MG NC-FinFETs. In order to clarify the effect of grains-distribution in MG FE gate, two experimental extreme cases are simulated which could help understanding the behavior of DE grains in MG NC-FinFETs. As presented in Figure. C3, the FE film is divided into two shoulder-to-shoulder grains of either FE or DE phase, where the FE grain with suitable ferroelectric parameters (E_C=1MV/cm, P_r=15μC/cm^2) can amplify the internal gate-voltage while DE grain only adds capacitive voltage division. Comparing the two location scenarios of FE/DE grains in terms of next to source or drain side in Figure. C3(d) and Figure. C3(c), when the FE grain is close to the source terminal, the polarization of FE grain will be larger than the opposing situation, and the device will present lager I_{on} and steeper SS. Therefore, it can be inferred that when the FE grains are distributed near the source terminal, the voltage amplification effect of the FE gate will be stronger than in the opposite case. It is worth noting that these effects are valid also for the state-of-the-art planar and nanosheet devices, due to the area of FE gate layer being small enough to reduce the averaging effect to underline the polycrystalline effect of FE gate.

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