SCIENCE CHINA
Information Sciences

• LETTER •

May 2023, Vol. 66 159402:1–159402:2
https://doi.org/10.1007/s11432-021-3490-3

A $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric capacitor-based half-destructive read scheme for computing-in-memory

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Received 29 December 2021/Revised 28 February 2022/Accepted 25 April 2022/Published online 4 April 2023

Citation Zhao Y L, Wang Y, Zhang D L, et al. A $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric capacitor-based half-destructive read scheme for computing-in-memory. Sci China Inf Sci, 2023, 66(5): 159402, https://doi.org/10.1007/s11432-021-3490-3

The emerging non-volatile memories (NVMs), including resistive random access memory (RRAM) [1], phase-change memory (PCM) [2], and ferroelectric random access memory (FeRAM) [3], have broad application prospects owing to their non-volatility and near-zero static energy consumption. Compared to other NVMs, ferroelectric capacitors (FeCAPs) offer advantages in energy consumption and endurance. However, the destructive read operation of capacitors (e.g., DRAMs and FeCAPs) destroys the stored data. Thus, an additional write-back operation to refresh the cell is required because after multiple rows of cells are activated and read concurrently for compute-in-memory (CIM) operations, they cannot perform their respective write-back actions. Because most CIM operations must keep data for reusing (e.g., weights in artificial neural networks), the destructive read operation restricts FeCAPs' application in CIM systems.

One way to realize CIM operations in FeCAPs is to use the same copy-operation scheme as in DRAMs [4]. To retain the stored data of CIM-operation cells, this scheme copies the cells to specific rows and activates them for charge sharing to realize a calculation. However, the copying operation increases energy consumption and CIM-operation time. Moreover, such specific rows decrease the effective storage capacity by occupying the storage cells. The existing schemes such as 2TnC [5] and 1T2C [6] can improve integration of FeCAPs or operating speed, but still inevitably use the copy-operation scheme.

In this study, we used the ferroelectric domain characteristics of FeCAPs to propose a half-destructive read scheme (HDRS) for CIM operations, which uses the FeCAPs' charge in two steps. Figure 1(a) depicts the state transitions and the corresponding operation scheme of $cell_0$ and $cell_1$ involved in a CIM operation. (1) Write: write '0' and '1' into $cell_0$ and $cell_1$, respectively. (2) CIM: a low voltage pulse is applied to the plate lines (PLs), and part of each cell's charge is used for the CIM operation. (3) Restore: a large voltage is applied to the PLs, and the residual charge of the cells is used to be sensed and restore the data. The proposed scheme neither includes the copy operation used in other schemes nor requires additional rows for CIM operations. Thus, it offers superior computational latency, energy consumption, storage cell utilization, and array endurance. To validate our scheme, we first tested the essential characteristics of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) FeCAP. Then, the proposed HDRS was applied to the FeCAPs to extract parameters and verify the feasibility of HDRS. Finally, the extracted parameters are used to perform simulations on a 128 × 128 1T1C FeCAP array.

The structure of the used HZO FeCAP comprising a TiN/HZO/TiN stack is shown in Figure 1(b). A 10-nm thick HZO thin film was deposited by using an atomic layer deposition technique (ALD) at 550°C. More details on the HZO FeCAP's characteristics are presented in Appendix A.

The HDRS was tested on the HZO FeCAP to verify its feasibility. Figures 1(c) and (d) show the polarization (P)-voltage (V) curves of the FeCAP cells storing '0/1' in the three phases of the HDRS. As evident from the figure, the remnant polarization (P_r) of the device storing '1' significantly changes in the CIM's phase, implying that the bitline (BL) voltage rises after charge sharing occurs between the cells and the BL in the FeCAP array. For the cell storing '0', P_r changes slightly, implying that the BL voltage will be minutely affected when the charge sharing occurs. Thus, the

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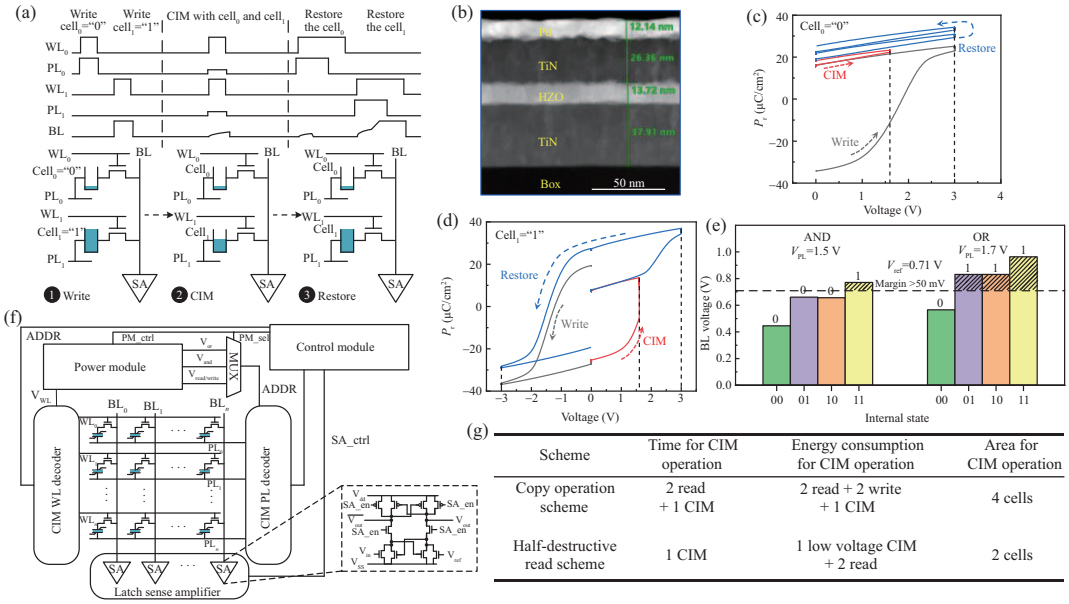

(g)

Scheme	Time for CIM operation	Energy consumption for CIM operation	Area for CIM operation
Copy operation scheme	2 read + 1 CIM	2 read + 2 write + 1 CIM	4 cells
Half-destructive read scheme	1 CIM	1 low voltage CIM + 2 read	2 cells

Figure 1 (Color online) (a) State transitions and the corresponding operation scheme of the FeCAP cells involved in CIM operations; (b) transmission electron microscope image of the HZO FeCAP structure; (c) *P*-*V* curves of the FeCAP storing '0' in three phases; (d) *P*-*V* curves of the FeCAP storing '1' in three phases; (e) simulated BL voltage during the CIM operation; (f) schematic of the simulation circuit for the HDRS; (g) comparison of the HDRS and copy-operation scheme for CIM operation in terms of time, energy consumption, and area.

difference between P_r changes in the restoring phase of the two conditions (FeCAP storing '0' or '1') ensures that the stored data ('0' or '1') can be read out and restored. The detailed test scheme and the FeCAP's variation analysis are given in Appendix B.

Simulation and discussion. We performed the SPICE simulation to verify our scheme. The simulation uses the FeCAP model proposed in [7] with the 130-nm logic process library. The CIM circuit is shown in Figure 1(f). The peripheral circuit can realize read and write as well as CIM operations. Notably, with output signals of a sense amplifier (SA) and different voltage pulses of PLs, the circuit can implement different CIM operations, including "AND" and "OR" logic ($V_{\rm out}$) and "NOT", "NAND", and "NOR" logic ($\overline{V_{\rm out}}$).

In addition, Figure 1(e) shows the BL voltage when the two cells perform "AND" and "OR" operations with different internal states. The low voltage pulses applied to the PLs can be adjusted for performing different CIM operations with the sense marginally exceeding 50 mV. Additional information on simulation is presented in Appendix C.

As shown in Figure 1(g), we compared the performance of the copy-operation scheme and the proposed HDRS in terms of the operation time, energy consumption, and CIM-operation area. The detailed instructions are presented in Appendix D.

Conclusion. We proposed an HDRS based on the HZO FeCAP for CIM operations. Based on the experimental data of the FeCAPs, the simulation and analysis demonstrated the advantages of the HDRS compared to the copy-operation scheme in terms of computational latency, energy consumption, effective storage capacity, and memory array endurance.

Acknowledgements This work was supported in part by National Key R&D Program of China (Grant No. 2019YFB2204800), Major Scientific Research Project of Zhejiang Lab (Grant No. 2019KC0AD02), National Natural Science Foundation of China (Grant Nos. 61904200, 92164204, 62025406), and Strategic Priority Research Program of the Chinese Academy of Sciences (Grant No. XDB44000000).

Supporting information Appendixes A–D. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Chen W-H, Li K-X, Lin W-Y, et al. A 65nm 1Mb nonvolatile computing-in-memory ReRAM macro with sub-16ns multiply-and-accumulate for binary DNN AI edge processors. In: Proceedings of IEEE International Solid-State Circuits Conference-(ISSCC), 2018
2 Wu J Y, Chen Y S, Khwa W S, et al. A 40nm low-power logic compatible phase change memory technology. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2018
3 Slesazeck S, Havel V, Breyer E, et al. Uniting the trinity of ferroelectric HfO_2 memory devices in a single memory cell. In: Proceedings of IEEE 11th International Memory Workshop (IMW), 2019
4 Hassan H, Patel M, Kim J S, et al. CROW: a low-cost substrate for improving DRAM performance, energy efficiency, and reliability. In: Proceedings of ACM/IEEE 46th Annual International Symposium on Computer Architecture (ISCA), 2019
5 Slesazeck S, Ravsher T, Havel V, et al. A 2TnC ferroelectric memory gain cell suitable for compute-in-memory and neuromorphic application. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2019
6 Wang Q, Zhang D L, Zhao Y L, et al. A 1T2C FeCAP-based in-situ bitwise X(N)OR logic operation with two-step write-back circuit for accelerating compute-in-memory. Micromachines, 2021, 12: 385
7 Aziz A, Ghosh S, Datta S, et al. Physics-based circuit-compatible SPICE model for ferroelectric transistors. IEEE Electron Device Lett, 2016, 37: 805–808