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$Hf_{0.5}Zr_{0.5}O_2$ 1T–1C FeRAM arrays with excellent endurance performance for embedded memory

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Since the initial report of HfO_2-based ferroelectric films in 2011, great attention has been paid to ferroelectric field-effect transistors and ferroelectric random-access memories (FeRAMs) [1–3]. Up to now, many efforts have been devoted to realizing the industrialization of HfO_2-based FE films. However, the limited fatigue performance has always been the main problem to be resolved.

Recently, HfO_2-based one transistor–one capacitor (1T–1C) FeRAM as embedded non-volatile memory has attracted great interest due to its process easiness and compatibility [3]. The conventional dynamic RAM (DRAM), where charges are stored at the floating node, always requires an ultra-low leakage performance at advanced technology nodes. Meanwhile, the ferroelectric capacitor maintains the charge through remanent polarization (P_r), alleviating stringent requirements for low leakage current.

However, many factors are considered in the design and fabrication of the HfO_2-based 1T–1C FeRAM that will affect the performance of the array, including the effect of the $Hf_{0.5}Zr_{0.5}O_2$ (HZO) crystallization temperature on the peripheral circuit, etch damage, effect of scaling on the bit-line (BL) sense margin, read/write circuit design, and reference voltage generation. Up to now, researchers have performed many studies on the HfO_2-based 1T–1C FeRAM. Okuno et al. [4] reported the first 1T–1C FeRAM arrays with the back end of the line (BEOL)-integrated HfO_2-based ferroelectric capacitors, which exhibited a low operation voltage of 2.5 V and a fast operation speed of 14 ns. In addition, the 16 kbit doped-HfO_2-based 1T–1C FeRAM arrays were realized with a 10^7 endurance cycles [5]. Although the HfO_2-based FeRAM has proven its feasibility, some key characteristics cannot meet the requirement for practical applications, and one of the most typical ones is the limited endurance.

In this study, 16 kbit 1T–1C FeRAM arrays with BEOL-integrated HZO-based ferroelectric capacitors were designed and realized. The ferroelectric characteristics of the test key (1C) and single-cell (1T–1C) were discussed. A good endurance of up to 10^9 cycles at the array level was achieved for the first time.

Figure 1(a) shows the integration overview and key process steps of fabricating the 1T–1C array. The TaN/HZO (20 nm)/TaN capacitors stack with diameters of 8, 10, 12, and 16 μm were directly integrated on top of the transistors fabricated with a 130 nm technology node, followed by annealing at 500°C for HZO crystallization. The wafer with metal-ferroelectric-metal capacitors was completed through BEOL metal line processing. Figure 1(b) shows the dedicated test structure schematics of 1C and 1T–1C single-cell integrated by BEOL. Here we used two parallel arrangements of 4×4 and 8×8 to characterize the ferroelectric characteristics. Figure 1(c) shows the measured polarization-voltage (P-V) loops of a single capacitor (1C) with a diameter of 8 μm and 1T–1C through an open transistor biased at a gate voltage of 4 V. 1C and 1T–1C structures achieve twice the remanent polarization ($2P_r$) above 30 μC/cm^2 with an applied V of 3.5 V. The findings demonstrated that the introduction of the 1T selector does not modify the capacitor behavior [6]. The characterization of the ferroelectric properties of the HZO film in the arrays can be found in Appendix A. The good endurance and decent retention performance ensure excellent reliability for the 1T–1C FeRAM. The schematics and simplified timing diagram for the "write" and "read" operations of the 1T–1C structure with a sensitive amplifier (SA) are shown in Appendix B. Figure 1(d) shows the local layout view of the 1T–1C FeRAM test chip with different blocks, demonstrating the word-line (WL) driver, sense amplifier, and cell matrix. Cell matrices with 64×32, 128×32, and 256×32 were used to investigate the effect of the BL length on the memory window. The schematics of the 1T–1C FeRAM chip with different blocks are shown in Appendix C. In addition, the functional "read" and "write" operations for "1" and "0" in

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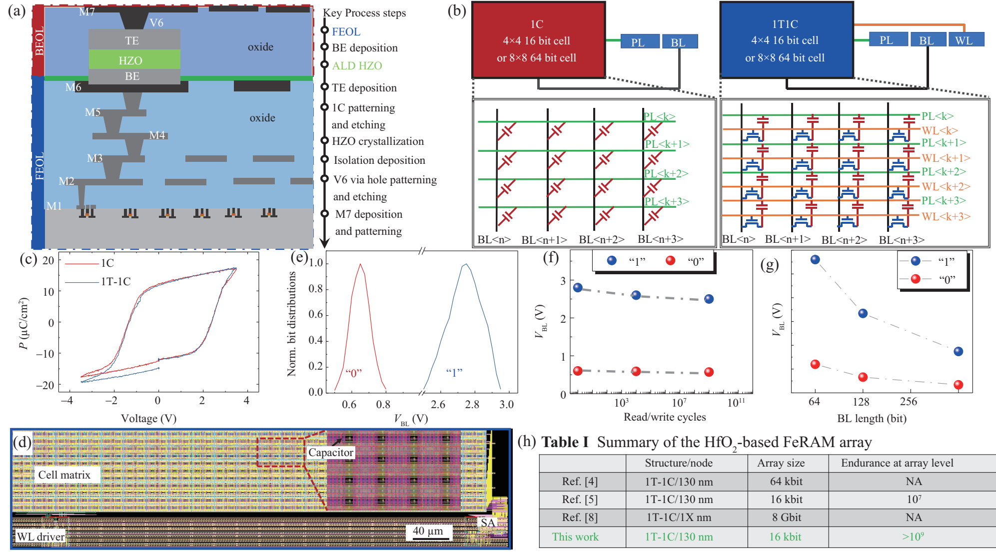

(h) **Table I** Summary of the HfO_2-based FeRAM array

	Structure/node	Array size	Endurance at array level
Ref. [4]	1T-1C/130 nm	64 kbit	NA
Ref. [5]	1T-1C/130 nm	16 kbit	10^7
Ref. [8]	1T-1C/1X nm	8 Gbit	NA
This work	1T-1C/130 nm	16 kbit	$>10^9$

Figure 1 (Color online) (a) Schematics and key process steps of fabricating TaN/HZO/TaN capacitors between M6 and M7 of a 130-nm complementary metal-oxide semiconductor technology node. (b) Test structure schematics of a BEOL-integrated one capacitor (1C) and one transistor–one capacitor (1T–1C) cell arrangement in parallel. (c) *P*-*V* loops of 1C and 1T–1C through open transistors (4 V). (d) Local layout view of the FeRAM test chip with different blocks, including the WL driver, SA, and cell matrix. (e) Distribution of $V_{\rm BL}$ is obtained for "0" and "1" states. (f) Endurance of array-level FeRAM. (g) $V_{\rm BL}$ variation vs. BL length. (h) Summary WL driver of the HfO_2-based FeRAM array.

the FeRAM array are exhibited in Appendix D, which follows the DRAM wafer test program. Figure 1(e) shows the distribution of $V_{\rm BL}$ obtained for "0" and "1" states for the cell matrix. The distribution range of $V_{\rm BL}$ corresponding to "0" and "1" states are (0.5 V, 0.8 V) and (2.5 V, 2.95 V), respectively, which demonstrate a large signal margin for the SA [4, 7].

Figure 1(f) shows that no bit fails through the SA reading after 10^9 write/read cycles at 3.5 V, 1 µs. Excellent endurance performance was achieved compared with the previous HfO_2-based FeRAM [4, 5, 8]. Here, $V_{\rm ref} = 1.8$ V is defined for the array digital reading operation. The slight decrease in $V_{\rm BL}$ in the case of "1" during the write/read cycling is due to the degradation of the polarization of the HZO FE film. $V_{\rm BL}$ in the cases of "0" and "1" were extracted by scanning $V_{\rm ref}$, remaining enough MW up to 10^9 write/read cycles. In addition, $V_{\rm BL}$ dropped faster in reading "1" as compared to reading "0". The effect of the BL length on $V_{\rm BL}$ is shown in Figure 1(g). Clearly, $V_{\rm BL}$ will increase with the decrease in the BL length, which is attributed to $C_{\rm BL}$ values and consistent with formula (B1) in Appendix B.

Conclusion. In this study, the BEOL integration of HZO ferroelectric capacitors in 130 nm node transistors is demonstrated, and 16 kbit 1T–1C array integration is realized. Excellent performance is realized for the single capacitor, including a 30 ns switching speed, $>10^4$ s data retention, and $>10^{11}$ cycling capability. Moreover, $>10^9$ write/read cycling for the 1T–1C cell is achieved for the first time.

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Supporting information Appendixes A–D. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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