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• **Supplementary File** •

$Hf_{0.5}Zr_{0.5}O_2$ 1T-1C FeRAM arrays with excellent endurance performance for embedded memory

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Appendix A Ferroelectric characteristics of the HZO film in the arrays

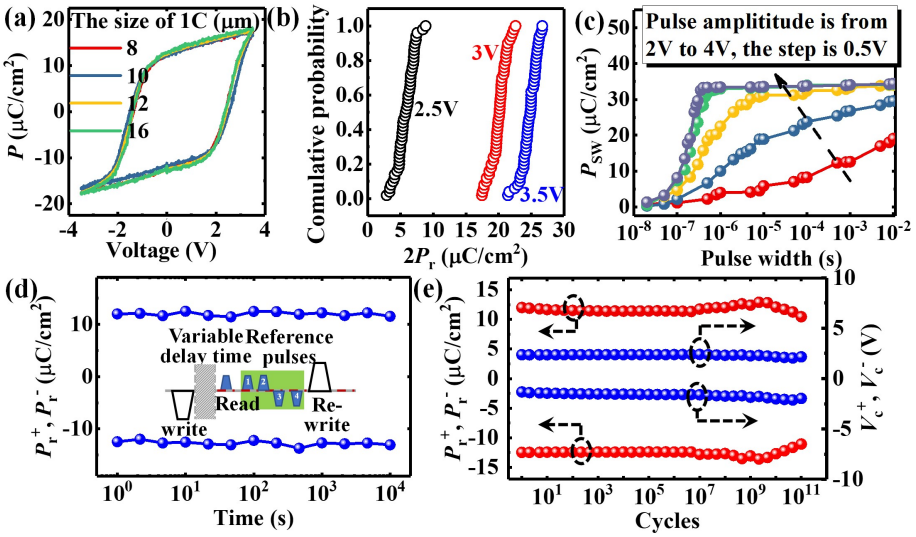

Figure A1 (a) *P*-*V* loops of 1C with different diameters. (b) The cumulative probability of $2P_r$ for 1C with a diameter of 8 μm. (c) Switching characteristics, (d) retention, and (e) endurance of 1C.

In order to verify the ferroelectric characteristics of the HZO film in the arrays, *P*-*V* curves for different sizes of BEOL integrated single capacitor were measured and shown in Figure A1(a), and the results indicate that all the size of a single capacitor (the diameters of 8 μm, 10 μm, 12 μm, and 16 μm) can exhibit excellent ferroelectric behavior. The cumulative probability of $2P_r$ at different sweeping ranges for the single capacitor with a diameter of 8 μm was shown in Figure A1(b). Fifty capacitors were measured for each condition. A similar variation of $2P_r$ at different applied V is observed. In addition, Figure A1(c) shows the P switching characteristics of a single capacitor with a diameter of 8 μm [1]. A fast operation speed of 30 ns and a switching polarization (P_{SW}) above 33 μC/cm^2 with 20 nm HZO film are achieved. Figure A1(d) shows the retention characteristics of the single capacitor. The pulse sequence for the retention test is shown in the inset. The negligible small variation of the P_r is observed during the data retention test up to 10^4 s. The endurance of the single capacitor is characterized by the stable *P*-*V* curves over 10^{11} cycles at 1 MHz. The evolution of the P_r and the coercive voltage (V_c) values are presented in Figure A1(e). The good endurance and the decent retention performance ensure excellent reliability for the 1T-1C FeRAM.

Appendix B 16 kbit 1T-1C array demonstration

The schematics and simplified timing diagram for "write" and "read" operations of 1T-1C structure with sensitive amplifier (SA) are shown in Figure B1(a) and (b), respectively. Here, the word line (WL), bit line (BL), plate line (PL), column select line (CSL), the local data line (LDQ), and pre-charge (PRE) are defined. During the "write" operation, WL is turned on, firstly. And

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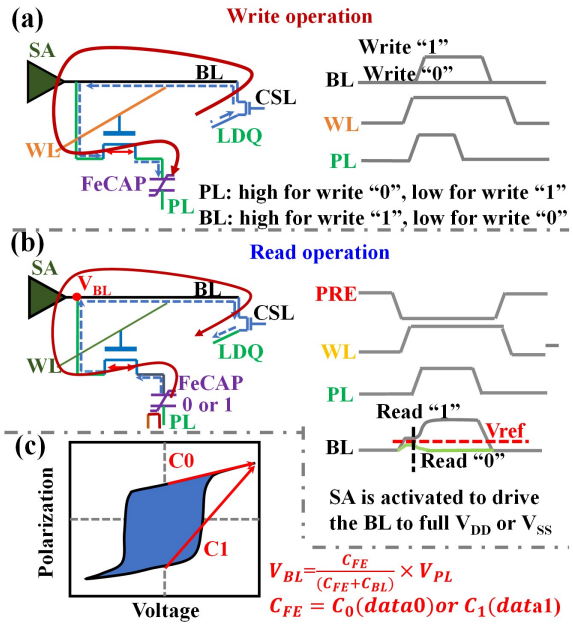


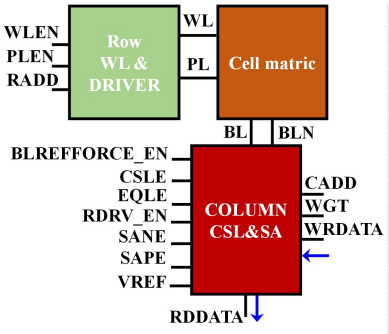
Figure B1 Schematics and simplified timing diagram for (a) write and (b) read operations of 1T-1C structure with sensitive amplifier (SA). Word line (WL), bit line (BL), plate line (PL), column select line (CSL), local data line (LDQ), and pre-charge (PRE) are defined. (c) Definition of C_{FE} in formula (B1).

then, the PL increases to V_{high} and subsequently is pulled back to V_{low}. BL is raised to V_{high} to write "1" during the PL is at V_{low}, and BL is driven to V_{low} to write "0" during the PL is at V_{high}. Finally, deactivating the WL leaves this state undisturbed until the next access. Similarly, during the "read" operation, data is read from the selected cell to SA *via* PL pulsing and then transferred to LDQ. The potential of BL (V_{BL}) is compared to a reference voltage (V_{ref}) with one SA per BL and converted into a digital SA outputs signal. The V_{BL} is determined by

$$V_{BL} = \frac{C_{FE}}{C_{FE} + C_{BL}} \times V_{PL} \tag{B1}$$

Where V_{PL} is the voltage of PL, C_{BL} is the BL capacitor, and C_{FE} is the ferroelectric capacitor. As shown in Figure B1(c), the C_{FE} is C_0 if a data "0" is stored, and is C_1 if a data "1" is stored, depending on the memory state of the cell. V_{BL} elevates at either $V_{\mathrm{BL}}{}^{\mathrm{C0}}$ ($C_{\mathrm{FE}} = C_0$) or $V_{\mathrm{BL}}{}^{\mathrm{C1}}$ ($C_{\mathrm{FE}} = C_1$). Here, the memory window (MW) of the 1T-1C cell is defined as the difference $\Delta V_{\mathrm{BL}} = V_{\mathrm{BL}}{}^{\mathrm{C1}} - V_{\mathrm{BL}}{}^{\mathrm{C0}}$.

Appendix C FeRAM test chip with different blocks



Signals	Description
REF_EN	ref_bl_voltage_force_enable
EQLE	SA equalize enable
PLEN	pl decoding enable
WLEN	wl decoding enable
SANE	SA n-sense enable
SAPE	SA p-sense enable
CSLE	bl decoding enable
WGT	write enable
RDRV_EN	read data drive enable
WRDATA	Write data
RDDATA	Read data
RADD	row address
CADD	column address
VREF	reference voltage

Figure C1 Schematics of the FeRAM test chip with different blocks, including row (row address, WL decoding and WL driver *et al.*,), column (column address, CSL and SA et al.,), cell-matrix. The main signals and their function were listed.

Appendix D The functional "read" and "write" operations for "1" and "0" in the FeRAM array

For the "read" operation, the BLs are driven to V_{SS}, and WL is turned on, firstly. Then, V_{BL} rises to $V_{\mathrm{BL}}{}^{\mathrm{C0}}$ in case of "0" and $V_{\mathrm{BL}}{}^{\mathrm{C1}}$ in case of "1" via PL pulsing. Secondly, by setting V_{BLN} to V_{ref}, during SA operation, BL rises to V_{BLH} (data "1")

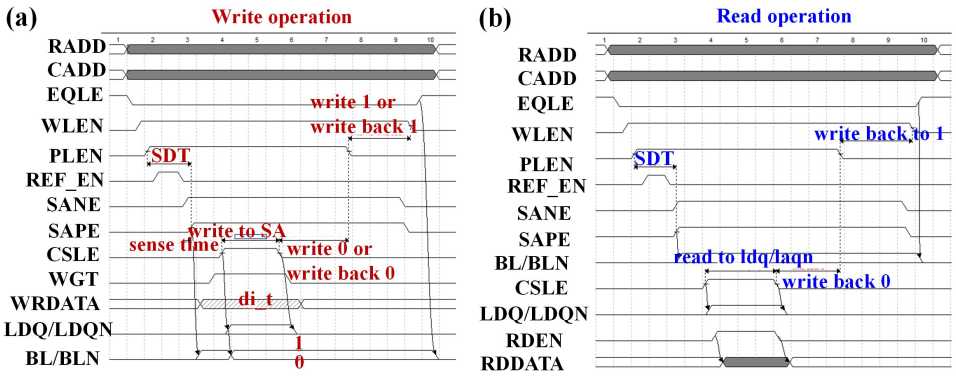


Figure D1 Time diagram of (a) write and (b) read operation of array-level FeRAM.

or falls to V_{SS} (data "0"), achieving data transfer from the cell to the SA (like DRAM active operation). Next, the data in SA is read out to LDQ when the CSLE signal rises to high. Thirdly, the cells are written back. Finally, BLs are pre-charged and WL is turned off. For the "write" operation, the data in SA originated from the cell, is overwritten from the external in/out (I/O) interface during CSLE signal rise to high. The rest of the "write" operation is similar to that of the "read" operation.

References

1 Li Y, Li J, Liang R, et al. Switching dynamics of ferroelectric HfO_2-ZrO_2 with various ZrO_2 contents. Appl. Phys. Lett, 2019, 114: 142902.