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A comprehensive study of device variability of sub-5 nm nanosheet transistors and interplay with quantum confinement variation

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Dear editor,

Gate-all-around (GAA) nanosheet transistor (NST) is one of the most promising candidates to replace FinFET as the next generation because of its best electrostatic integrity and gate control over the channel [1]. However, statistical variability induced by traditional statistical variation sources including random discrete dopants (RDD), line edge roughness (LER), metal gate granularity (MGG), and strong quantum confinement effect has severely limited the performance improvement of NST, which requires a comprehensive study. Although the technology computer-aided design (TCAD)-based studies of global variation and statistical variability and their interplay in advanced semiconductor devices including bulk HKMG MOSFET [2] and FinFET [3] have been reported, there are no corresponding studies considering the interplay between quantum confinement effect and statistical variability.

In this study, a sub-5 nm NST TCAD simulation platform is at first developed and calibrated against the industry technology structure, experimental data of electrical characteristics, and 2D Poisson-Schrodinger (PS) quantum simulations. Based on the well-calibrated nominal device, the key figures of merit including SS, DIBL across the whole design of experiment (DoE) space are presented and analyzed. At last, we study and analyze the statistical variability introduced by RDD generated in source/drain and extension regions, nanosheet edge roughness (SER), and MGG combined with quantum confinement effect.

Device design. The structure of the simulated NST, which consisted of three horizontally stacked nanosheets, is schematically illustrated in Figure 1(a). The key design parameters of three stacked sub-5 nm technology NSTs are based on experimental data [1, 4] (see Appendix A for the detailed structure description). In this study, all simulations are carried out with 3D Sentaurus TCAD tools, 'atomistic' simulator GARAND, and 2D PS simulator.

Device calibration. Firstly, the 3D horizontally stacked n-channel NST is established in the 3D Sentaurus TCAD simulation platform. To improve the computational efficiency and accurately capture the quantum confinement effect, drift diffusion (DD) model coupled with the density gradient (DG) quantum correction strictly calibrated against 2D PS simulation is employed in TCAD simulation [5]. 1D charge distributions along the vertical direction ('z' direction) in the left corner for different thick nanosheets compared between TCAD and 2D PS simulations at $V_{\rm g}$ = 0.7 V and low drain voltage are presented in Figure 1(b). It states more clearly that the DG quantum correction solution is strictly calibrated by 2D PS simulation in a wide range of NST channel thickness. Finally, the device $I_{\rm ds}$-$V_{\rm gs}$ characteristics by TCAD simulation are compared with the IBM experimental data [1] presented in Figure 1(c), illustrating an excellent agreement.

Process induced global variation. To cover the process parameter variation, the 3σ process-induced long-range variations of $\Delta L_{\rm g} = \pm 2$ nm and $\Delta T_{\rm sh} = \pm 2$ nm are assumed to form a $5 \times 5 = 25$ node Cartesian product space. The 2D maps of SS and DIBL across the whole DoE space by TCAD simulations are presented in Figure 1(d) and (e), respectively. It is clearly found that the key figures of merit are the best for about 4 nm thick NSTs and if the nanosheet thickness reduces further, the device performance parameters will drop sharply and even be unacceptable up to 3 nm because the electrons are firmly confined to the vertical center of nanosheet (as shown in Figure 1(b)).

Statistical variability. Owing to the un-doped channel, RDD is mainly generated in the source, drain, and extension regions. For SER [4], we only consider the top and bottom surface roughness of three stacked nanosheets modeled by using the 2-D autocorrelation function (ACF) [6] parameterized with a correlation length (Λ) of 20 nm and

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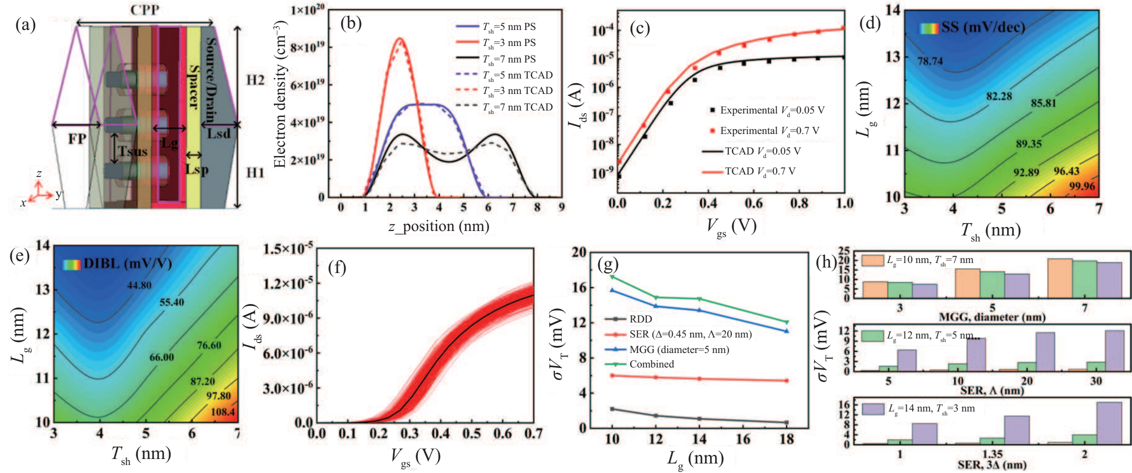

Figure 1 (Color online) (a) Schematic view of the 3D NST in this study; (b) 1D charge distribution along the vertical direction in the left corner for different thick nanosheets compared between TCAD and PS simulation at $V_\mathrm{g} = 0.7$ V and low drain voltage; (c) I_ds-V_gs characteristics of NST compared between TCAD simulations and experimental data [1]; 2D map of SS (d) and DIBL (e) across the whole DoE space by TCAD simulation; (f) full electrical transfer characteristics simulation of NSTs with the 12 nm gate length and 5 nm thick channel including RDD, SER with RMS = 0.45 nm and Λ = 20 nm and MGG with average TiN metal grain diameter of 5 nm at $V_\mathrm{d} = 0.05$ V; (g) gate length dependence of σV_T for 4 m thick NSTs with different statistical variability sources; (h) σV_T dependence of V_T variability respectively on MGG average grain diameter (top graph), SER correlation length (Λ) (middle graph) and SER RMS (Δ) (bottom graph) for the NSTs at three nodes of DoE space.

root mean square (RMS) of 0.45 nm [4]. For simplicity, we assume that there is no correlation between the edge roughness lines along x- and y- directions. TiN gate metal grains with an average diameter of 5 nm are assumed and MGG is modeled with two possible work functions spanning 0.2 eV occupying 40% probability for ⟨111⟩ grain and 60% probability for ⟨200⟩ grain of occurrence [2]. The statistical impedance field method (sIFM) is carried out to investigate the variation of the device characteristics. Figure 1(f) shows the I_ds-V_gs characteristics of the uniform NST and 1000 microscopically different atomistic samples with the combination of three statistical variability sources.

The gate length dependence of σV_T for 4 nm thick NSTs is shown in Figure 1(g). Owing to the low RMS of 0.45 nm for the 4 nm thick nominal NST and the range of gate length varying close to the correlation length of 20 nm, Figure 1(g) shows that the SER-induced σV_T slowly decreases with the gate length gradually increasing. The dependence of σV_T on MGG average grain diameter, SER correlation length (Λ) and SER RMS (Δ) for the NSTs at three corner nodes of DoE space is presented in Figure 1(h), respectively. The SER with larger Λ and RMS all brings obviously more V_T fluctuations, but SER-induced variability is more sensitive to RMS. Meanwhile it seems that σV_T is linearly proportional to the RMS of SER but is saturated for large Λ.

Conclusion. The comprehensive studies aimed at the interplay between the quantum confinement effect and device statistical variability among process design of experiments for sub-5 nm NSTs have been presented and analyzed through strictly calibrated TCAD simulation platform for the first time. The impact of quantum confinement variation on the key performance parameters of NSTs with different channel geometry structures also have been studied. It is found that the NSTs with the optimized nanosheet thickness of approximate 4 nm have the best key figures of merit. After considering the interplay between the quantum confinement and statistical variability, MGG as the dominant statistical variability source brings the largest threshold voltage fluctuation and the MGG-induced variability can be suppressed with the average grain size reduction, but SER can also cause the comparable threshold voltage variation for 3 nm thick NSTs mainly due to the strong quantum confinement variation. Meanwhile the SER-induced variability can also be suppressed by the uniform smooth nanosheet edges.

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Supporting information Appendixes A–D. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Loubet N, Hook T, Montanini P, et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In: Proceedings of Symposium on VLSI Technology, Kyoto, 2017. T230–T231

2 Wang X, Brown A R, Idris N, et al. Statistical threshold-voltage variability in scaled decananometer bulk HKMG MOSFETs: a full-scale 3-D simulation scaling study. IEEE Trans Electron Dev, 2011, 58: 2293–2301

3 Wang X, Cheng B, Brown A R, et al. Interplay between process-induced and statistical variability in 14-nm CMOS technology double-gate SOI FinFETs. IEEE Trans Electron Dev, 2013, 60: 2485–2492

4 Rawat A, Gorad A, Ganguly U. Analytical estimation of LER-like variability in GAA nano-sheet transistors. In: Proceedings of International Symposium on VLSI Technology, Systems and Application, Taipei, 2019. 1–2

5 Ancona M G. Density-gradient theory: a macroscopic approach to quantum confinement and tunneling in semiconductor devices. J Comput Electron, 2011, 10: 65–97

6 Park J, Lee H, Oh S, et al. Design for variation-immunity in sub-10-nm stacked-nanowire FETs to suppress LER-induced random variations. IEEE Trans Electron Devices, 2016, 63: 5048–5054