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An efficient path delay variability model for wide-voltage-range digital circuits

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Dear editor,

As process technology advances, the parasitic effects of integrated circuits become increasingly prominent, posing serious challenges for integrated circuit design [1,2]. Variations in the process corner, voltage, and temperature (PVT) have a more significant impact on path delay in digital circuits in advanced processes, especially at the near-threshold voltage (NTV) [3,4]. The delay variability of the critical path needs to be evaluated to minimize the timing margin while ensuring reliability. Because NTV circuits have more severe variability than the super-threshold voltage (STV) circuits, modeling and analysis of a wide voltage range circuit appear to be more difficult [5,6]. Performing circuit timing analysis over a wide voltage range with traditional EDA tools (VCS, HSIM, or HSPICE, etc.) becomes complicated and time-consuming, which is inconvenient for the rapid analysis of circuit timing and unsuitable for the wide-voltage design of large-scale system-level integrated circuits. Fortunately, a framework was proposed to fully capture the PVT variations in path delay variability based on the classic fan-out-of-4 (FO4) metric [7] as shown in Figure 1(a), which allowed rapid evaluation of additional random variations in cycle time margin, providing designers with significant convenience. This model is referred to as the single-level FO4 model, which is suitable for a wide voltage range from sub-threshold to nominal voltage when the path is not very long. Unfortunately, it loses accuracy when a path has a long logic length, as referenced in Appendix A, because it ignores the impact of input slew and load by assuming adjacent cells are independent of each other. Obviously, the variance of the path is always larger than the sum of the variances of cells.

Therefore, we propose an enhanced path delay variability model across a wide voltage range by describing the relationship between logic paths and the FO4 chains while taking into account the impact of input slew and output load, as illustrated in Figure 1(b). This method is based on the multi-level popular FO4 chain that is expanded to isolate the impact of process technology and PVT conditions by simply normalizing paths' delay variability to FO4's. The delay variability is then described as a functional relationship between gate- and transistor-level factors such as logic depth, type of cells, fan-in, driving ability, transistor sizes, and cell strength. The proposed multi-level FO4 chain enables complex long-path integrated circuit design across a wide voltage range. This method is applicable to different process nodes and different paths, offering a quick estimation of the path delay variability at different supply voltages and complementary metal oxide semiconductor (CMOS) technologies with limited accuracy loss. Examples of 28 nm digital circuits show that our model conforms with Monte Carlo simulations as well as chips' measurements.

This model adopts multi-level FO4 delay chain technology to characterize the trend of the influence coefficient γ, which fixes the problem of the large error in the single-level FO4 model across a wide voltage range. Its key point lies in that we use an average effect of the m-level FO4 chain to characterize the path, which takes into the effect of the input slew and load dependency of the cells in a path. Our path delay variability model is exhibited in (1) and (2).

$$\frac{\sigma_{\text{path}}}{\mu_{\text{path}}} = X_{\text{path}} \times \frac{\sigma_{\text{FO4}(m)}}{\mu_{\text{FO4}(m)}}, \tag{1}$$

$$\begin{aligned}\sigma_{\text{FO4}(m)} &= \sqrt{\left(m \cdot \sigma_{\text{FO4}}^2 + \text{Cov}\right)/m} \\ &= \sqrt{\sigma_{\text{FO4}}^2 + \text{Cov}/m},\end{aligned} \tag{2}$$

$$X_{\text{path}} = \sqrt{\sum_{i=1}^{N} X_{\text{cell},i}^2 \times \left(\mu_{\text{cell},i}/\mu_{\text{path}}\right)^2}. \tag{3}$$

σ_{FO4}^2 is the variance of the FO4 inverter's delay, $\sigma_{\text{FO4}(m)}^2$ is the mean of the variance of m-level FO4 chain's delay,

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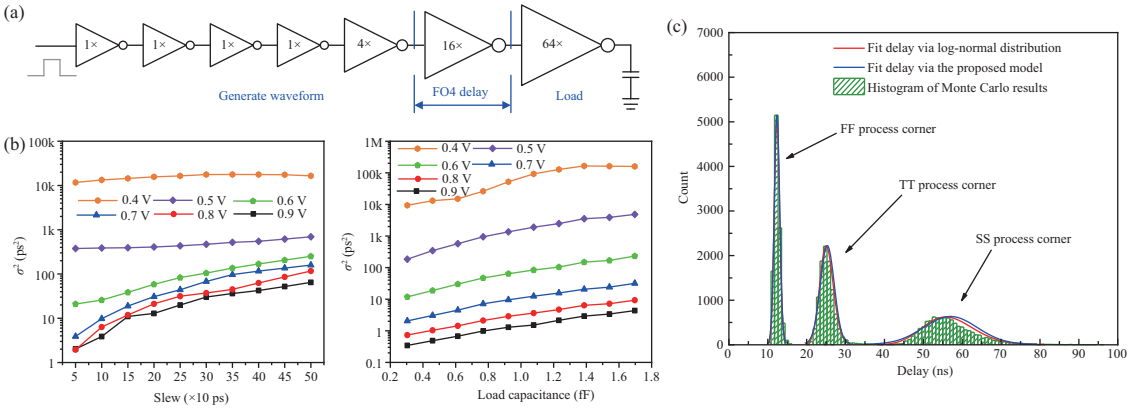

Figure 1 (Color online) (a) Schematic of an FO4 inverter; (b) the impact of input slew and output load on σ^2; (c) simulation and predicted $\sigma_{\rm path}$ and $\mu_{\rm path}$ by the proposed model or log-normal distribution at TSMC 28 nm, SS/TT/FF corner, 0.3 V, 25°C (10k Monte Carlo).

as shown in (2), with Cov being the sum of covariance in the path. The mean of the m-level FO4 chain's delay is $\mu_{{\rm FO4}(m)}$. To establish our path variability model, we adopt the following five steps.

Step 1. Establish an FO4 chain framework to obtain $\sigma_{\rm FO4}$ and $\mu_{\rm FO4}$ at wide-voltage, process corners, and temperatures with Monte Carlo simulations.

Step 2. Establish a typical cell set and obtain $\sigma_{\rm cell}$ and $\mu_{\rm cell}$ of the cells at wide voltages, process corners, and temperatures.

Step 3. Construct $X_{\rm cell}$'s lookup table under typical corners, temperatures, according to the results of Steps 1 and 2 based on Monte Carlo simulations of typical cells to obtain $\sigma_{\rm cell}$, $\mu_{\rm cell}$, $\sigma_{\rm FO4}$ and $\mu_{\rm FO4}$.

Step 4. Construct a lookup table for computing the logic length of the stable point m in a path. The lookup table is based on the Monte Carlo simulations of a constructed path. The m table is one-dimensional, and the variable is cells' types.

Step 5. Calculate $X_{\rm path}$ by (3) for a specific path based on the obtained parameters, and finally calculate the variability parameter of $\sigma_{\rm path}/\mu_{\rm path}$ by (1).

The extensive delay variability with different paths from 0.4 to 1.1 V at TT corner and 25°C in TSMC 28 nm process is shown in Appendix A, where the X-axis represents Monte Carlo simulation results, and the Y-axis indicates the model calculation results. The majority of the data is in or close to the $y = x$ line, indicating that our model calculation results are in good agreement with the Monte Carlo simulation results.

Results. We compare our model with SPICE as shown in Figure 1(c) showing that our model is highly accurate for paths with a logic depth greater than 20. For all paths from 0.4 to 1.1 V, the average error of $\mu_{\rm path}/\sigma_{\rm path}$ between our model and the Monte Carlo results is 7.3%, which is relatively high and acceptable for path delay variability quick estimation.

Conclusion. In this study, to quickly evaluate long-path circuit timing, we propose an efficient path delay model with m-level FO4 delay chain taking the influence of input slew and output load on circuit variation into account. It is verified that the m-level FO4 model achieves high accuracy compared with the classic EDA tools across wide PVT conditions. This model provides a quick estimation of the timing variations of the very large scale integrated circuit across different PVT conditions, which is useful for accelerating the design process of integrated circuits.

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Supporting information Appendix A. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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