SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

February 2023, Vol. 66 122409:1–122409:10
https://doi.org/10.1007/s11432-022-3508-7

Freely switching between ferroelectric and resistive switching in $Hf_{0.5}Zr_{0.5}O_2$ films and its application on high accuracy on-chip deep neural networks

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Received 6 January 2022/Revised 18 February 2022/Accepted 8 June 2022/Published online 11 January 2023

Abstract The $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based ferroelectric field-effect transistor (FeFET) synapse is a promising candidate for at-scale deep neural network (DNN) applications, because of its high symmetry, great accuracy and fast operation speed. However, the degradation of the remanent polarization (P_r) over time caused by the depolarization field has not been effectively resolved, greatly affecting the accuracy of the trained DNN. In this study, we demonstrate a ferroelectric (FE)-resistive switching (RS) switchable synapse using the FE mode for high-speed weight training and the RS mode for stable weight storage to overcome accuracy degradation. The FE-RS hybrid characteristic is accomplished by an HZO-based metal-ferroelectric-metal (MFM) capacitor with asymmetric electrodes, and the best FE endurance, as well as the most reliable RS behavior, is demonstrated by testing several electrodes materials. High memory windows are achieved in both FE and RS modes. Through this design, excellent accuracy is maintained over time, as verified by network simulation.

Keywords $Hf_{0.5}Zr_{0.5}O_2$ films, ferroelectric, resistive switching, accuracy, on-chip DNN

Citation Jiang P F, Xu K R, Yu J, et al. Freely switching between ferroelectric and resistive switching in $Hf_{0.5}Zr_{0.5}O_2$ films and its application on high accuracy on-chip deep neural networks. Sci China Inf Sci, 2023, 66(2): 122409, https://doi.org/10.1007/s11432-022-3508-7

1 Introduction

Deep neural networks (DNNs) have been successfully demonstrated for artificial intelligence (AI) tasks, such as text, image, and speech recognition [1]. With the exponential growth of the number of devices required for ultralarge-scale data processing, transmitting and storing all the data would consume unaffordable power and time budgets. One of the optimization directions is to use traditional logic devices, developing edge-computing accelerators to preprocess data in place and transmitting only the most critical part of the data to the Cloud [2,3]. However, this method can mainly reduce the power consumption in the neural network's computation part. The power consumption of data transmission between the off-chip memory (dynamic random-access memory (DRAM)) and registers is still as high as several watts or even dozens of watts [4,5], even under a 14-nm process node. Thus, developing new computational devices and architectures is particularly important. In-memory computing architectures based on emerging nonvolatile memories (NVMs) can provide on-chip information computing and storage, which is promising for achieving edge systems with power consumption lower than 100 mW. This solution has high requirements in terms of area, latency, power consumption, and device accuracy.

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Analog NVMs meet the requirements for on-chip weight training and storage for DNN acceleration. Typical analog NVMs, such as resistive random-access memory (RRAM) and ferroelectric field-effect transistor (FeFET), have been systematically studied. NVM's optimizable characteristics for improved synaptic performance include symmetry and linear conductance (to obtain more conductance states), operation speed, and accuracy (parameter consistency). Woo et al. [6] proposed an AlO_x/HfO_2 bi-layer RRAM array in the case of filament-type RRAM, but due to the lack of symmetry, there are few available conductance states. While interfacial or multifilament-type RRAM, such as $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO)-based interfacial RRAM devices [7], Ag^+-ion-based conductive-bridge memristor devices [8], and TaO_x-based resistive synaptic arrays with super multistate (200 conductance states) [9], can overcome the symmetry problem, the operation speeds become extremely slow due to the weak programming. To our knowledge, the best synaptic performance of RRAM-based synapses was proposed by Li et al. [10]. The 128 × 64 memristor cross-bar array can demonstrate signal processing, image compression, and convolutional filtering functions, but the parameter consistency issue remains unsolved. The parameter consistency issue, which refers to the consistency in a single device during writing (here, the read disturbance is not considered), mainly adversely affects the training process of DNNs and reduces the accuracy of the algorithm (assuming that the read operation does not affect the stored state). Since the consistency problem of RRAM devices is difficult to fundamentally solve, the only way to deal with it is to train off-line and then infer on-line, and the price is a dramatic increase in power consumption.

When compared with RRAM-based synapses, the FeFET has inherent advantages in symmetry, operation speed, and accuracy owing to the precise and fast partial polarization switching under the programming electric field, which makes it a promising candidate for DNN applications [11, 12]. However, the issue of P_r degradation over time resulting from field depolarization is a fatal flaw [13–16]. In actual network applications, the stored information is quantified as a weight; thus, even slight variations ultimately decrease the accuracy of the entire network during the inference process [17, 18]. Under these circumstances, it is particularly important to address the P_r delegation over time in FeFET-based DNNs. Unfortunately, P_r delegation is an inherent problem of FeFETs because of the field depolarization. In filamentary RRAM, the resistance state remains relatively unchanged over time. If the advantages of RRAM and FeFET can be combined, the overall performance of the on-chip DNN in both the training and inference processes can be greatly improved.

In this study, we demonstrate an $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based metal-ferroelectric-metal (MFM) capacitor with asymmetric electrodes for the design of ferroelectric (FE)-resistive switching (RS) hybrid synapses. The FE mode of the MFM capacitor, which is associated with an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET), is used for on-line weight training, while the RS mode is used for weight storage (Figure 1). After investigating several top electrode (TE) metals with TiN bottom electrodes (BEs), the best FE endurance and most reliable RS behavior were obtained. To realize key operations, such as matrix products and weight updates, such synapses' cell structures can be developed in a pseudo-crossbar array. We stimulate the accuracy degradation of a DNN training a neural network on the MNIST dataset by comparing the measured degradation speed of P_r and resistance states over time in the capacitor. The results show that in the single FE mode, the DNN's recognition accuracy drops to <60% in 10^4 s. In contrast, there is almost no degradation in accuracy over time in the FE-RS hybrid mode. The proposed synapse has great potential for on-line learning.

2 Results and discussion

The FE endurance performance of capacitors with different metal TEs was analyzed at 1 MHz for bipolar cycle switching and 50 kHz for P-V measurement (Figure 2(a)), and the variation in P-V loops over different cycle numbers is shown in Figure 2(b)–(g). The electrode materials, Pt, Pd, Ta, Ru, W and Au, were selected based on the following considerations. First, the RS behavior in HZO films is based on the valence change mechanism (VCM) of the oxygen vacancies [19–21], and the utilization of TiN BEs to induce stable FE characteristics limits the redox reaction to occurring near the BE of the MFM capacitor [22–25]. Thus, TEs must be chemically stable metals, meaning it is difficult for them to undergo redox reactions. Second, the TE should not negatively affect the ferroelectricity; in other words, the TE should have been proven to produce stable ferroelectricity in the literature. Finally, the compatibility of material preparation with the standard complementary metal-oxide-semiconductor (CMOS) process needs to be considered. For an intuitive demonstration, voltage was applied to the BE when exhibiting

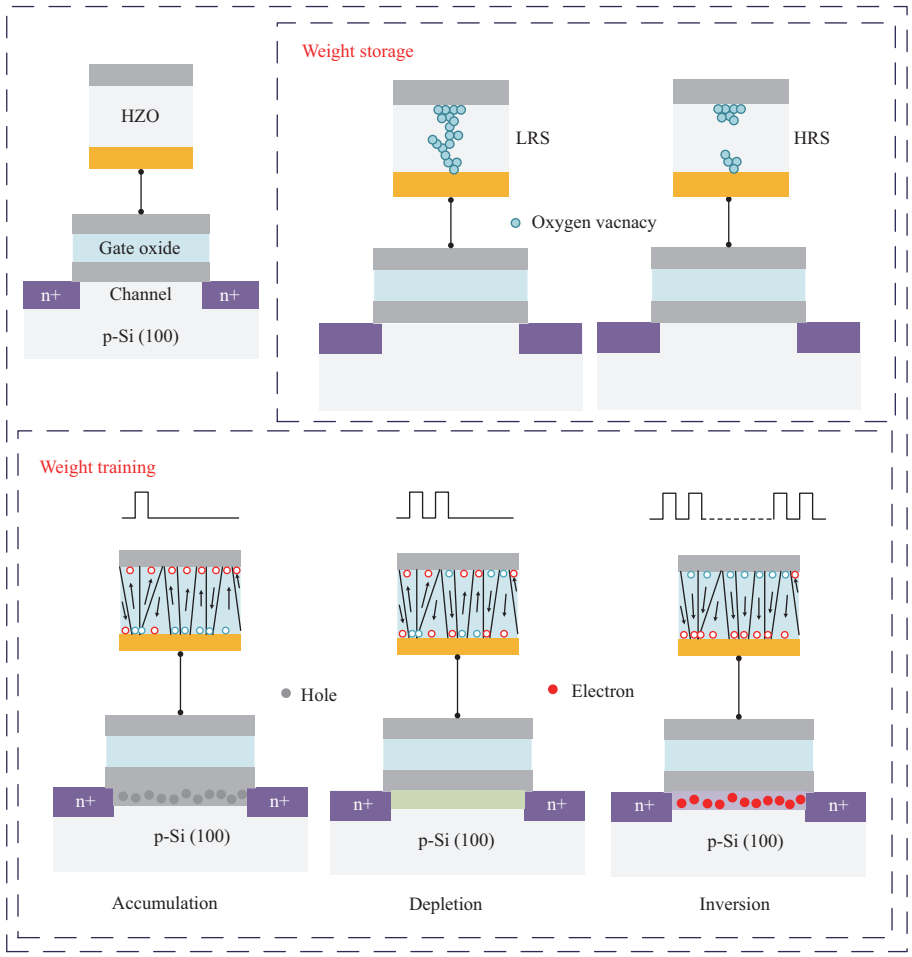

Figure 1 (Color online) Schematic diagram of synapse working principle. An HZO-based ferroelectric capacitor is connected with a transistor in series. During the weight-training process, by verifying the programming pulse applied on the top electrode of the ferroelectric capacitor, the partial polarization switching can carry out a gradual modulation to the channel and lead to the accumulation, depletion or possible inversion (depending on the strength of the polarization control ability) state. Then during the weight storage process, by switching the resistance state between high and low resistance states, the voltage drop on the gate will make corresponding changes.

the electrical performance of a single capacitor. Due to the asymmetric electrode structure applied to obtain RS characteristics, as well as the 8 nm film thickness, the HZO layers easily breakdown, and the endurance limits of all samples are not outstanding compared to other reports. However, the endurance limits of at least 10^8 cycles are basically equal to those of most reported ferroelectric capacitors [26–30] and sufficient to meet the training time requirements.

Of all kinds of TE metals, Ta is the first to be excluded. Although the value of P_r for Ta is quite large, its endurance performance is the worst. The large work function difference between Ta and TiN (near 0.45 eV) leads to an asymmetrical E_c, and this large E_c may be one of the root causes of the poor endurance [22]. In addition, Au is not applicable. Its initial P-V loop is anti-ferroelectric-liked with small P_r, and its remarkable wake-up effect may affect the stability of the weights.

The RS characteristics of other samples need to be investigated. To guarantee the read margin of the FE current, the high resistance state (HRS) current during RS operation must be low and not cover up the FE current. The compliance current is one of the key factors that determine the reset states, and we set it to a large value (1 mA) to achieve an exhaustive reset process [30]. As shown in Figure 3, capacitors with Pt and Pd TE exhibit gradient reset processes with large memory windows; however, the other two electrode metals cannot achieve similar functions. The capacitor with Ru TE exhibits a mutated reset process and thus cannot achieve multi-value RS behavior by adjusting the reset voltage; additionally, the RS memory window of the capacitor with W TE is too small. Based on the above investigations, Pt and Pd are available for our FE-RS hybrid synapse.

The capacitors with Pt TEs demonstrate that the operation modes of FE and RS can be freely switched

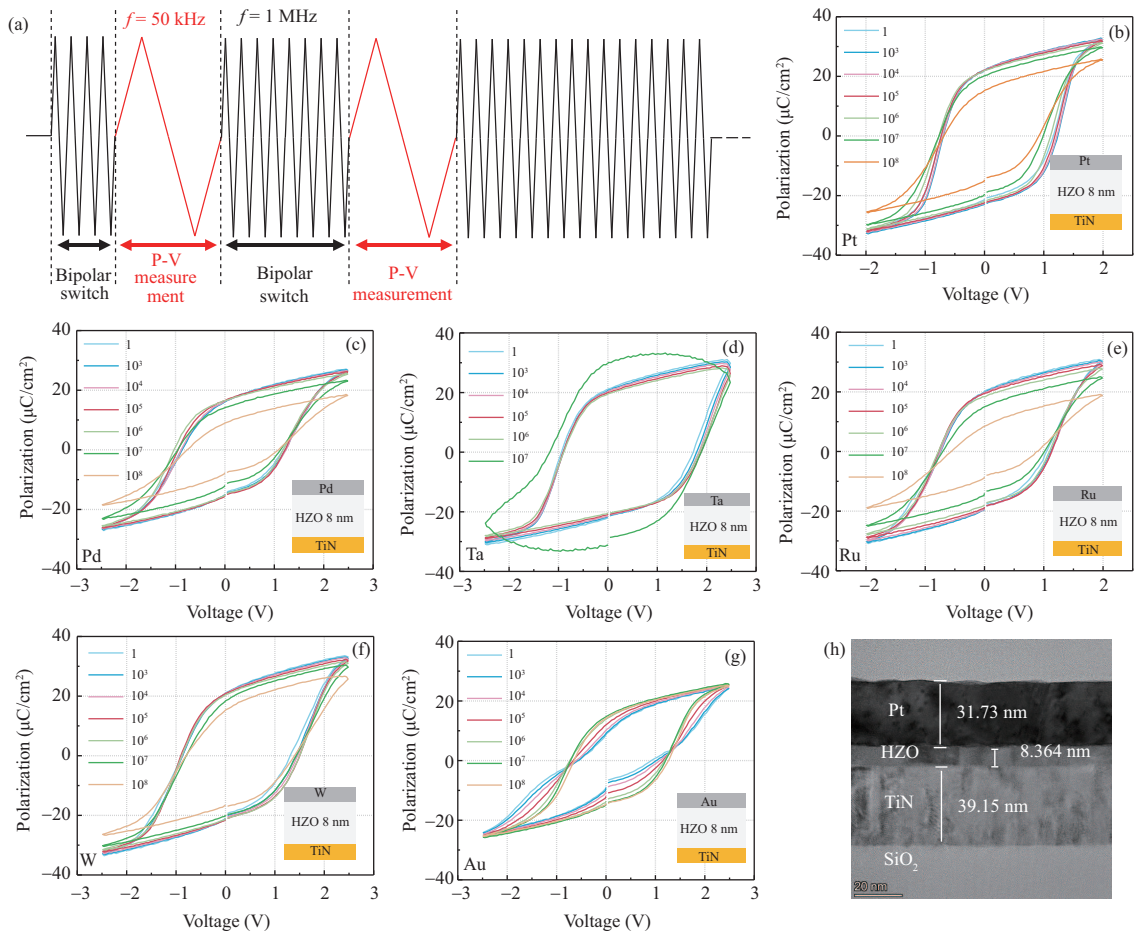

Figure 2 (Color online) Testing method and the FE endurance performance of HZO-based capacitors with TiN BE and different TE metals. (a) The pulse frequency for bipolar switching stress cycling is 1 MHz, and the pulse frequency for P-V measurement is 50 kHz. Capacitors with (b) Pt, (c) Pd, (d) Ta, (e) Ru, (f) W, and (g) Au TEs, respectively. (h) SEM section view image of a TiN/HZO/Pt structured FE capacitor.

(Figure 4(a)). Here, we start from the FE operation, and the initial state shows a large P_r ($2P_r$ approximately 40), with coercive voltages at approximately −0.8 and 1 V, respectively. Then, during the first RS operation, to ensure the formation of a strong conductive filament (CF) and a subsequent thorough reset process, a 3 mA compliance current is applied. A thorough reset makes the capacitor return to the HRS; thus, the leakage current does not cover the FE switching current. The FE and RS measurements are operated one by one following the sequence of the blue arrow. The RS operations shown in the lower figures in Figure 4(a) are cycled for 20 times, which demonstrate great stability and parametric uniformity. Here we only show a part of data of the operation transformation, and the results are enough to justify our findings. All the P-V loops during the operation transformation are assembled and show great uniformity (Figure 4(b)), which demonstrates that the transformation does not interfere with the original characteristics of the two operations. Based on the independent FE and RS operation modes, the core function of our FE-RS hybrid synapse is implemented, and the ability of multi-times transformation enables the network to be retrained for different tasks. Considering the memory window, the endurance performance, the multi-value operation ability, and the CMOS compatibility, Pt should be the best choice for the TE metal. To investigate the crystalline properties and chemical composition of the ferroelectric layers, a TiN/HZO/Pt structured capacitor was subject to high-resolution transmission electron microscopy (HRTEM) imaging and energy dispersive X-ray spectroscopy (EDX) mapping (data are not shown here). The HRTEM images prove that the HZO layer is polycrystalline with multiple mixed phases. The component elements (including Pt, O, Hf, Zr, Ti, and N) were investigated by EDX mapping. In the HZO layer, the component ratio of Hf and Zr approaches 1:1, and the fraction of Zr is marginally greater. To determine the crystal phases of the HZO layers, a special aberration corrected transmission electron microscope (AC-TEM) was used for higher resolution (Figure 5(a)), and the fast

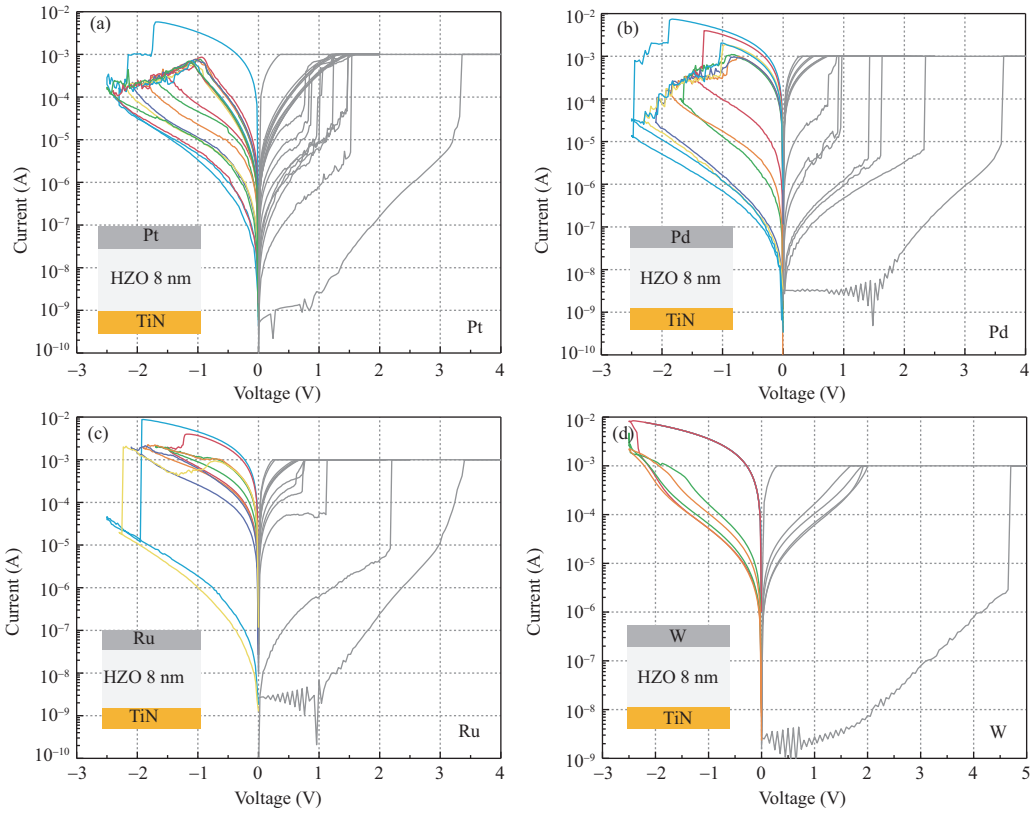

Figure 3 (Color online) RS cycling performance of HZO-based capacitors with TiN BE and different TE metals. Capacitors with (a) Pt, (b) Pd, (c) Ru, and (d) W TEs, respectively.

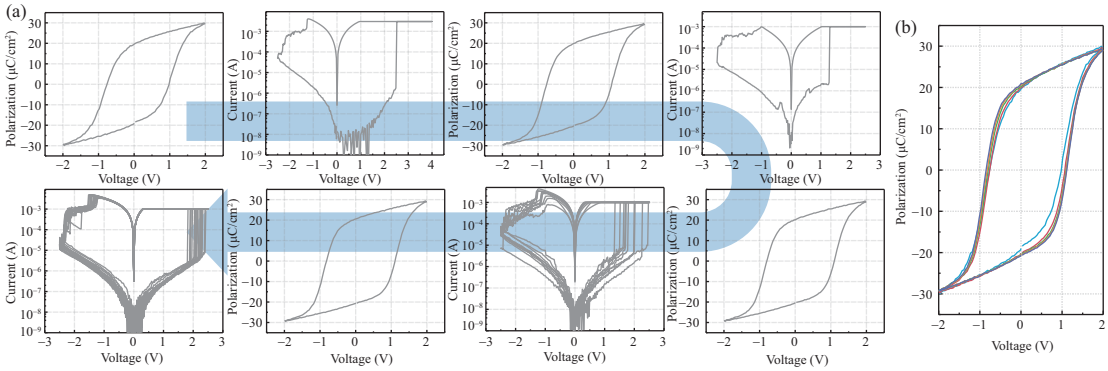

Figure 4 (Color online) Free transformation between ferroelectric and resistive-switch operation. (a) Transformation from ferroelectric to resistive-switching in turn. (b) All the P-V loops during the operation transformation are assembled and show great uniformity, which demonstrates that the transformation does not interfere with the original characteristics of the two operations.

Fourier transform (FFT) patterns from the square areas of the TEM image were analyzed. The square area is in accordance with the diffraction pattern of the orthorhombic phase (o-phase, space group $Pca2_1$) with a zone axis [0 0 1], as displayed in Figure 5(b).

The TiN/HZO/Pt structured capacitor was used for all the following experiments. The P-V loops under different polarization voltages show a precise and analogic P_r response (Figure 6(a)). After forming, the RS memory window is greater than 3 orders of magnitude. The RS behavior between the high and low resistance states can be achieved by adjusting the reset voltage (Figure 6(b)). With the multi-value characteristics, this capacitor has the potential for analog synapse applications based on FE or RS properties. To implement the function shown in Figure 1(a), which uses the FE mode for weight training and the RS mode for weight storage, an n-channel MOSFET is connected to the MFM structured capacitor in series (the width of the channel is 300 nm). The transfer and output characteristics of such a

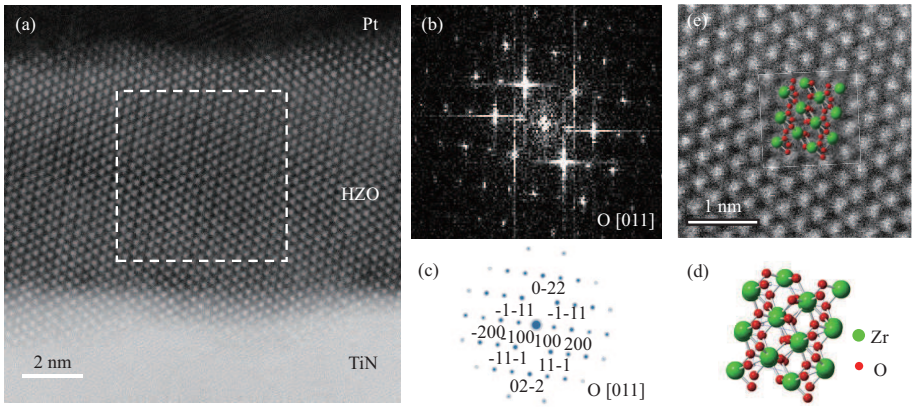

Figure 5 (Color online) Atomic structure of HZO o-phase in the TiN/HZO/Pt structured capacitor. (a) AC-TEM image; (b) and (c) FFT diffraction pattern with [0 0 1] zone axis; (d) schematic of the unit cell of HZO; (e) the arrangement of atoms in the lattice matches the o-phase structure.

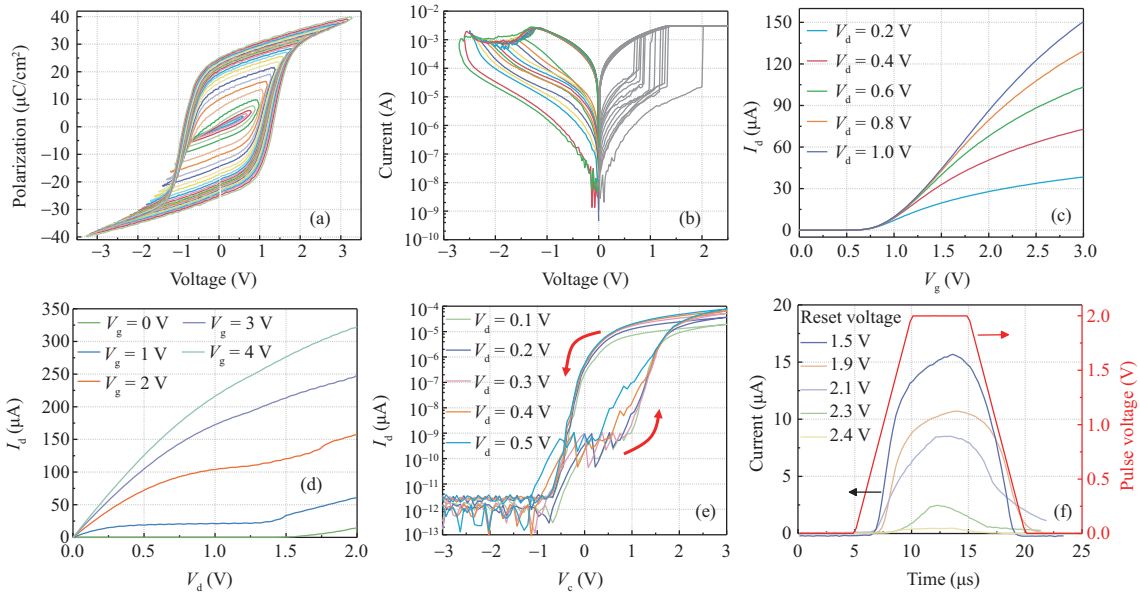

Figure 6 (Color online) Electrical performance of the TiN/HZO/Pt structured capacitor and corresponding FE-RS hybrid synapse. (a) P-V loops under different polarization voltages; (b) the multivalue resistive-switching behaviors; (c) transfer characteristics of a fresh MOSFET under different drain voltages; (d) output characteristics of a fresh MOSFET under different gate voltages; (e) transfer characteristics of a 1T-1C series-connected device under different drain voltages; (f) different reset voltages to achieve multivalue resistances and modulate the voltage drop on the gate with the modulation of drain current I_d.

fresh transistor (T_0) are shown in Figures 6(c) and (d), respectively. When the gate is connected to an FE capacitor, the voltage applied on the capacitor (V_c) can modulate the threshold voltage (V_{th}) owing to the effect of polarization (Figure 6(e)). Since the HRS of capacitor is much smaller than the gate resistance, to amplify the regulation effect of the capacitor on the gate voltage during the RS process [31,32], another transistor T_1 is used to connect the bottom electrode of the capacitor with the source, and the channel resistance of T_1 is set to match the resistance of the capacitor. Here, we replace T_1 with a 10 MΩ resistor, and the operation voltage is applied to the TE of the capacitor. It should be emphasized that the reset voltage polarity must be consistent with the polarization direction in assisting transistor turning on. Since the minimum reset voltage is 1.5 V, which is larger than E_c, it can be supposed that during the reset process with different operation voltages, the polarization directions of the capacitor are all saturated and assist with the T_0 turning on. The result of the modulation of the drain current by RS operation is shown in Figure 6(f).

The transistors used in this study were fabricated based on the 180 nm process node, so the area of the gate was much smaller than that of the MFM structured capacitor (50 μm × 50 μm). Based on poor

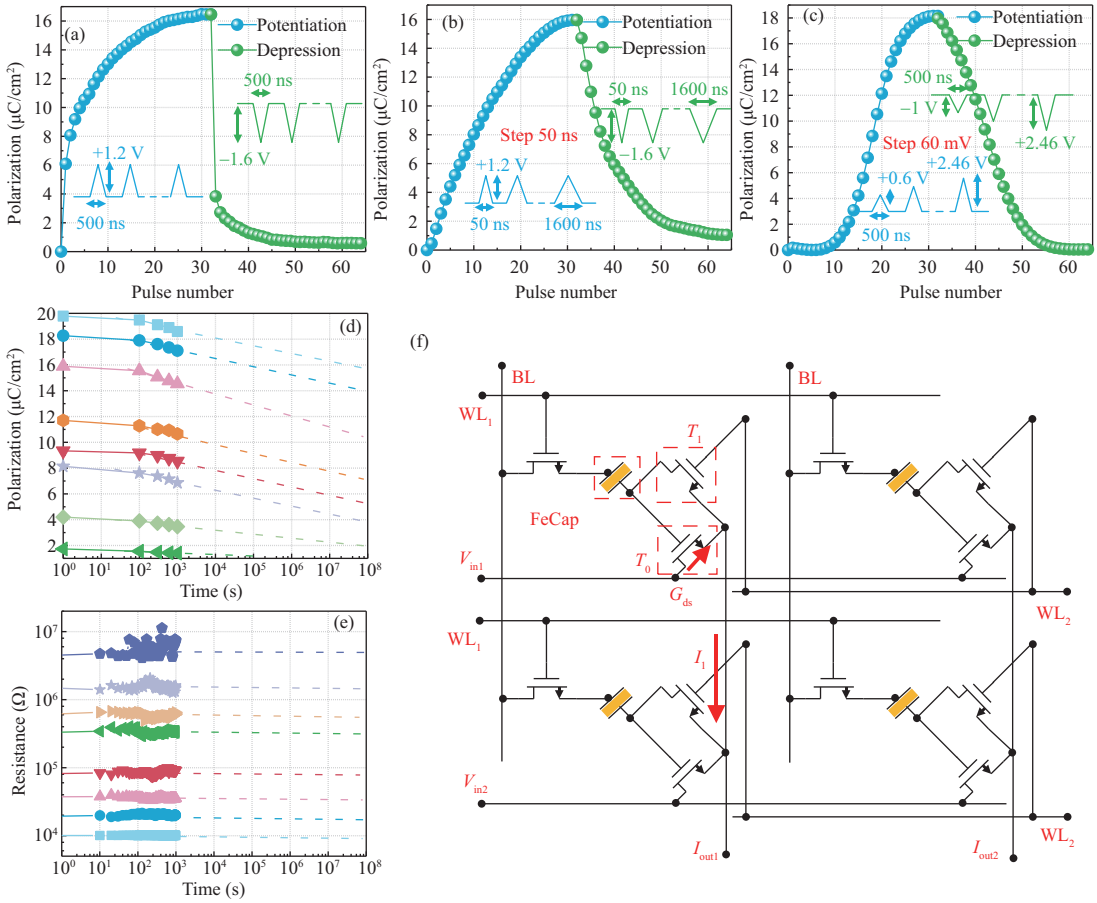

Figure 7 (Color online) Remanent polarization response according to the programming pulse number. (a) Scheme 1: fixed pulse height and width. (b) Scheme 2: fixed pulse height and modulated pulse width. (c) Scheme 3: modulated pulse height and fixed pulse width. Retention characteristics of the TiN/HZO/Pt capacitor: (d) FE and (e) RS operation. The circuit unit structure of FE-RS hybrid synapses: (f) structure of the pseudo-crossbar array.

area matching, the retention of polarization in the capacitor can be extremely poor when it is connected to the gate [33]. This means that the normal FeFET conductance behavior in response to multiple pulse schemes cannot be measured (unless the area matching is optimized). Owing to the excellent scalability of HfO_2-based ferroelectric, we believe that area match problem can be easily solved. Therefore, since we have proven that the connected FE capacitor can indeed modulate the $V_{\rm th}$ of T_0, the polarization characteristics in a single FE capacitor are used to represent the FeFET conductance responses in this study. This substitution is a way of compromise to investigate the polarization degradation and its effect to the recognition accuracy of DNN, but the difference between the polarization tuning and the conductance tuning cannot be ignored.

By verifying the programming pulse schemes, we can obtain synaptic potentiation and depression behaviors. There were three kinds of programming schemes, and all of them had 32 triangle pulses in the potentiation and depression processes. In scheme 1, the pulse height and pulse width were fixed at +1.21 V/−1.6 V and 500 ns. In scheme 2, the pulse height was fixed to the same value as that in scheme 1, but the pulse width was modulated starting from 50 ns increase in steps of 50 ns. In scheme 3, the pulse width was fixed as in scheme 1, but the pulse height was modulated from +0.6 V/−1 V increasing/decreasing in steps of 60 mV. All the values of pulse heights, pulse widths, and progressive steps were the best values selected from many experiments that achieved the best results. As shown in Figure 7(c), scheme 3 with a fixed pulse width and modulated pulse height displays the best linearity and symmetry, which means that it is the most suitable programming scheme for synaptic behaviors.

Since the degradation of P_r over time is one of the most important factors inducing a recognition accuracy decrease in FeFET-based DNNs, the degradation speed of the device in both FE and RS modes was investigated, and the TiN/HZO/Pt structured capacitor was still used to represent the entire synapse. The retention characteristics (at room temperature) of both the FE and RS modes were measured for

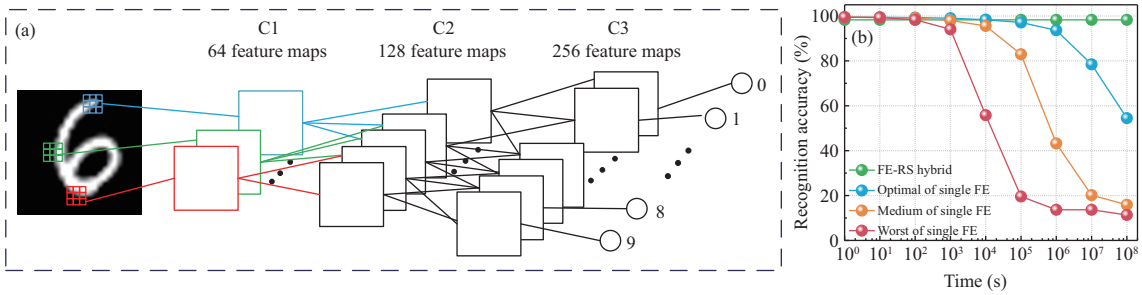

Figure 8 (Color online) Simulation results. (a) The MNIST dataset trained on a neural network consists of three convolutional layers and a fully-connected classifier for simulation. (b) The accuracy declines over time due to the effect of the retention properties.

10^3 s, and extended to 10^8 s (Figures 7(d) and (e)), in which the polarization shows an obvious decline over time, while the resistance shows excellent stability. Figure 7(d) shows that the decay rates of polarization over time are different when starting from different initial values (the middle values have faster decay rates), and all the decay rates are extracted for the subsequent network simulation.

The cell structure of such FE-RS hybrid synapses can be developed in a pseudo-crossbar array, as shown in Figure 7(f), to realize key operations such as matrix products and weight updates. The input vector $V_{\rm in}$ is calculated through the weight matrix $G_{\rm ds}$ and outputs $I_{\rm out}$. $\rm WL_1$ is used to select specific units to program, and the programming pulse is input through BL. The FeCap and series connected T_0 are the core components to perform the FE and RS operations. To amplify the regulation effect of the ferroelectric capacitor on the gate voltage, another MOSFET T_1 is used to connect the bottom electrode and the source. T_1 is controlled by $\rm WL_2$; during the weight training process, it is turned off; then, during the inference process, it is turned on, and the channel resistance should be adjusted to match the resistance of the ferroelectric capacitor. Thus, such a 3T1C cell structure is the minimum size to implement the FE-RS hybrid synapse. With the back-end-of-line (BEOL)-compatible FE capacitor, the only extra area consumption compared to the minimum 2T FeFET-based DNN cells is for the transistor T_1.

To investigate the effect of P_r degradation over time on the accuracy of DNN over time, a neural network consisting of three convolutional layers and a fully connected classifier was trained on MNIST dataset for simulation. The feature maps of each layer were 64, 128 and 256. For better performance, batch normalization and rectified linear units were applied (Figure 8(a)). We trained both a full-precision model (for a single FE mode) and a 3-bit quantized model (for the FE-RS hybrid mode). In the single FE mode, the polarization characteristics were used to represent the FeFET conductance response; thus, the weights were analogous to $[-1, 1]$ mapped to the polarization of $[2, 20]$. Based on the different decline rates of different initial polarization values, we assumed that all devices in the network belong to the fastest, slowest, and evenly distributed decline rates. In the FE-RS hybrid mode, to reduce the impact of RRAM parameter variation, the analogically trained weights were quantized into 3-bit digital data. In the full-precision model, the initial recognition accuracy reaches 99.46%, but according to the decline rate category of devices in the network, the accuracy decreases significantly over time. In the worst case, after 10^4 s, the accuracy degrades to less than 60%, which means that the network is no longer working. In the quantized model, the initial recognition accuracy is slightly lower at 98.3%, but does not degrade over time (Figure 8(b)).

3 Conclusion

In this study, an FE-RS hybrid synapse was demonstrated that overcame the accuracy degradation in FeFET-based DNNs. The proposed device can be freely switched between the FE and RS modes. Several TE metals were investigated to obtain the best FE endurance and most stable RS behavior. The quantized model for the FE-RS hybrid mode shows an initial accuracy of up to 98.3% and does not degenerate over time. According to existing reports, the optimized synapse adds only one additional transistor in area consumption in a unit cell with almost no increase in power consumption, while the reliability in terms of the recognition accuracy maintenance of the whole network is greatly improved. Therefore, the FE-RS hybrid synapse proposed in this study has great value for in-memory computing applications.

4 Experimental section

The HZO-based MFM capacitor was manufactured on SiO_2/Si substrates with a TiN BE. An 8 nm atomic layer deposited (ALD) HZO (Hf:Zr approximately 1:1) layer was deposited at 280°C using TEMAH ($Hf[NCH_2C_2H_5]_4$), TEMAZ ($Zr[NCH_3CH_5]_4$) and H_2O as the Hf, Zr and O precursors. To obtain stable filamentary RRAM characteristics, an asymmetric electrode structure was applied, and all electrode films were deposited by a sputtering system. The prepared capacitors were annealed at 500°C in a N_2 environment for 30 s to induce ferroelectricity, and the cell size was 50 μm × 50 μm. The NMOS transistors used in this paper are fabricated by 0.18 μm CMOS technology. The electrical characteristics were tested by an Agilent B1500 semiconductor parameter analyzer with a B1530A generator unit module and a radiant precision multiferroic II tester. The simulation of the effect of P_r degradation over time on the accuracy of the DNN was trained in a neural network on MNIST dataset.

Acknowledgements This work was supported in part by National Key Research and Development Program of China (Grant No. 2017YFA0206102), National Natural Science Foundation of China (Grant Nos. 61922083, 61904200, 61974049), and Strategic Priority Research Program of the Chinese Academy of Sciences (Grant No. XDB44000000).

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