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# 1.7 kV normally-off p-GaN gate high-electron-mobility transistors on a semi-insulating SiC substrate

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**Abstract** A study of 1.7 kV normally-off p-GaN gate high-electron-mobility transistors (HEMTs) on SiC substrates is presented. The fabricated p-GaN HEMT with a gate-drain spacing $L_{\mathrm{GD}} = 5$ μm exhibited a threshold voltage of 1.10 V, a maximum drain current of 235 mA/mm, an ON/OFF ratio of $10^8$, and a breakdown voltage of 440 V. Benefiting from the semi-insulating and high-critical-electric-field substrate, the p-GaN HEMT with $L_{\mathrm{GD}} = 23$ μm achieved the remarkably high breakdown voltage of 1740 V with substrate grounded. This breakdown voltage is very high compared with the reported values for p-GaN HEMTs on silicon substrates with substrate grounded. The vertical breakdown voltage for the p-GaN-on-SiC material exceeded 3 kV with substrate grounded. In addition, the maximum drain current at 500 K was 48% of that at 300 K with a negligible threshold voltage shift. These results indicate the substantial potential of p-GaN gate HEMTs on SiC substrates for high-voltage power applications.

**Keywords** p-GaN gate, HEMTs, high voltage, SiC substrate

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## 1 Introduction

GaN-based wide-bandgap semiconductor devices possess high breakdown voltages and low values of specific ON-resistance $R_{\mathrm{ON,sp}}$, and are promising materials for power applications [1–4]. Specifically, p-(Al)GaN gate high-electron-mobility transistors (HEMTs) on silicon substrates have been commercialized widely for power applications below 650 V [5–7], because they possess the advantages of high electron mobility of two-dimensional electron gas (2DEG), high breakdown voltage, an (Al)GaN-based pn junction, and a low-cost silicon substrate. The limited breakdown voltage $V_{\mathrm{BR}}$ has hindered the development of p-GaN HEMT products operating above 1200 V. For GaN-on-Si HEMTs, the substrate needs to be grounded for $V_{\mathrm{BR}}$ measurements, and the value of the substrate-grounded $V_{\mathrm{BR}}$ is limited by the vertical breakdown mechanism [8, 9]. Increasing the GaN buffer thickness is an effective way to increase the vertical breakdown voltage. A 5.5 μm GaN buffer and a 4.6 μm AlGaN-based buffer would experience vertical material breakdown at 1207 and 1380 V, respectively [10, 11]. For p-GaN HEMT on silicon, a substrate-grounded breakdown voltage of 1000 V has been achieved for a 4 μm AlGaN-based buffer and a 500 nm GaN channel layer. The breakdown voltage was increased to 1344 V by using a 5 μm high-resistivity GaN buffer and a 400 nm GaN channel layer [12, 13]. Owing to the large lattice mismatch

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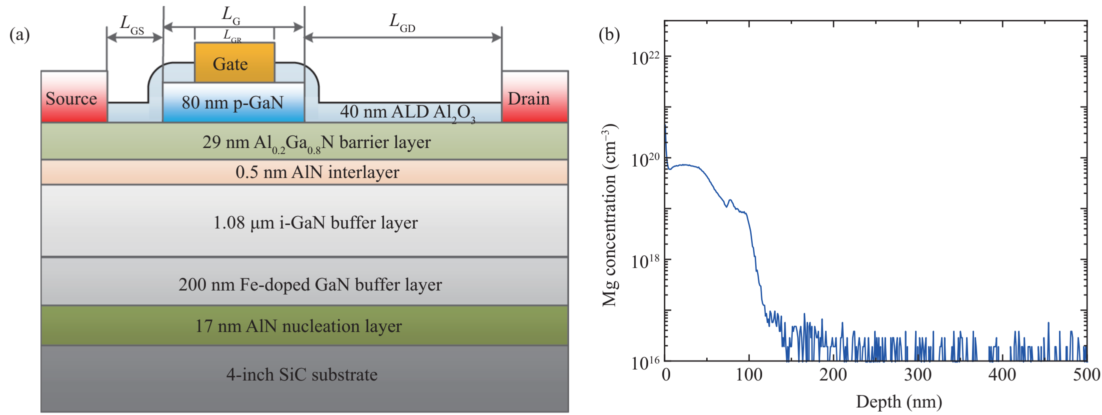


**Figure 1** (Color online) (a) Schematic of p-GaN gate HEMT on SiC substrate; (b) depth-profile SIMS measurement of Mg ions in the topmost layers of the epi structure.

and thermal mismatch, it is very difficult to grow thick (Al)GaN buffer layers on a silicon substrate, limiting the level of the vertical breakdown.

GaN-on-SiC devices have been used widely in radio frequency applications because of the high-quality GaN epilayer and excellent heat dissipation [14–16]. Compared with a silicon substrate, a semi-insulating SiC substrate cannot conduct electricity and possesses a high critical electric field value. Therefore, the vertical breakdown is rare in GaN-on-SiC devices, and enhancement of $V_{\rm BR}$ is the preferable option. Highly reliable p-GaN gate HEMTs on SiC are fabricated by taking advantage of the low lattice mismatch between GaN and SiC and the good thermal conductivity. Because of their high 2DEG mobility, GaN-on-SiC power devices can achieve a higher power figure-of-merit (FOM) compared with SiC power devices. Because of the declining costs of SiC substrates, p-GaN gate HEMTs on SiC have been identified as promising materials for high-voltage and high-temperature power applications. However, p-GaN gate HEMTs on SiC substrates have not yet been studied intensively.

In this study, we fabricated 1.7 kV normally-off p-GaN gate HEMTs on SiC substrates. The fabricated device with a gate-drain spacing of 23 μm exhibited a remarkably high $V_{\rm BR}$ of 1740 V with substrate grounded, a specific on-resistance ($R_{\rm ON,sp}$) of 9.56 m$\Omega$·cm$^2$, and a high power FOM of 317 MV/cm$^2$. The vertical material breakdown voltage was more than 3 kV. In addition, high-temperature performance tests were conducted up to 500 K, with the material demonstrating good thermal stability throughout. We report on our fabrication of these devices and our evaluation of their properties in the sections that follow.

## 2 Material growth and device fabrication

Normally-off p-GaN transistors were fabricated on semi-insulating SiC substrates using metal organic chemical vapor deposition (MOCVD), as shown in Figure 1(a). P-GaN epilayer consisted of a 17 nm AlN nucleation layer, a 200 nm Fe-doped GaN buffer layer, a 1.08 μm i-GaN buffer layer, a 0.5 nm AlN interlayer, a 29 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, and an 80 nm p-GaN layer. The epilayer material was annealed at 800°C for 20 min. The annealing process was carried out in situ in an $N_2$ atmosphere.

The depth profile of Mg ions obtained by secondary-ion mass spectrometry (SIMS) measurement is displayed in Figure 1(b). The Mg ion concentration was $7.1\times10^{19}$ cm$^{-3}$ in the p-GaN layer. The activated hole concentration reached a value of $1.77\times10^{18}$ cm$^{-3}$, which was measured by a Hall measurement based on the van der Pauw technique and the Hall effect. High-resolution X-ray diffraction (HRXRD) was performed to characterize the crystalline quality. As shown in Figure 2, the full width at half maximum (FWHM) values of the X-ray rocking curves (XRCs) for epitaxial p-GaN layers were approximately 189 and 240 arcsec for the (002) and (102) diffraction patterns, respectively, which are comparable to those for conventional GaN layers on SiC substrates [17].

The device fabrication commenced with p-GaN gate patterning using a low-power inductively coupled plasma etching process. Subsequently, p-GaN etching was performed using a low-power (15 W) $BCl_3/Cl_2$-based inductively coupled plasma etching process with an etching rate of 10 nm/min. The ohmic contacts were realized by evaporating a Ti/Al/Ni/Au metal stack and using rapid thermal processing at 860°C, whereas the p-GaN gate contact was formed by a Ni/Au metal stack. The p-GaN HEMTs were passivated

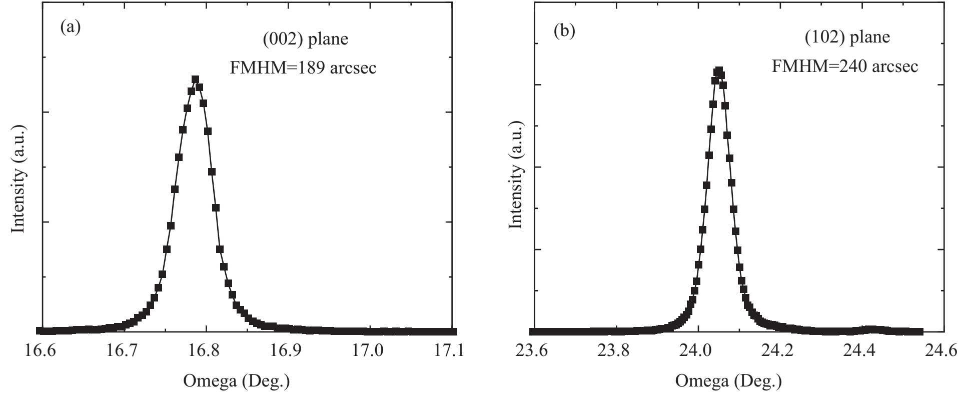


**Figure 2** XRCs of the (a) (002) and (b) (102) diffraction patterns for the p-GaN epilayers on a SiC substrate.

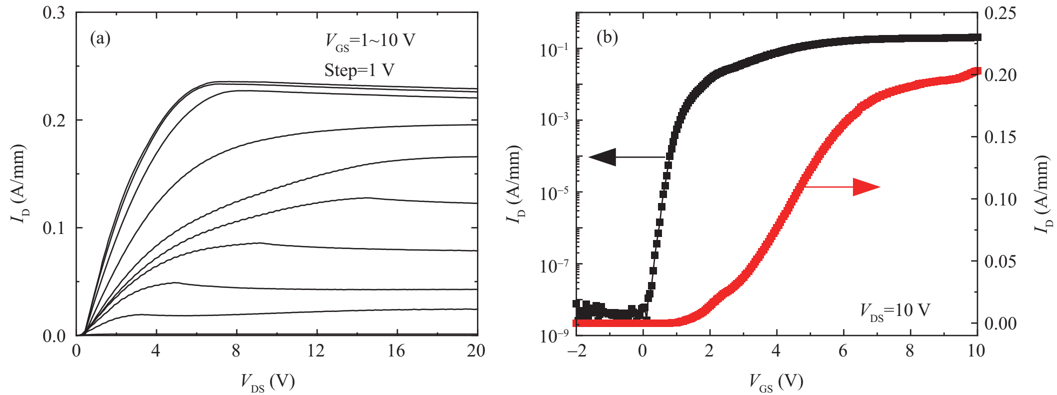


**Figure 3** (Color online) (a) Output and (b) transfer curves of the p-GaN gate HEMT on a SiC substrate with $L_{\rm GD}$ = 5 μm.

with 40 nm $Al_2O_3$ using an atomic layer deposition (ALD) system. The measured p-GaN gate HEMTs on SiC substrates featured a gate length $L_{\rm G}$ = 4 μm, a gate root $L_{\rm GR}$ = 2 μm, a gate-source spacing $L_{\rm GS}$ = 2 μm, and gate-drain spacings $L_{\rm GD}$ = 5/11/17/23 μm.

## 3 Results and discussion

The output and transfer characteristics of the p-GaN gate HEMT with $L_{\rm GD}$ = 5 μm are demonstrated in Figure 3. The maximum drain current $I_{\rm Dmax}$ was 235 mA/mm at $V_{\rm GS}$ = 10 V, and the ON/OFF ratio reached a value of $10^8$. The threshold voltage $V_{\rm TH}$ was 1.10 V, defined at $I_{\rm D}$ = 1 mA/mm. The variation of the knee voltage with $V_{\rm GS}$ (displayed in Figure 3(a)) may be ascribed to the electron Coulomb scattering mechanism and hole carrier injection. With increasing values of $V_{\rm GS}$, the electron density under the gate would increase as well, and the Coulomb scattering would be expected to have a substantial impact on electron carriers. As a further consequence of increasing values of $V_{\rm DS}$, a larger $V_{\rm DS}$ would be required to reach the saturation drain current, resulting in a positive knee-voltage shift for 2 V $\leqslant V_{\rm GS} \leqslant$ 6 V. For $V_{\rm GS}$ > 6 V, the larger number of hole carriers resulting from the increased $V_{\rm GS}$ would inject into the channel, and the current would be increased further, which might weaken the effect of the electron Coulomb scattering mechanism and lead to the negative knee-voltage shift observed for increasing $V_{\rm GS}$ [18]. In order to reduce the 2DEG density under the p-GaN gate and enlarge $V_{\rm TH}$, the AlGaN barrier under the p-GaN gate can be etched partly, or a thin barrier layer can be used [19]. A gate metal with a low work function, a p-GaN bridge, or a p-channel field-effect-transistor bridge can be utilized to increase $V_{\rm TH}$ by increasing the Schottky barrier height [20–23].

The breakdown characteristics of the p-GaN HEMTs on SiC substrates were measured with $V_{\rm GS}$ = 0 V and the substrate grounded, as shown in Figure 4(a). The breakdown voltage $V_{\rm BR}$ was 440 V for the p-GaN HEMT with $L_{\rm GD}$ = 5 μm. The value of $V_{\rm BR}$ increased to 860, 1280, and 1740 V for $L_{\rm GD}$ = 11, 17, and 23 μm, respectively. The breakdown voltage of 1740 V is very high compared with the reported breakdown voltages of p-GaN HEMTs on grounded silicon substrates [5, 12, 13, 20].

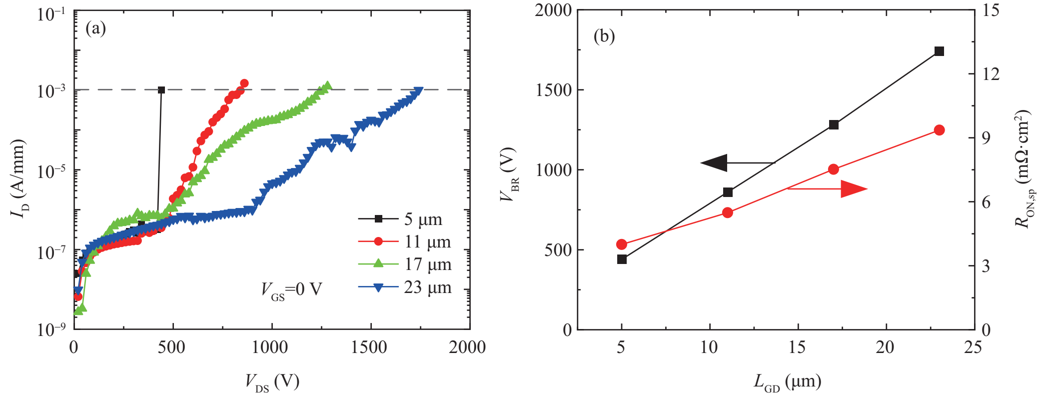


**Figure 4** (Color online) (a) Breakdown characteristics of p-GaN HEMTs as a function of $L_{GD}$; (b) dependence of $V_{BR}$ and $R_{ON,sp}$ on $L_{GD}$. The p-GaN HEMTs breakdown curves were measured with the substrate grounded.

The specific on-state resistance of the p-GaN HEMT with $L_{GD}$ = 5 μm was 18 Ω·mm, and the corresponding $R_{ON}$ was 4.00 mΩ·cm$^2$, taking a transfer length of 1.5 μm for each ohmic contact into account. As shown in Figure 4(b), $R_{ON}$ increased to 9.56 mΩ·cm$^2$ for $L_{GD}$ =23 μm, and the corresponding maximum current $I_{Dmax}$ was 143 mA/mm. For the p-GaN HEMTs on SiC substrates with $L_{GD}$ =23 μm, the power FOM was 317 MV/cm$^2$, which is among the best FOMs of p-GaN gate HEMTs with grounded silicon substrate ever measured. The scope of potential applications of p-GaN HEMTs on SiC substrates could be substantially broadened by increasing the range of possible values of $V_{BR}$ and $R_{ON}$. The p-GaN etching process and ohmic contacts utilized in this study were not completely optimized, and large channel resistivities and ohmic contact resistivities were obtained, leading to the low current density and large $R_{ON}$. The drain current and $R_{ON}$ could be further optimized by employing the ultra-low etching rate technique and optimizing the ohmic contact [13].

In order to investigate the device's performance at high temperatures, a p-GaN HEMT with $L_{GD}$ = 5 μm was tested between 300 and 500 K. The output curves of the p-GaN HEMT at 500 K are displayed in Figure 5(a). The maximum drain current decreased from 235 mA/mm at 300 K to 112 mA/mm at 500 K. The transfer curves of p-GaN HEMT between 300 and 500 K are displayed in Figure 5(b). As shown in Figure 5(c), the shift in $V_{TH}$ between 300 and 500 K can be obtained from the data displayed in Figure 5(b). The value of $V_{TH}$ at 500 K was 1.17 V, and the shift in $V_{TH}$ ($\Delta V_{TH}$) was less than 0.1 V for the entire range of 300–500 K. The dependence of the quantity $I_{D,HT}/I_{D,RT}$ ($I_D$ at high temperature/$I_D$ at room temperature) on temperature is displayed in Figure 5(d). The values of $I_{D,HT}/I_{D,RT}$ were 83%, 62%, 51%, and 48% at 350, 400, 450, and 500 K, respectively. These values were not lower than those reported for p-GaN HEMTs on silicon substrates [24, 25]. The drain current reduction at high temperatures mainly resulted from the severe phonon scattering at high temperatures. The small shift in $V_{TH}$ and the high value of the ratio $I_{D,HT}/I_{D,RT}$ at 500 K indicated that the p-GaN HEMTs on SiC substrates exhibited excellent high-temperature performance.

The values of $V_{BR}$ for p-GaN HEMTs on silicon substrates are limited by the weak breakdown electric field of the silicon substrates. Increasing the GaN buffer thickness is the dominant method used to increase the value of $V_{BR}$ for p-GaN HEMTs on silicon substrates. In contrast, the SiC substrate cannot conduct electricity, and the value of $V_{BR}$ for p-GaN HEMTs on SiC substrates is not limited in the manner applicable to silicon substrates. The measured values of the vertical breakdown voltage for the p-GaN-on-SiC material are presented in Figure 6. The vertical leakage at 3 kV was less than $10^{-2}$ A/cm$^2$, which is a very low value for vertical leakage. Therefore, the p-GaN-on-SiC HEMTs demonstrated their ability to achieve breakdown voltages of 3 kV with the substrate grounded. The substrate-grounded value of $V_{BR}$ for p-GaN HEMTs on SiC substrates can be further improved by using field plates or other termination techniques.

## 4 Conclusion

In summary, we have demonstrated that p-GaN gate HEMTs on SiC deliver high levels of performance. The p-GaN device with $L_{GD}$ = 23 μm exhibited a remarkably high $V_{BR}$ of 1740 V (at 1 mA/mm) with

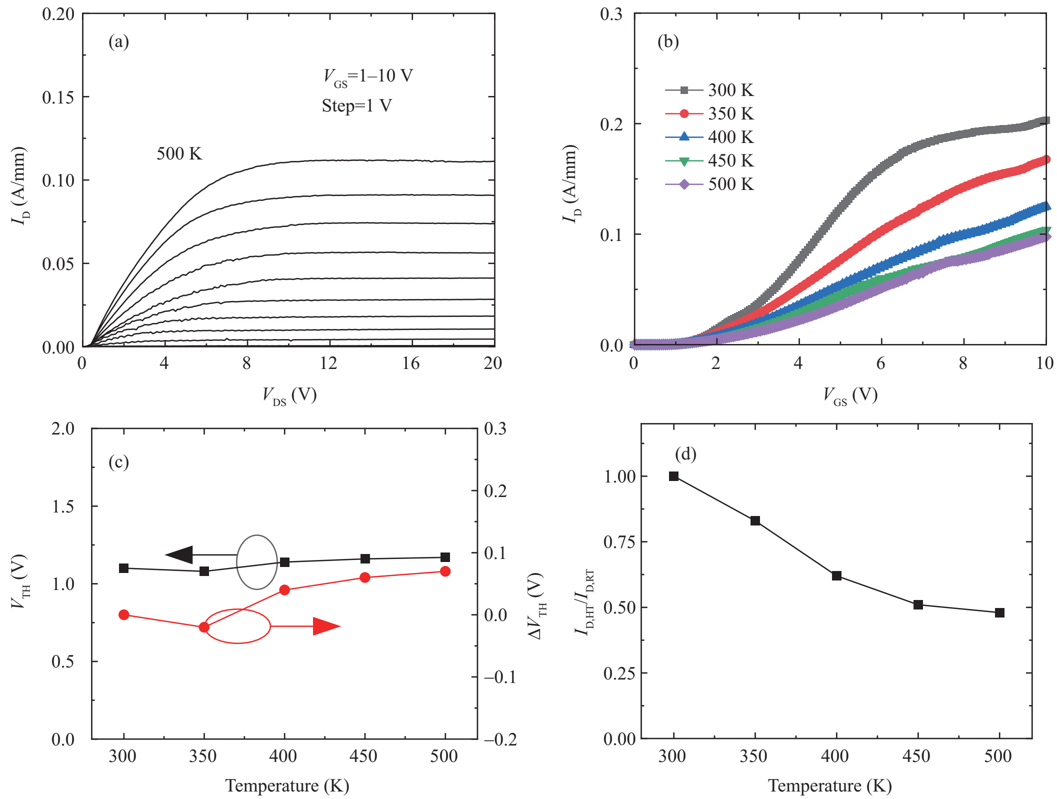


**Figure 5** (Color online) (a) Output curves of p-GaN HEMT at 500 K. (b) Transfer curves of p-GaN HEMTs at 300, 350, 400, 450, and 500 K. Dependence of (c) $V_{TH}$, $V_{TH}$ shift and (d) $I_{D,HT}/I_{D,RT}$ on the temperature.

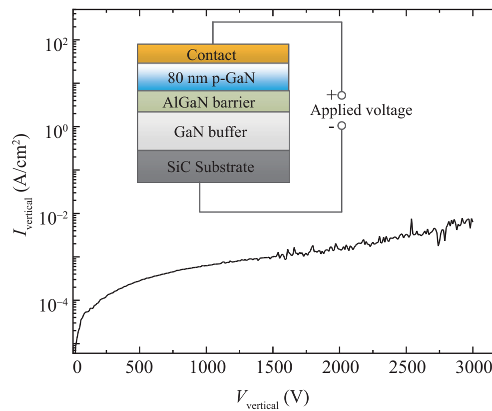


**Figure 6** (Color online) Vertical breakdown measurement for the pGaN-on-SiC material.

substrate grounded, which is not limited by the vertical breakdown mechanism. The shift in $V_{TH}$ and the variation in the maximum drain current were investigated across a range of high temperatures. A vertical breakdown voltage of 3 kV was obtained for p-GaN on SiC material. Experimental results demonstrated that p-GaN-on-SiC HEMTs transcend the vertical breakdown limits of p-GaN-on-Si HEMTs, indicating their potential use in 2 kV high-voltage power applications.

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**References**

1 Mishra U K, Parikh P, Wu Y F. AlGaN/GaN HEMTs — an overview of device operation and applications. Proc IEEE, 2002, 90: 1022–1031

2 Chen K J, Haberlen O, Lidow A, et al. GaN-on-Si power technology: devices and applications. IEEE Trans Electron Dev, 2017, 64: 779–795

3 Xing H, Dora Y, Chini A, et al. High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates. IEEE Electron Dev Lett, 2004, 25: 161–163
4 Xiao M, Du Z, Xie J, et al. Lateral p-GaN/2DEG junction diodes by selective-area p-GaN trench-filling-regrowth in AlGaN/GaN. Appl Phys Lett, 2020, 116: 053503
5 Uemoto Y, Hikita M, Ueno H, et al. Gate injection transistor (GIT) — a normally-off AlGaN/GaN power transistor using conductivity modulation. IEEE Trans Electron Dev, 2007, 54: 3393–3399
6 Wang H, Wei J, Xie R, et al. Maximizing the performance of 650-V p-GaN gate HEMTs: dynamic RON characterization and circuit design considerations. IEEE Trans Power Electron, 2017, 32: 5539–5549
7 Huang X, Liu Z, Li Q, et al. Evaluation and application of 600 V GaN HEMT in cascode structure. IEEE Trans Power Electron, 2014, 29: 2453–2461
8 Tao M, Liu S, Xie B, et al. Characterization of 880 V normally off GaN MOSHEMT on silicon substrate fabricated with a plasma-free, self-terminated gate recess process. IEEE Trans Electron Dev, 2018, 65: 1453–1457
9 Wu Y, Zhang W, Zhang J, et al. Au-free $Al_{0.4}Ga_{0.6}N/Al_{0.1}Ga_{0.9}N$ HEMTs on silicon substrate with high reverse blocking voltage of 2 kV. IEEE Trans Electron Dev, 2021, 68: 4543–4549
10 Cheng K, Liang H, van Hove M, et al. AlGaN/GaN/AlGaN double heterostructures grown on 200 mm silicon (111) substrates with high electron mobility. Appl Phys Express, 2012, 5: 011002
11 Rowena I B, Selvaraj S L, Egawa T. Buffer thickness contribution to suppress vertical leakage current with high breakdown field (2.3 MV/cm) for GaN on Si. IEEE Electron Dev Lett, 2011, 32: 1534–1536
12 Tanaka K, Morita T, Umeda H, et al. Suppression of current collapse by hole injection from drain in a normally-off GaN-based hybrid-drain-embedded gate injection transistor. Appl Phys Lett, 2015, 107: 163502
13 Jiang H, Lyu Q, Zhu R, et al. 1300 V normally-off p-GaN gate HEMTs on Si with high on-state drain current. IEEE Trans Electron Dev, 2021, 68: 653–657
14 Lu W, Yang J W, Khan M A, et al. AlGaN/GaN HEMTs on SiC with over 100 GHz f/sub T/ and low microwave noise. IEEE Trans Electron Dev, 2001, 48: 581–585
15 Wu Y F, Saxler A, Moore M, et al. 30-W/mm GaN HEMTs by field plate optimization. IEEE Electron Dev Lett, 2004, 25: 117–119
16 Lee D S, Gao X, Guo S, et al. 300-GHz InAlN/GaN HEMTs with InGaN back barrier. IEEE Electron Dev Lett, 2011, 32: 1525–1527
17 Feng Y, Sun H, Yang X, et al. High quality GaN-on-SiC with low thermal boundary resistance by employing an ultrathin AlGaN buffer layer. Appl Phys Lett, 2021, 118: 052104
18 Greco G, Iucolano F, Roccaforte F. Review of technology for normally-off HEMTs with p-GaN gate. Mater Sci Semicon Proc, 2018, 78: 96–106
19 Zhong Y, Sun Q, Yang H, et al. Normally-off HEMTs with regrown p-GaN gate and low-pressure chemical vapor deposition $SiN_x$ passivation by using an AlN pre-layer. IEEE Electron Dev Lett, 2019, 40: 1495–1498
20 Zhang L, Zhou H, Zhang W, et al. AlGaN-channel gate injection transistor on silicon substrate with adjustable 4-7-V threshold voltage and 1.3-kV breakdown voltage. IEEE Electron Dev Lett, 2018, 39: 1026–1029
21 Chen J, Hua M, Wang C, et al. Decoupling of forward and reverse turn-on threshold voltages in schottky-type p-GaN gate HEMTs. IEEE Electron Dev Lett, 2021, 42: 986–989
22 Hwang I, Oh J, Choi H S, et al. Source-connected p-GaN gate HEMTs for increased threshold voltage. IEEE Electron Dev Lett, 2013, 34: 605–607
23 Hwang I, Kim J, Choi H S, et al. p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current. IEEE Electron Dev Lett, 2013, 34: 202–204
24 Zhang C, Li S, Liu S, et al. Electrical performances and physics based analysis of 650V E-mode GaN devices at high temperatures. In: Proceedings of the 26th International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA), Hangzhou, 2019
25 Hao R, Fu K, Yu G, et al. Normally-off p-GaN/AlGaN/GaN high electron mobility transistors using hydrogen plasma treatment. Appl Phys Lett, 2016, 109: 152106