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A 70%-power transmission efficiency, 3.39 Mbps power and data telemetry over a single 13.56 MHz inductive link for biomedical implants

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Abstract The application of wireless power and data telemetry to implantable medical devices (IMDs) has grown dramatically in recent decades. Achieving a high data rate and high-power transmission efficiency (PTE) over the same inductive link remains challenging. This paper presents a power and data telemetry circuit over a single 13.56 MHz inductive link. On the transmitter (TX) side, a binary-phase-shift keying (BPSK) modulation based on a Class-E amplifier that features a high modulation rate and a high quality (Q)-factor is proposed. A digital-assisted phase-locked-loop (PLL) is proposed on the receiver (RX) side as a BPSK demodulator to handle the long settling process. The maximum data rate can be extended to 1/4 of the carrier frequency. The prototype has been fabricated with a 180 nm BCD (Bipolar-CMOS-DMOS) process. The measurement shows that up to 31.25 mW of power can be delivered simultaneously with 3.39-Mbps of data transmission, while a 2×10^{-7} bit-error-rate (BER) can be ensured over a transmission distance of 5 mm. The peak PTE is 70%, whereas the RX energy efficiency is 183 pJ/bit. The results demonstrate the potential of the proposed techniques in applications to various biomedical implants with intensive bandwidth and energy efficiency requirements.

Keywords power and data telemetry, inductive link, implantable medical device (IMD), brain-computer interface (BCI), phase-locked-loop (PLL), binary-phase-shift keying (BPSK), power transfer efficiency (PTE)

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1 Introduction

Wireless data telemetry has been used extensively in biomedical implants [1–3], body area networks (BANs) [4–6], and smart sensor nodes [7]. Particularly, in biomedical implants that interface with the central neural system, such as cochlear implants and visual prostheses, a large volume of data are required to be transmitted through multiple channels. In such scenarios, a robust downlink between the external devices and the implantable medical devices (IMDs) with an over Mbps data rate is highly required [8]. In addition, because of safety concerns regarding biomedical implants, wireless power transfer is preferred over using the battery supply to continuously power the IMDs. The typical power transmission distance depends on the applications. For example, invasive brain-computer interfaces (BCIs) need to be placed inside the 1–3 mm epidural spacing between the outer surface of the brain and the skull [9]. At the same time, the retina prostheses implants are expected to be placed inside the eyeball through a 5-mm incision [10]. The power requirement of biomedical implants typically ranges from hundreds of microwatts to tens of milliwatts [11].

Wireless power and data telemetry over the inductive links have been investigated in-depth [12–16]. The main challenges are the extremely limited space and available power to establish a wideband and

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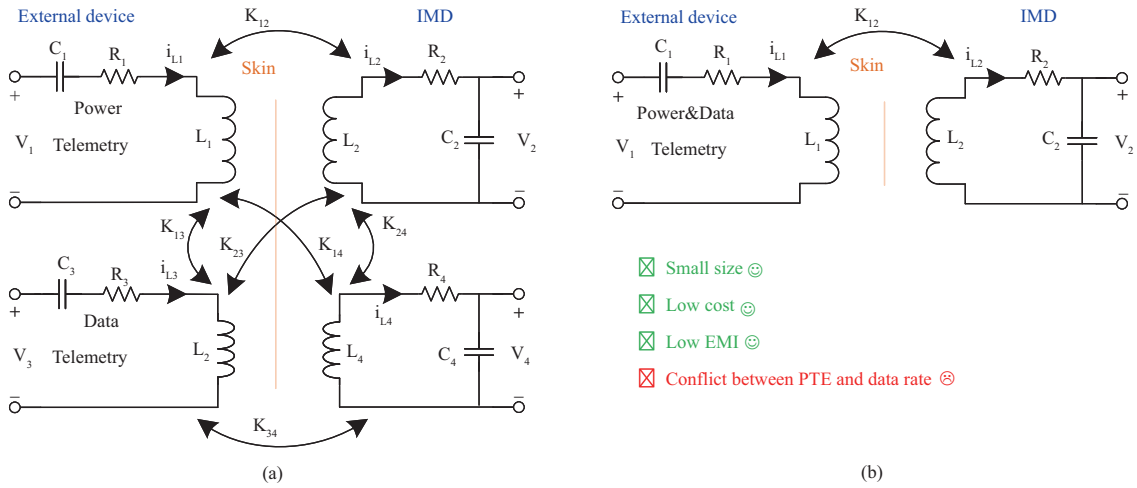

Figure 1 (Color online) Wireless power and data telemetry. (a) Dual inductive links; (b) single inductive link.

robust connection between the IMDs and the external devices. Thus, the main target is to increase the power transmission efficiency (PTE) while realizing compact, high data rate and low bit-error-rate (BER) IMDs with minimal power consumption. Typically, a high-frequency data carrier (>50 MHz) is required to extend the data rate, whereas a lower frequency power carrier (<20 MHz) should be kept to reduce the electromagnetic (EM) field absorption in the tissue [15]. This circumstance has led to the conventional use of dual-carrier power and data links with a separate pair of coils for each link [12,14,15], as shown in Figure 1(a). Although each link can be optimized independently with separately dedicated channels, this approach needs more complex circuits and coil structures, resulting in a bulky system. Furthermore, the dual-link approach also suffers from strong crosstalk between the power and data links, thereby leading to a high BER.

In contrast, simultaneous power and data transmission using a single inductive link instead of multiple links enables a compact biomedical implant while alleviating design constraints on biological and physical aspects, as shown in Figure 1(b). It also reduces the possibility of human exposure to EM fields or disturbances that might affect the functionality of the implant because of electromagnetic interference (EMI) [17]. Nevertheless, simultaneous high PTEs and high data rates are difficult to obtain over the same inductive link due to many conflicting requirements. For example, on the transmitter (TX) side, a high quality-factor (Q) resonant network is highly desirable to improve the PTE. However, this attribute not only raises major problems such as sensitivity to tolerances and environmental factors, but also severely restricts the available bandwidth and thus the downlink data rate [18].

Most conventional modulation techniques, such as amplitude-shift keying [19], frequency-shift keying (FSK) [8], or phase-shift keying (PSK) [20], cannot address the aforementioned conflicts between high PTEs and high bandwidth. Recently, several attempts have been made to address these challenges by adopting appropriate modulation schemes. Ref. [21] proposed a novel carrier-width modulation (CWM), allowing simultaneous power and data transmission over a single 27.12 MHz inductive link. It achieves a 9.04 Mbps data rate with only 13.68 μW of power consumption. However, the concept is only partially proved since only the demodulator has been fabricated and tested, where an arbitrary signal generator is used instead of an actual inductive link. A fully integrated power and data telemetry with binary-phase-shift keying (BPSK) modulation has been proposed in [22]. However, it only achieves a low data rate (16 kbps). Moreover, an energy storage battery is still required to charge the IMD, which occupies additional volume and raises safety concerns. An energy recycling telemetry with simultaneous 11.5 mW of power and 6.78 Mbps of data delivery over a single 13.56-MHz inductive link with a new cyclic on-off keying (COOK) has been proposed in [23]. However, only backward data telemetry is supported. A single-die inductive antenna driver, tuner, and modulator are presented in [18]. With instantaneous response adaptive-predictive self-tuning, it allows data modulation rates to exceed the classical restrictions of a high Q-factor antenna. Nevertheless, the data rate is still limited to 500 kbps. In conclusion, a single inductive downlink that efficiently delivers tens of milliwatts of power and Mbps data is still lacking.

Therefore, this paper presents simultaneous power and data telemetry over a single 13.56-MHz inductive link for biomedical implants. It introduces several innovations, as follows. On the TX side, a BPSK

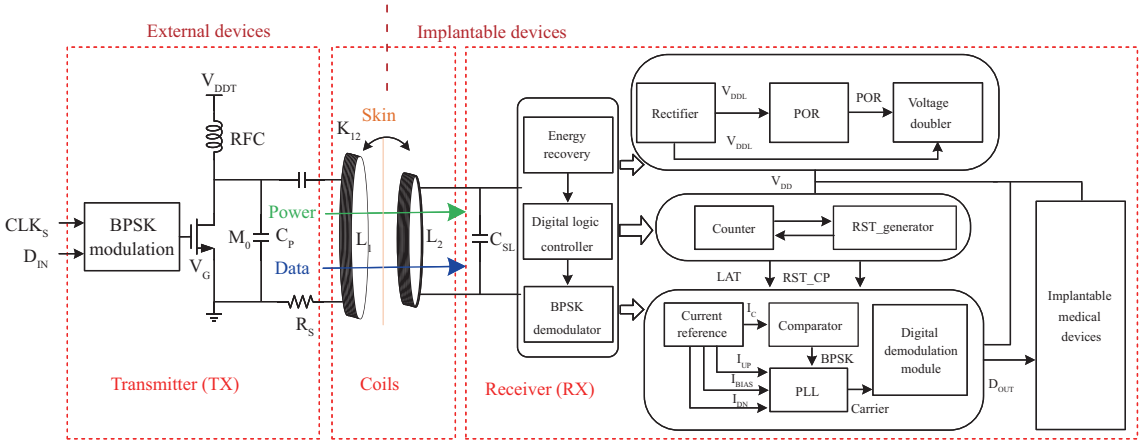

Figure 2 (Color online) Architecture of the proposed power and data telemetry over a single inductive link.

modulated Class-E amplifier that completes the data modulation within two carrier cycles is proposed. This technique features a high modulation rate and a high Q-factor. On the receiver (RX) side, an innovative digital-assisted loop reset control is proposed to handle the long settling process of the phase-locked-loop (PLL) demodulator. This technique extends the maximum data rate to 1/4 of the carrier frequency. The prototype has been fabricated with a 180 nm BCD (Bipolar-CMOS-DMOS) process. The measurement shows that up to 31.25 mW of power and 3.39-Mbps of data can be transmitted simultaneously. A 2×10^{-7} BER can be ensured over a transmission distance of 5 mm. The peak PTE is 70%, whereas the energy efficiency of the RX is 183 pJ/bit.

The rest of the paper is organized as follows. Section 2 discusses the proposed architecture, with the circuit implementation detailed in Section 3. Section 4 shows the measurement results, while the conclusion is drawn in Section 5.

2 Proposed architecture

Figure 2 shows the architecture of the proposed power and data telemetry, which consists of an TX, and an RX linked by a single pair of inductive coils. The TX transmits the power and data as an external device, whereas the implanted RX implements the function of power conversion and data demodulation. The recovered power and data can be delivered to the subsequent IMDs.

On the TX side, the data to be transmitted is modulated to the carrier. The modulated signal then drives the primary coil via a Class-E amplifier. Since the BPSK modulation can be completed within two carrier cycles, independent of the Q-factor of the resonant network, the conflicts between high PTE and high bandwidth can be eliminated, leading to a simultaneous high modulation rate and high PTE.

On the RX side, the received power coupled on the secondary coil is recovered by the energy recovery circuit. The circuit consists of a rectifier that drives a voltage doubler. The DC voltage is boosted and then delivers the power to the demodulator. The energy can be stored or delivered to other functional blocks such as nerve stimulators. An innovative digital-assisted PLL has been proposed as a BPSK demodulator. A reset-control loop has been implemented to deal with the long settling process. It resets the PLL and latches the recovered data when the input phase transitions. The benefit is that the data rate can be significantly extended.

The pair of inductive coils has been optimized with an HFSS simulator (ANSYS Inc.). Since the coil structure affects the quality factor, coupling coefficient, and mutual inductance, it must be carefully optimized to suit the implantable devices [24]. The coupling coefficient would be slightly affected due to the EM field absorption of the skin and tissue. This factor needs to be considered as well to leave a sufficient margin for the coil parameters. Besides, the optimization process considers the coils' skewing. The spiral printed-circuit-board (PCB) based coils have been optimized with the outer (inner) diameter of 27.14 mm (1.95 mm) for both TX/RX coils. The inductance of the coil is 1.58 μH at 13.56 MHz.

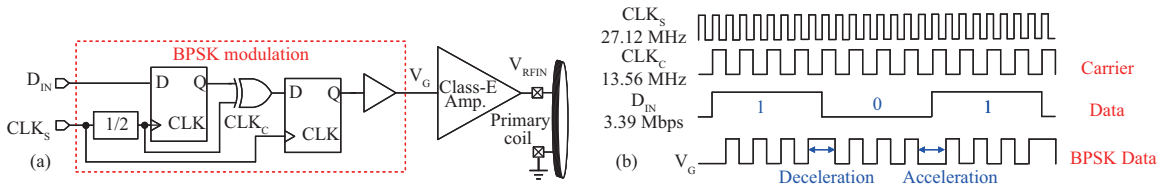

Figure 3 (Color online) (a) Schematic of the BPSK demodulation circuit and (b) illustration of the timing diagram.

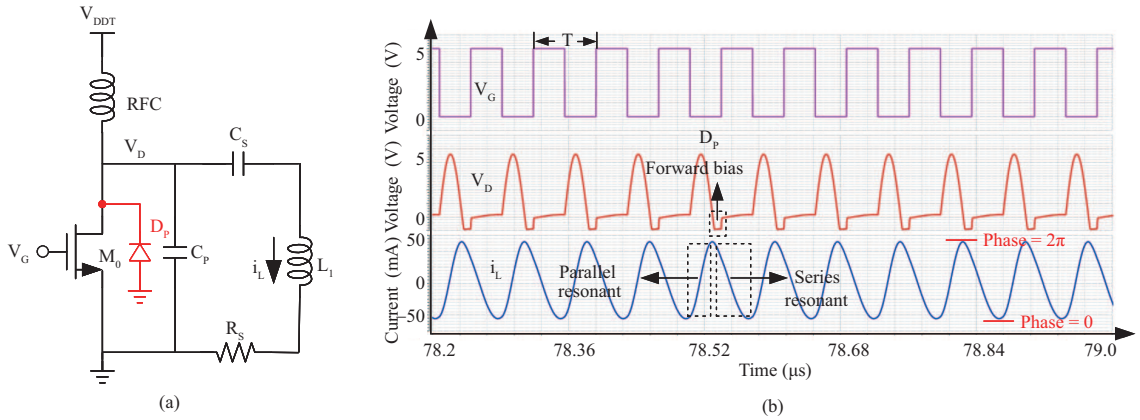

Figure 4 (Color online) (a) Schematic of the Class-E amplifier and (b) simulation waveform of the Class-E amplifier.

3 Circuit implementation

3.1 BPSK modulator and TX

Figure 3(a) shows the proposed BPSK modulator. The BPSK signal (V_G) is generated according to the input data (D_{IN}). Figure 3(b) illustrates its timing diagram. The phase of V_G is binary modulated. When the data transitions from '1' to '0', the phase is in 'deceleration' mode. On the contrary, when the data transitions from '0' to '1', the phase is in 'acceleration' mode. V_G is buffered before driving the Class-E amplifier.

Figure 4(a) shows the schematic of the Class-E amplifier. The binary-resonance-frequency loading network of L_1, C_S, and C_P is of particular interest. When M_0 is turned on, the capacitor C_P is shorted, and the resulting network has the series resonance frequency of ω_s, which can be expressed as

$$\omega_s = \frac{1}{\sqrt{L_1 \cdot C_s}}, \tag{1}$$

when M_0 is turned off, the inductor L_1 and the connected capacitors C_P and C_S determine the parallel resonance frequency ω_p, which is higher than ω_s and can be expressed as

$$\omega_p = \frac{1}{\sqrt{L_1 \cdot \frac{C_s \cdot C_p}{C_s + C_p}}}. \tag{2}$$

Figure 4(b) shows the transient simulation waveform of the Class-E amplifier. The phase of the inductor current i_L is the integration of the resonance frequency over time. Therefore, the integration slope is larger in the parallel resonance mode than in the series resonance mode. It can be inferred that under certain conditions of ω_s and ω_p, the phase of i_L can be modulated within two carrier cycles. Figure 5 illustrates the method to calculate the parameters of the components to achieve BPSK. The purpose is to modulate the phase of i_L by $m \cdot \pi$ within two cycles, where m ($\leqslant 1$) is a constant. One critical effect is the forward bias of the parasitic diode D_P from M_0's 'body' to 'drain'. During the typical Class-E mode, M_0 is turned on when its drain voltage (V_D) is zero (known as zero voltage switching, ZVS). Under the ideal ZVS condition, the power loss due to D_P can be ignored, so that the PTE can be maximized. However, in the proposed TX, the phase (or duty-cycle) of V_G is modulated, ZVS cannot always be ensured. When V_D is negative, D_P will be forward biased, shorting C_P while keeping series resonant. The parallel resonant

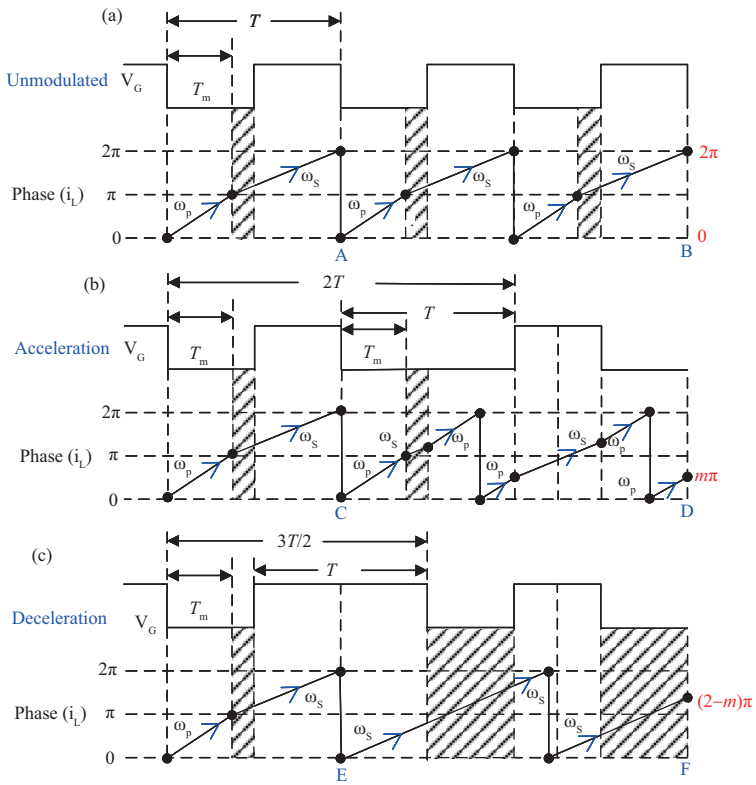

Figure 5 (Color online) Phase of inductor current. (a) Umodulated mode; (b) acceleration mode; (c) deceleration mode.

is achieved when M_0 is turned off while V_D is still positive. Considering the forward-bias effect of D_P (as denoted by the shadow area), the parameters for BPSK can be calculated as follows.

In Figure 5(a), the phase of V_G is unmodulated; from A to B, one can get the following equation:

$$\omega_p \cdot 2T_m + \omega_s \cdot 2(T - T_m) = 4\pi, \tag{3}$$

where $T = 1/\omega$ is the period of the carrier, T_m is the time in series resonance mode during each carrier cycle.

In Figure 5(b), the phase is in 'acceleration' mode; from C to D, one can get the following equation:

$$\omega_p \cdot (T + T_m) + \omega_s \cdot (T - T_m) = 4\pi + m \cdot \pi. \tag{4}$$

In Figure 5(c), the phase is in 'deceleration' mode; from E to F, one can get the following equation:

$$\omega_s \cdot 2T = 4\pi - m \cdot \pi. \tag{5}$$

Given a specific value of m, Eqs. (3)–(5) can be solved. Then the parameters of C_S and C_P can be obtained by (1) and (2). In this design, $C_S = 132$ pF and $C_P = 86$ pF are chosen. The nominal frequency of ω_s and ω_p equals $5/6\omega$ and $4/3\omega$, respectively. As a result, the carrier phase can be modulated by $\pm 2/3\pi$ within two carrier cycles in 'acceleration' and 'deceleration' modes. Due to the parasitic capacitance at the PCB level, ω_s and ω_p might deviate from the nominal frequency so that the phase modulation value might be shifting. However, the PLL-based demodulation can still be correctly performed as long as the phase modulation value is larger than zero (detailed in Subsection 3.3). This ensures the robustness of TX to the parasitic parameters.

The quality factor Q of the series branch of L_1-R_S-C_S network is defined as $\omega \cdot L_1 \cdot C_S$. From (3)–(5), as long as the period of the carrier is fixed, the BPSK modulation can be completed within two carrier cycles, regardless of the quality factor Q. Figure 6 shows the simulation waveform of the BPSK modulated Class-E amplifier with different values of Q (= 4/20/100). The waveform demonstrates that the proposed circuit exactly modulates the phase by $2/3\pi$ within two carrier cycles. Therefore, a high Q-factor can be adopted without slowing down the modulation so that both high PTE and high data rate can be obtained

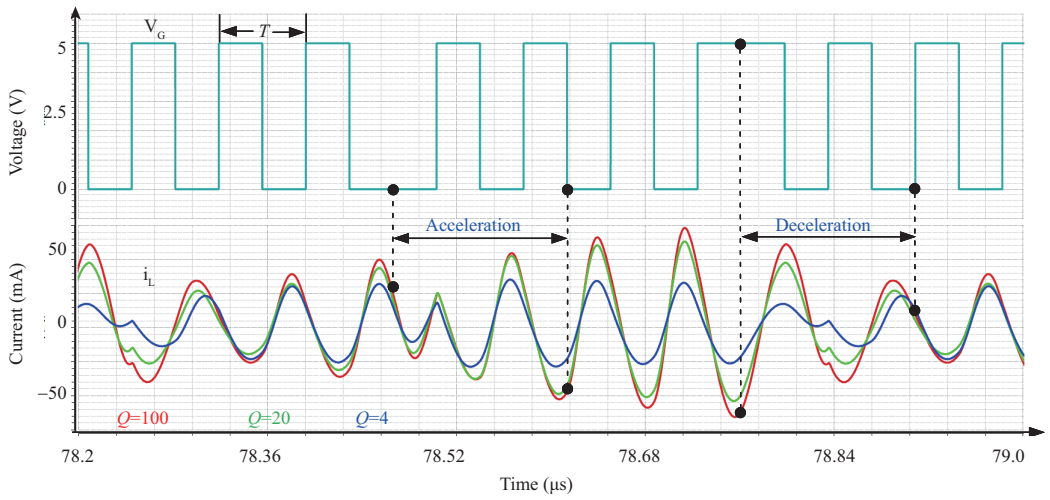

Figure 6 (Color online) Simulation waveform of the BPSK modulated Class-E amplifier.

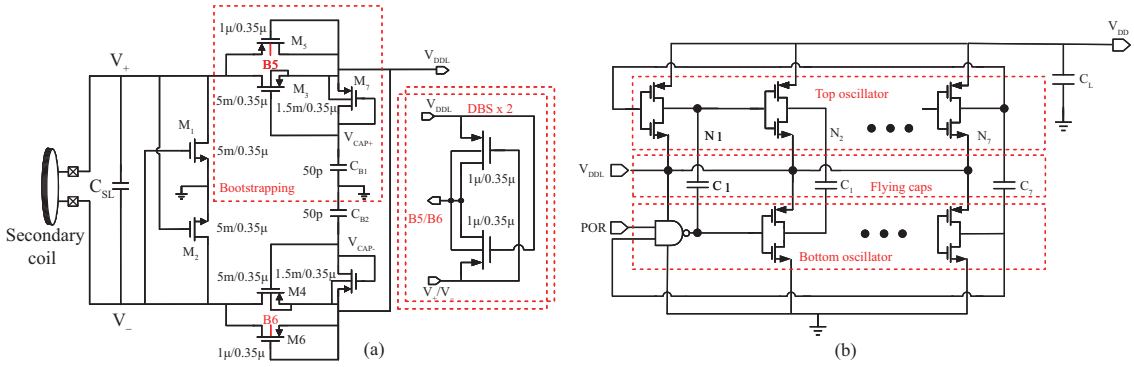

Figure 7 (Color online) Schematic of (a) the full-wave rectifier and (b) the voltage doubler.

simultaneously. This unique feature contrasts the conventional BPSK modulation, where the Q-factor determines the duration of the modulation process. Although the non-ZVS operation increases power loss compared to the conventional ZVS operation as the cost, the data rate can be increased significantly as the benefit. In addition, the power loss can be partially compensated through the adoption of high-Q resonant tank or by optimizing the duty cycle of the carrier signal to achieve near-ZVS operation. However, this will introduce hardware overhead, so that a 50% duty cycle is adopted in our design.

3.2 Energy recovery circuit

The energy recovery circuit that powers the IMDs consists of a full-wave rectifier and a voltage doubler. Figure 7(a) shows the schematic of the full-wave rectifier [25]. It generates a DC output voltage (V_{DD}) from the AC input coupled from the secondary coil. Instead of the low-threshold transistors, the normal threshold power transistors M_3 and M_4 are employed to decrease the power loss due to the leakage current. However, the power conversion efficiency is adversely affected due to the relatively higher threshold voltage of M_3 and M_4. Therefore, the bootstrapping circuit is adopted. The voltage held on the capacitor is around twice as high as the PMOS threshold voltage below the input voltage. As a result, the effective threshold voltage of the rectifier is reduced to $V_{TH3} - V_{TH7}$, where V_{TH3} and V_{TH7} are the threshold voltage of the M_3 and M_7, respectively. Furthermore, the dynamic bulk switching (DBS) technique is applied to bias the bulk of M_5 and M_6. Therefore, the leakage current into the substrate can be lower and thereby prevent the latch-up issue.

Figure 7(b) shows the schematic of the self-oscillating voltage doubler following the full-wave rectifier [26]. It consists of two stacked ring oscillators with output nodes of corresponding stages connected through flying capacitors (C_1 to C_7). In each stage, inverters from the top and bottom ring either charge or discharge the flying capacitors, thereby transferring power to V_{DD}. The top oscillator starts regular oscillation on its own as V_{DD} rises higher than V_{DDL}. Since the top oscillator is initially much weaker

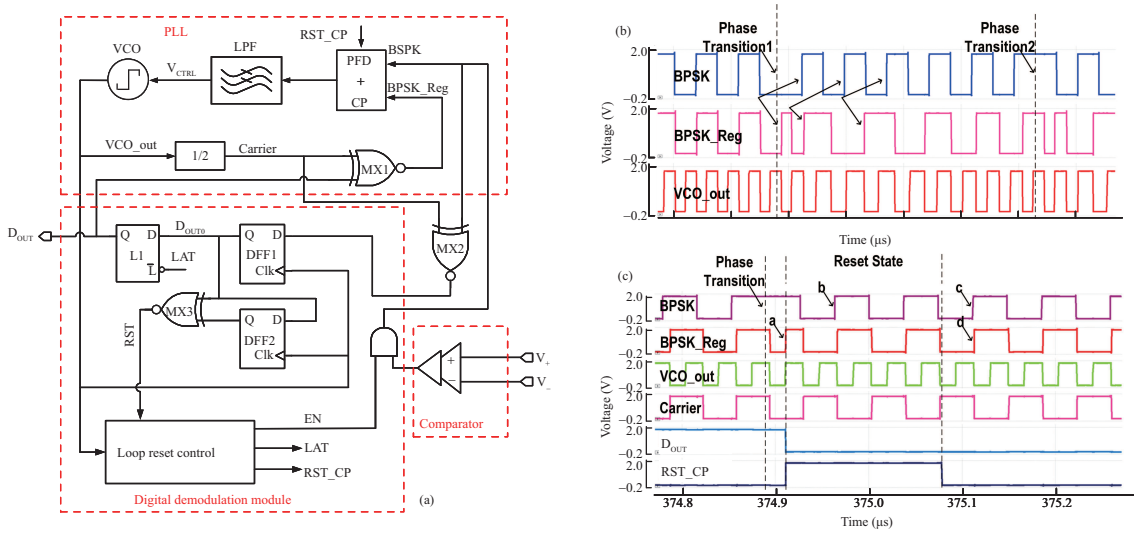

Figure 8 (Color online) (a) Schematic of the PLL; (b) simulation waveform without digital-assisted reset control; (c) simulation waveform with digital-assisted reset control.

than the bottom, the top oscillation is naturally synchronized to the bottom oscillator. After synchronization, the voltage doubler starts regular operation, boosting the output voltage. The real value of V_{DD} is less than $2{\cdot}V_{DDL}$ because of the parasitic effects. The output can be regulated to the target value at the cost of contention loss as well. Nevertheless, it is unnecessary to implement the output regulation as long as V_{DD} is within the acceptable range to enable the subsequent circuit.

3.3 Digital-assisted PLL

A digital-assisted PLL is proposed to demodulate the data from the received signal. Figure 8(b) shows the transient simulation waveform in the conventional PLL. At phase transition 1, the PLL loses the lock state. Thus the following data cannot be correctly demodulated until it restores lock again. The recovery process from the unlock state relates to PLL's bandwidth and fundamentally limits the maximum data rate, which is normally constrained to around 1/8 of the carrier frequency [27]. In other words, with a carrier frequency of 13.56 MHz, the maximum data rate is 1.7 Mbps. In reality, the data rate can hardly reach 1 Mbps to ensure a sufficient performance margin. Inspired by [22], we therefore propose a digital control circuit that resets the charge-pump (CP) to maintain PLL's lock state and then demodulates the data. We proved the idea with circuit simulation [28], hereby we provide detailed analysis and real silicon verification. With the proposed technique, the PLL's bandwidth no longer limits the maximum data rate, which is to be improved significantly.

Figure 8(a) shows the schematic of the proposed PLL-based demodulator. A compactor converts the input analog BPSK signal to the digital counterpart 'BPSK'. The PLL circuit is executed to synchronize the phase between 'BPSK' and the feedback signal 'BPSK_Reg'. The latter is the product of the carrier signal 'Carrier' and the recovered data 'D_{OUT}', where the carrier signal is with half the frequency of the voltage-controlled oscillator (VCO). A simple XNOR digital gate MX1 performs the mixing operation to generate the product. When the PLL is locked in phase, the frequency of the VCO's output signal is twice that of the incoming carrier frequency. Another XNOR gate (MX2) mixes 'BPSK' and 'Carrier'. Its output is then synchronized by the VCO's output with a D flip-flop (DFF1). The demodulated data ('D_{OUT}') can be acquired by latching the output from DFF1. In the conventional PLL, the phase difference of two transition edges between 'BPSK' and 'BPSK_Reg' could lead to error pulses in the output of the phase-frequency detector (PFD). The error pulses could disturb PLL's lock state, thereby resulting in error bits. To eliminate the error, at phase transition edges, the proposed PLL enters the reset phase by setting the reset signal 'RST' and generating the 'LAT' and 'RST_CP' signals. The 'LAT' signal latches the data in one previous cycle through L1, whereas the 'RST_CP' signal keeps the charge-pump (CP)'s output voltage unchanged during phase transition. As shown in Figure 8(c), in the reset phase, the phase difference between the rising edges 'a' and 'b' will not be detected so that the VCO keeps running at the locking frequency. The reset phase ends after 4.5 VCO cycles. By then the VCO

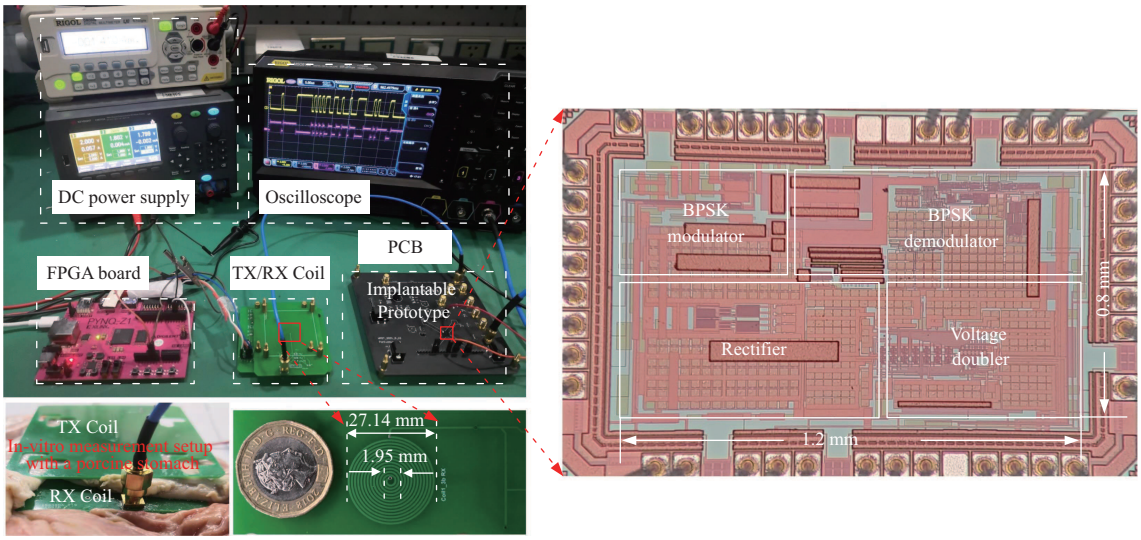

Figure 9 (Color online) The coil, PCB, measurement platform and the die photograph of the prototype.

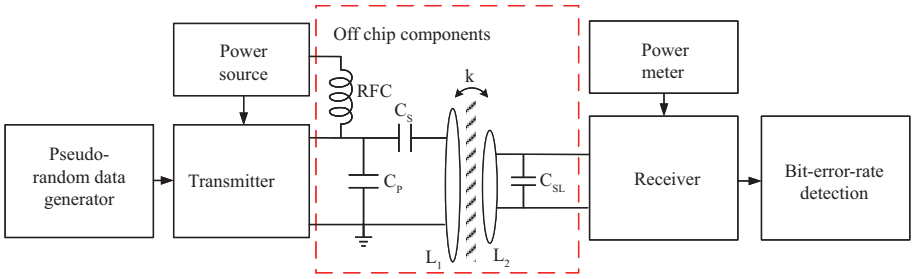

Figure 10 (Color online) The experiment setup for the BER and power efficiency measurement.

is reconnected to the PLL loop, and the PFD detects the phase difference between the rising edges 'c' and 'd'. Since the free-running VCO almost keeps the locking frequency, the phase difference between the rising edges 'c' and 'd' has a value close to zero. After the VCO is reconnected, only minor phase adjustment is required to recover the lock state, thus eliminating the long settling process.

Considering the phase of the data is modulated within two carrier cycles (4 VCO cycles), 4.5 VCO cycles are allocated for the reset phase. As a result, within an entire minimum data period (correspondent to 8 VCO cycles), the remaining 3.5 VCO cycles are allocated for phase adjustment after the VCO is reconnected. By reducing the duration time for the phase adjustment, the data rate can be further improved. However, this could lead to more settling errors and thereby increase the BER. With the proposed demodulator, the maximum data rate is equal to 1/4 of the carrier frequency, doubled value compared with the conventional PLL-demodulator, without introducing any power consumption overhead.

The digital-assisted loop reset control circuit consists of a counter clocked by the VCO. When the 'RST' signal is generated, the counter is kick-started and ends the reset phase after 4.5 VCO cycles later. It also generates the enable signals sequentially for the latch, VCO, and RST generation circuit to initialize the PLL after the whole system powers up correctly.

4 Measurement results

The proposed power and data telemetry circuit has been implemented with a 180 nm BCD technology. The core area is 0.96 mm^2. Figure 9 shows the die photograph of the prototype. The TX/RX coil, PCB, and the measurement platform to verify the prototype are shown in the figure as well. Figure 10 shows the experiment setup for the BER and PTE measurement, where a pseudo-random data sequence is generated and then modulates the Class-E amplifier on the TX side. At the same time, the energy and data are recovered on the receiver side. In our measurement, the Xilinx FPGA development board PYNQ-Z1 (Digilent Inc) is adopted to generate the pseudo-random BPSK data. The Class-E amplifier utilizes an

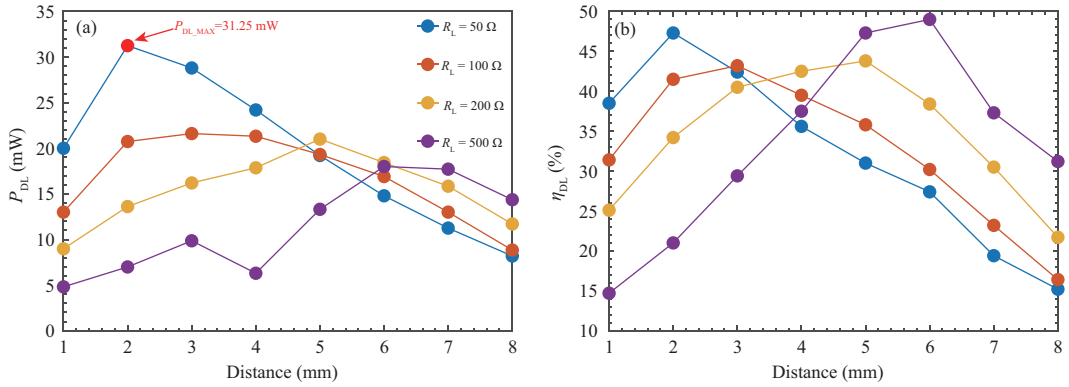

Figure 11 (Color online) Measurement results versus transmission distance with R_L (Data rate = 3.39 Mbps, V_{DDT} = 2 V). (a) Delivered power (P_{DL}); (b) power transmission efficiency (η_{DL}).

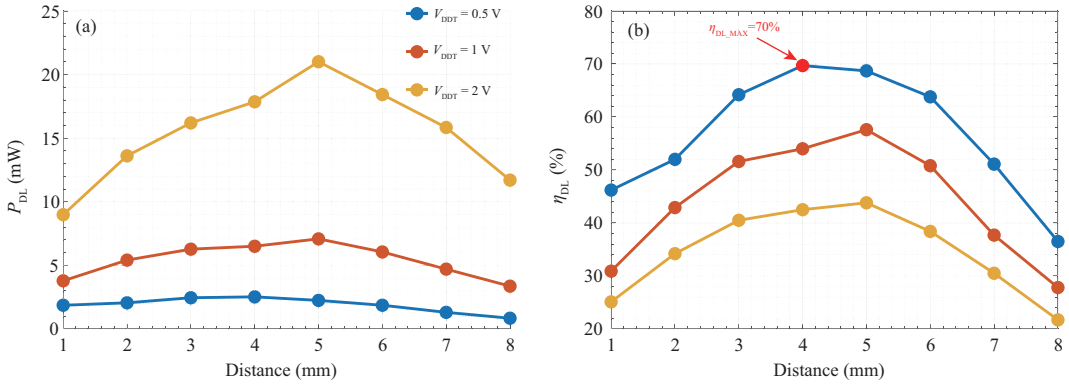

Figure 12 (Color online) Measurement results versus transmission distance with different V_{DDT} (Data rate = 3.39 Mbps, R_L = 200 Ω). (a) Delivered power (P_{DL}); (b) power transmission efficiency (η_{DL}).

off-chip power MOSFET (Rohm Semiconductor, RSF014N03TL). The delivered power and demodulated data are subsequently measured for the calculation of the PTE and BER. The power efficiency can be measured by dividing the received power on the load resistance with a certain value by the transmitted power on the TX side. The BER can be calculated by comparing the original data sequence with the received data and detecting the error bit.

4.1 Power telemetry

To verify the power telemetry, the delivered power (P_{DL}) versus the transmission distance is measured with different load resistance (R_L), transmission voltage (V_{DDT}) and data rate. The PTE (η_{DL}) is then calculated by the ratio of the delivered power and the total power consumed by the TX.

Figure 11 shows the measured P_{DL} and η_{DL} with different R_L. With increasing transmission distance, P_{DL} reaches its peak and then drops gradually. The peak value of P_{DL} is obtained at the impedance matching point between the source resistance and R_L. The maximum delivered power is 31.25 mW when V_{DDT} = 2 V (η_{DL} = 47.3%). The power could be further increased by increasing V_{DDT}. However, since the peak voltage of V_D in the Class-E amplifier stays around $3{\cdot}V_{DDT}$, the power switch M_0 has to withstand the increasing voltage stress as V_{DDT} rises.

Figure 12 shows the measured P_{DL} and η_{DL} with different V_{DDT}. The maximum delivered power (P_{DL_MAX}) is rising as the increasing V_{DDT}, whereas the η_{DL} is dropping. This outlines the basic trade-off between the P_{DL} and η_{DL}, so that the optimum V_{DDT} can be chosen accordingly. The maximum power transmission efficiency (η_{DL_MAX}) is 70% (P_{DL} = 2.5 mW). When transmitting 2.26 Mbps data under 0.5 V transmission voltage, the total power consumption is 2.95 mW. The power transmitted by the TX, received by the coupling coil and delivered to the load (start-up circuit and demodulator) are 1.48, 1.21 and 0.82 mW, respectively, corresponding to 50.2%, 81.8% and 67.8% power efficiencies for the TX, coupling coils and RX. Through simulation check, the power efficiencies are 87.6% and 78.2% for the rectifier and the voltage doubler, respectively. The overall simulated efficiency is 68.4%, which agrees

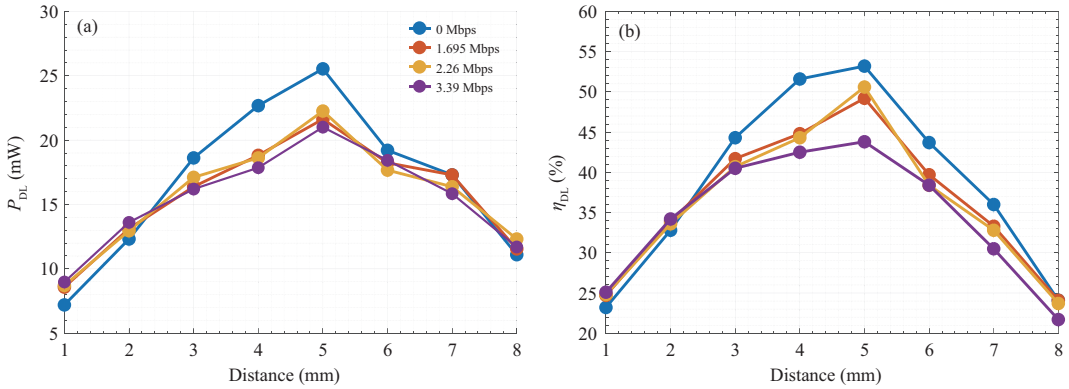

Figure 13 (Color online) Measurement results versus transmission distance with different data rates (V_{DDT} = 2 V, R_L = 200 Ω). (a) Delivered power (P_{DL}); (b) power transmission efficiency (η_{DL}).

quite well with the measurement result of 67.8%. The efficiency is comparable to the state-of-the-art studies [29, 30].

Figure 13 shows the measured P_{DL} and η_{DL} with different data rates. Interestingly, P_{DL} and η_{DL} do not change significantly as the data rate increases. For example, the peak η_{DL} only reduces by 9% (from 53% to 44%) without and with data telemetry up to 3.39 Mbps. The reduction is mainly due to the increase in switching loss in the power transistor during data transmission. This proves the effectiveness of the proposed BPSK modulation, where the PTE is not necessary to trade with the data rate as in the conventional power and data link. The PTE without data transmission is measured as well, as shown by the blue curve in the figure. The result indicates the PTE is mainly limited by the loss of Class-E amplifier under normal operation rather than the loss induced by the data transmission. Our analysis shows the loss due to the forward-biasing parasitic diode D_P dominants the loss of the Class-E amplifier. Therefore, the PTE could be further improved by optimizing the duty cycle of the BPSK modulated signal to reduce the forward bias duration of D_P. This would be achieved at the cost of increased control complexity. As shown in [16], when k is relatively large (>0.05) as in our system, the source can be equivalent to a voltage source in series with a resistor R_1. Under the condition of resonance, the equivalent load impedance Z_{IN} is proportional to the value of the load resistor R_L, which increases with increasing distance. When Z_{IN} equals the source impedance, the transmission achieves the highest power efficiency. As a result, the power efficiency rises initially and then reduces with increasing distance. The analysis agrees well with the measurement result for each V_{DDT} in Figure 12. On the other hand, the conduction loss of the forward-bias diode (D_P in Figure 4(a)) rises exponentially with V_{DDT}. Therefore, the energy loss increases significantly with increasing V_{DDT}, leading to lower efficiency at heavy loads when V_{DDT} is high.

Figure 14(a) shows the measured output voltage of the energy recovery circuit, where V_{DDL} and V_{DD} are the output voltage of the rectifier and the voltage doubler, respectively. The charging up procedure of V_{DD} takes around 4 ms with 10 nF off-chip decoupling capacitance. Figures 14(b) and (c) show the measured V_{DD} versus the transmission distance and the coil misalignment along the X and Y axis. The minimum operating voltage of 1 V can be ensured when the transmission distance and the misalignment are below 7 mm.

4.2 Data telemetry

Figure 15(a) shows the measurement results of the TX and RX, including the transmitted data (D_{IN}), the output voltage of the primary coil (V_{RFIN}), the BPSK demodulation signal (BPSK_Reg), and the recovered data (D_{OUT}). Under 13.56 MHz carrier frequency and 3.39 Mbps data rate, the transmitted data can be correctly demodulated. Figure 14(b) shows the BER versus the transmission distance with different data rates. The BER is below the limit of measurement accuracy ($\leqslant 10^{-7}$) when the transmission distance is below 4 mm. At the maximum data rate of 3.39 Mbps, 2×10^{-7} BER can be ensured over a transmission distance of 5 mm, meeting the typical requirements of retina prostheses implants. The in-vitro measurement with a porcine stomach (Figure 9) shows $<10^{-6}$ BER can be obtained over a distance of 4 mm. Figure 16 shows the power consumption breakdown of the BPSK demodulator. When the data rate is 3.39 Mbps, the demodulator consumes 622 μW power, corresponding to 183 pJ/bit energy

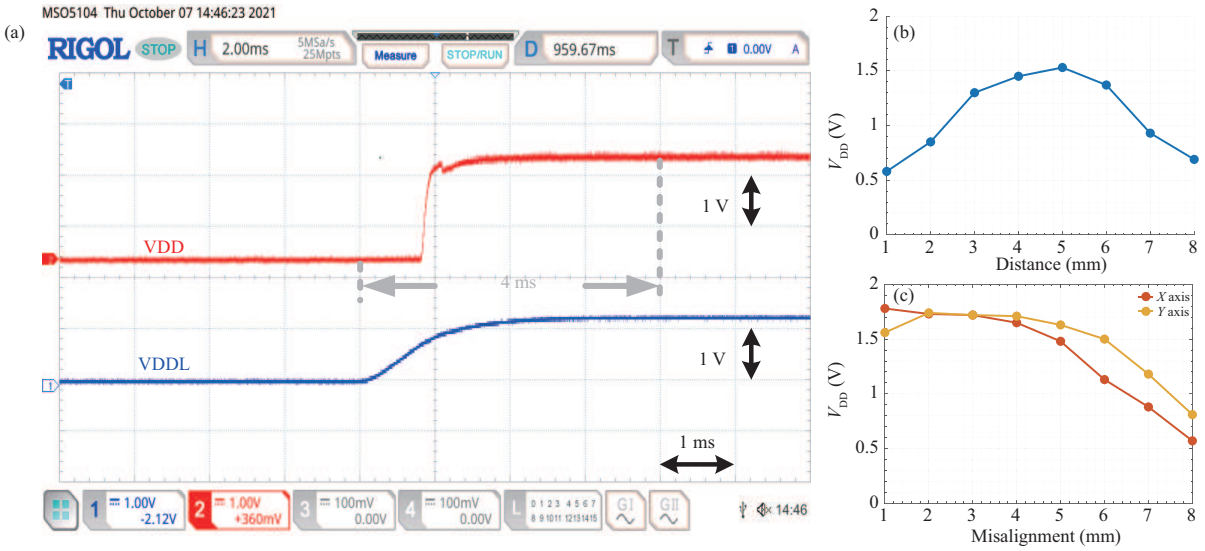

Figure 14 (Color online) (a) Measured output voltage of the energy recovery circuit; (b) measured V_{DD} versus transmission distance; (c) measured V_{DD} versus coil misalignment.

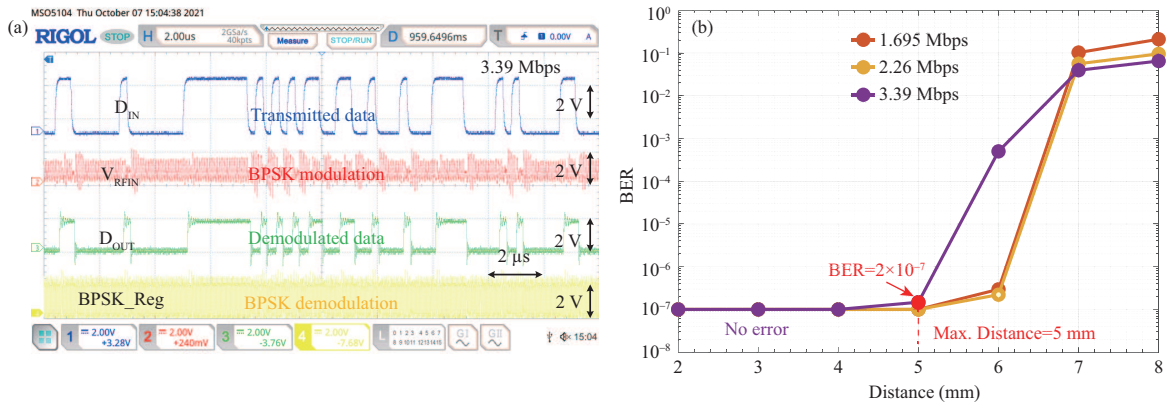

Figure 15 (Color online) (a) Measurement waveform of the TX and RX; (b) measured BER versus the transmission distance with different data rates.

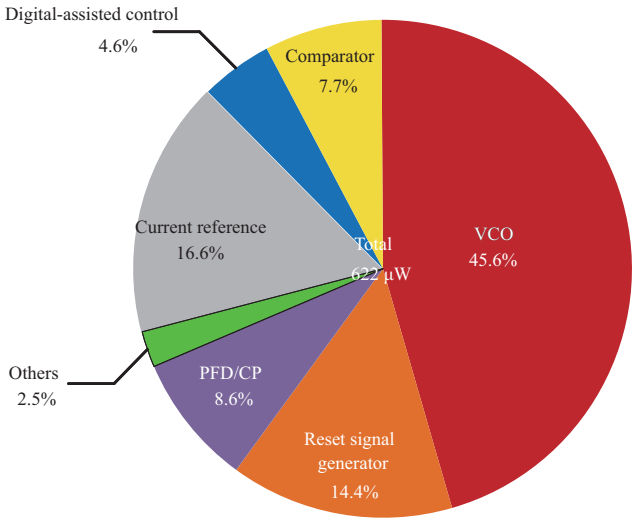

Figure 16 (Color online) RX power consumption breakdown.

Table 1 Performance comparison of wireless power-and-data telemetry circuit

		[15] TBCAS'2015	[2] TBCAS'2020	[31] JSSC'2018	[32] JSSC'2020	[33] ISSCC'2021	This work
Technology		350 nm CMOS	350 nm CMOS	180 nm CMOS	65 nm CMOS	180 nm BCD	**180 nm BCD**
Area (mm^2)		1.6	15	2.8	5.1	2.3	**0.96**
Direction		Downlink	Uplink/Downlink	Uplink/Downlink	Downlink	Downlink	**Downlink**
Coil pair No.		4	4	2	1	1	**1**
Data carrier frequency (MHz)		50	13.56	6.78	13.56	6.5/7.5	**13.56**
Transmission distance (mm)		10	1500	6.35	–	5	**5**
Power	Max. delivered power (mW)	42	–	520	9.2	115	**31.25**
	MAX. PTE	62%	–	74%	–	89.6%	**70%**
Data	Modulation mode	PDM	OOK/PPM	PWM OOK	ASK	FSK	**BPSK**
	Downlink data rate (Mbps)	13.56	0.05	0.03	0.15	2.5	**3.39**
	Bit error rate	4.3×10^{-7}	–	–	10^{-3}	4×10^{-7}	2×10^{-7}
	Data rate/carrier frequecy	0.271	0.004	0.003	0.011	0.33	**0.25**
	RX energy efficiency (pJ/bit)	162	4000	–	880	–	**183**

efficiency. The power consumption is dominant by the VCO, occupying 45.6%.

5 Conclusion

This paper presents power and data telemetry over a single 13.56-MHz inductive link for biomedical implants. The prototype has been fabricated with a 180 nm BCD process. The measurement results show that up to 31.25 mW of power can be delivered. The proposed BPSK modulator uses an innovative digital-assisted PLL that extends the maximum data rate to 1/4 of the carrier frequency (3.39 Mbps), with low BER (2×10^{-7}) over a transmission distance below 5 mm. The maximum PTE is 70%, whereas the RX energy efficiency is 183 pJ/bit. Table 1 summarizes the overall performance with a comparison to the-state-of-the-art [2,15,31–33]. This work achieves the highest data rate among the power and data telemetry over a single inductive link [32,33]. At the same time, the RX energy efficiency is competitive with the results with separate links [2,15].

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References

1 Rush A D, Troyk P R. A power and data link for a wireless-implanted neural recording system. IEEE Trans Biomed Eng, 2012, 59: 3255–3262
2 Jia Y, Guler U, Lai Y P, et al. A trimodal wireless implantable neural interface system-on-chip. IEEE Trans Biomed Circuits Syst, 2020, 14: 1207–1217
3 Sabor N, Li Y F, Zhang Z, et al. Detection of the interictal epileptic discharges based on wavelet bispectrum interaction and recurrent neural network. Sci China Inf Sci, 2021, 64: 162403
4 Desai N, Yoo J, Chandrakasan A P. A scalable, 2.9 mW, 1 Mb/s e-textiles body area network transceiver with remotely-powered nodes and bi-directional data communication. IEEE J Solid-State Circuits, 2014, 49: 1995–2004
5 Zhang Q R, Xie Q S, Duan K F, et al. A digital signal processor (DSP)-based system for embedded continuous-time cuffless blood pressure monitoring using single-channel PPG signal. Sci China Inf Sci, 2020, 63: 149402
6 Zhao K, Li Y F, Wang G X, et al. A robust QRS detection and accurate R-peak identification algorithm for wearable ECG sensors. Sci China Inf Sci, 2021, 64: 182401
7 Shi Y, Choi M, Li Z, et al. A 10 mm^3 inductive coupling radio for syringe-implantable smart sensor nodes. IEEE J Solid-State Circ, 2016, 51: 2570–2583
8 Ghovanloo M, Najafi K. A wideband frequency-shift keying wireless link for inductively powered biomedical implants. IEEE Trans Circ Syst I, 2004, 51: 2374–2383
9 Harrison R R, Watkins P T, Kier R J, et al. A low-power integrated circuit for a wireless 100-electrode neural recording system. IEEE J Solid-State Circuits, 2007, 42: 123–133
10 Jow U-M, Ghovanloo M. Design and optimization of printed spiral coils for efficient transcutaneous inductive power transmission. IEEE Trans Biomed Circ Syst, 2007, 1: 193–202
11 Ramrakhyani A K, Mirabbasi S, Chiao M. Design and optimization of resonance-based efficient wireless power delivery systems for biomedical implants. IEEE Trans Biomed Circ Syst, 2011, 5: 48–63
12 Wang G X, Liu W T, Sivaprakasam M, et al. Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants. IEEE Trans Circ Syst I, 2005, 52: 2109–2117
13 Simard G, Sawan M, Massicotte D. High-speed OQPSK and efficient power transfer through inductive link for biomedical implants. IEEE Trans Biomed Circ Syst, 2010, 4: 192–200
14 Kiani M, Jow U-M, Ghovanloo M. Design and optimization of a 3-coil inductive link for efficient wireless power transmission. IEEE Trans Biomed Circ Syst, 2011, 5: 579–591

15 Kiani M, Ghovanloo M. A 13.56-Mbps pulse delay modulation based transceiver for simultaneous near-field data and power transmission. IEEE Trans Biomed Circ Syst, 2015, 9: 1–11
16 Yousefi A, Abidi A A, Markovic D. Analysis and design of a robust, low-power, inductively coupled LSK data link. IEEE J Solid-State Circ, 2020, 55: 2583–2596
17 Trigui A, Hached S, Ammari A C, et al. Maximizing data transmission rate for implantable devices over a single inductive link: methodological review. IEEE Rev Biomed Eng, 2019, 12: 72–87
18 Kennedy H, Bodnar R, Lee T, et al. A high-Q resonant inductive link transmit driver with adaptive-predictive phase-continuous tuning and deviation frequency calibration for enhanced FSK/PSK modulation and power transfer. IEEE J Solid-State Circ, 2020, 55: 2401–2413
19 Harrison R R, Kier R J, Chestek C A, et al. Wireless neural recording with single low-power integrated circuit. IEEE Trans Neural Syst Rehabil Eng, 2009, 17: 322–329
20 Hu Y M, Sawan M. A fully integrated low-power BPSK demodulator for implantable medical devices. IEEE Trans Circ Syst I, 2005, 52: 2552–2562
21 Trigui A, Ali M, Ammari A C, et al. A 1.5-pJ/bit, 9.04-Mbit/s carrier-width demodulator for data transmission over an inductive link supporting power and data transfer. IEEE Trans Circ Syst II, 2018, 65: 1420–1424
22 Lee S-Y, Hsieh C-H, Yang C-M. Wireless front-end with power management for an implantable cardiac microstimulator. IEEE Trans Biomed Circ Syst, 2012, 6: 28–38
23 Ha S, Kim C, Park J, et al. Energy recycling telemetry ic with simultaneous 11.5 mW power and 6.78 Mb/s backward data delivery over a single 13.56 MHz inductive link. IEEE J Solid-State Circuits, 2016, 51: 2664–2678
24 Wu C Y, Qian X H, Cheng M S, et al. A 13.56 MHz 40 mW CMOS high-efficiency inductive link power supply utilizing on-chip delay-compensated voltage doubler rectifier and multiple LDOs for implantable medical devices. IEEE J Solid-State Circ, 2014, 49: 2397–2407
25 Hashemi S S, Sawan M, Savaria Y. A high-efficiency low-voltage CMOS rectifier for harvesting energy in implantable devices. IEEE Trans Biomed Circ Syst, 2012, 6: 326–335
26 Jung W, Oh S, Bang S, et al. An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler. IEEE J Solid-State Circ, 2014, 49: 2800–2811
27 Luo Z Y, Sonkusale S. A novel BPSK demodulator for biological implants. IEEE Trans Circ Syst I, 2008, 55: 1478–1484
28 Pan L, Chen M, Chen Y, et al. An energy-autonomous power-and-data telemetry circuit with digital-assisted-PLL-based BPSK demodulator for implantable flexible electronics applications. IEEE Open J Circ Syst, 2021, 2: 721–731
29 Haddad P A, Gosset G, Raskin J P, et al. Automated design of a 13.56 MHz 19 μW passive rectifier with 72% efficiency under 10 μA load. IEEE J Solid-State Circ, 2016, 51: 1290–1301
30 Chang R C H, Chen W C, Liu L, et al. An AC-DC rectifier with active and non-overlapping control for piezoelectric vibration energy harvesting. IEEE Trans Circuits Syst II, 2020, 67: 969–973
31 Desai N, Juvekar C, Chandak S, et al. An actively detuned wireless power receiver with public key cryptographic authentication and dynamic power allocation. IEEE J Solid-State Circuits, 2018, 53: 236–246
32 Ye D, Wang Y, Xiang Y, et al. A wireless power and data transfer receiver achieving 75.4% effective power conversion efficiency and supporting 0.1% modulation depth for ASK demodulation. IEEE J Solid-State Circ, 2020, 55: 1386–1400
33 Park Y, Koh S T, Lee J, et al. 33.7 a frequency-splitting-based wireless power and data transfer IC for neural prostheses with simultaneous 115 mW power and 2.5 Mb/s forward data delivery. In: Proceedings of IEEE International Solid- State Circuits Conference (ISSCC), 2021. 472–474