

# Degradation induced by holes in Si<sub>3</sub>N<sub>4</sub>/AlGa<sub>N</sub>/Ga<sub>N</sub> MIS HEMTs under off-state stress with UV light

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**Abstract** In this study, the negative shift of the threshold voltage ( $V_{TH}$ ) and degradation of the leakage current triggered by the ultraviolet (UV) light (375 nm) have been investigated when a large reverse gate-to-drain voltage was applied to a Si<sub>3</sub>N<sub>4</sub>/AlGa<sub>N</sub>/Ga<sub>N</sub> metal-insulator-semiconductor high electron mobility transistor. However, an increase in leakage was not observed under the blue light or in the dark. The holes generated in the channel by UV illumination were attracted by the gate electrode owing to the reverse voltage. During the movement, holes were captured by border traps at very deep levels in the Si<sub>3</sub>N<sub>4</sub> near AlGa<sub>N</sub>, leading to a negative shift of  $V_{TH}$  that was difficult to recover. According to the simulation based on Silvaco Atlas TCAD, the trapped holes significantly increased the electric field strength in Si<sub>3</sub>N<sub>4</sub>. Therefore, as the injection barrier for electrons from the gate became thinner, it was easier for electrons to tunnel through the Si<sub>3</sub>N<sub>4</sub>. Finally, for the degraded devices under the UV light stress, Fowler-Nordheim tunneling was the dominant leakage conduction mechanism, as exhibited by the current density versus electric field strength curve fitting. In addition, the holes with high energies collided with Si<sub>3</sub>N<sub>4</sub> and generated new defects at the edge of the gate near the drain side.

**Keywords** Ga<sub>N</sub>, MIS HEMTs, off-state stress, UV light, hole trapping

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## 1 Introduction

Gallium nitride (Ga<sub>N</sub>) based high electron mobility transistors (HEMTs) have garnered significant attention in power electronics applications owing to their excellent properties, such as high current densities, high critical electric field strengths, and low on-resistances [1–3]. In particular, the metal-insulator-semiconductor (MIS) structure is appealing to these applications as it features a low gate leakage current [4–6]. Presently, Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> deposited through atomic layer deposition are the two common gate insulators owing to their wide bandgaps and high permittivities. However, high density interface states and fixed charges at the oxide/Ga<sub>N</sub> interface may cause crucial reliability issues, such as a shift in the threshold voltage ( $V_{TH}$ ) [7–9]. In contrast, the Si<sub>3</sub>N<sub>4</sub>/Ga<sub>N</sub> system exhibits a more stable performance owing to the absence of Ga-O bonds [10, 11]. In comparison with Si<sub>3</sub>N<sub>4</sub> deposited through plasma-enhanced chemical vapor deposition (PECVD) and grown through metal organic chemical vapor deposition (MOCVD), low pressure chemical vapor deposition (LPCVD) Si<sub>3</sub>N<sub>4</sub> results in higher reliability owing to the advantages of high temperatures of approximately 800°C and no damage induced by the plasma impact [11–14]. Therefore, it is very important to investigate the degradation of LPCVD-Si<sub>3</sub>N<sub>4</sub> MIS HEMTs.

Several reports on the reliabilities of LPCVD-Si<sub>3</sub>N<sub>4</sub> MIS HEMTs, including the time-dependent dielectric breakdown (TDDB) [15, 16], bias temperature instability [17], and off-state stress [18, 19], have

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focused on degradation in the dark. However, it is also important to study the degradation of devices under illumination, which is a possible condition that exists in the actual operating environment. Illumination supplies energy for electrons trapped in body defects or interface states to overcome the potential barrier [20]. In addition, intrinsic GaN can absorb light with a wavelength of approximately 365 nm and generate photogenic carriers, increasing the electron concentration of the two-dimensional electron gas (2DEG). Meanwhile, the holes induced by the ultraviolet (UV) light could lower the barrier of the channel and increase the drain current ( $I_D$ ) [21, 22]. These transit behaviors of electrons and holes are unique as opposed to what is observed in the dark and can induce special degradation phenomena. The UV light can accelerate the de-trapping processes of electrons in the channel, affecting the permanent degradation resulting from TDDB [23]. Hua et al. [24, 25] stated that the new trap states, induced by the hole current during the reverse-bias stress under the UV light could trap electrons in the subsequent monitoring process. In this study, the degradation of the  $V_{TH}$  and leakage current in LPCVD-Si<sub>3</sub>N<sub>4</sub> MIS HEMT under the off-state stress was investigated under the UV light. During the short-term stress, a large and negative shift of  $V_{TH}$  was observed because holes generated by intrinsic excitation were accumulated under the gate. Furthermore, a jump in the off-state drain current ( $I_{D,off}$ ) occurred in the subsequent stress caused by the trapping and movement of holes.

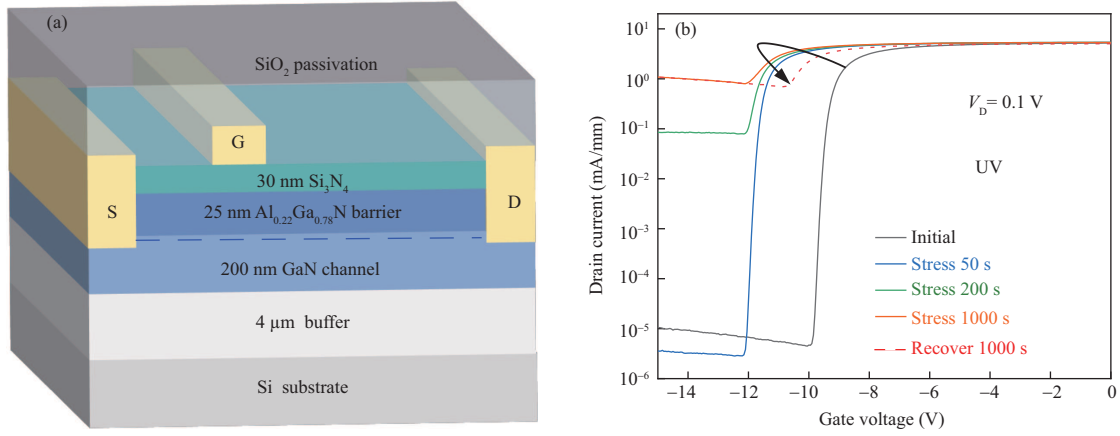
## 2 Device fabrication

All the off-state stresses in this study were conducted on the depletion-mode Si<sub>3</sub>N<sub>4</sub>/AlGaIn/GaN MIS HEMTs. A schematic of the device is shown in Figure 1(a). The epi-layers consisting of a 4 μm GaN buffer layer doped with C, a 200 nm undoped GaN channel, and a 25 nm Al<sub>0.22</sub>Ga<sub>0.78</sub>N barrier layer were grown on a silicon substrate through metal organic chemical vapor deposition. The device fabrication process flow began with mesa etching, and thereafter a 30 nm Si<sub>3</sub>N<sub>4</sub> layer was deposited through LPCVD. The source and drain regions were defined by inductively coupled plasma etching, followed by the evaporation of the Ti/Al/Ni/Au stacked metal and rapid annealing to form an ohmic contact; Ni/Au was evaporated for the gate electrode. The SiO<sub>2</sub> layer was subsequently grown through PECVD as the second passivation layer. Finally, the interconnections for the device tests were fabricated through the evaporation of Ti/Au. The devices under test had a gate-to-source space of 3 μm, gate-to-drain space of 20 μm, and gate length of 3 μm. In this study, the Cascade M150 probe station and UV light were both connected to a Keysight B1500A semiconductor device analyzer and a B2201A low-leakage-switch mainframe, such that the power supplies for devices and illuminants were both controlled by EasyEXPERT software for a rapid switching time.

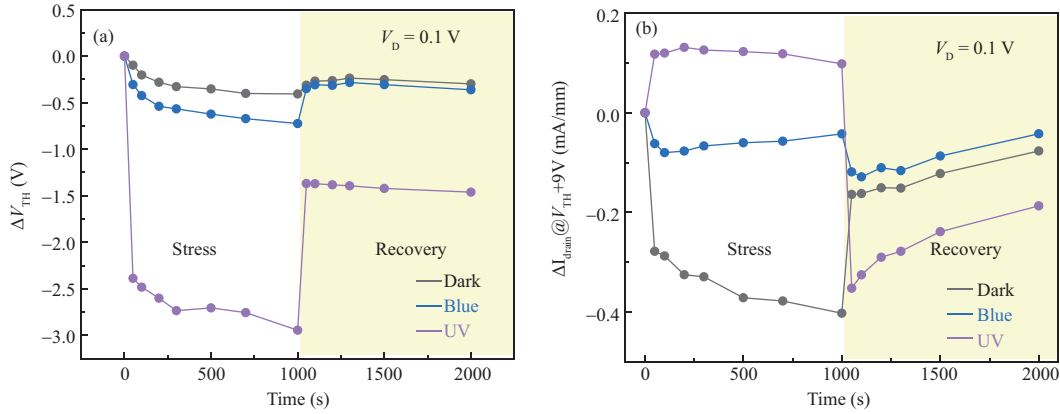
## 3 Results and discussion

During the off-state stress, to standardize the gate overdrive voltage, stress conditions were performed with  $V_{TH} - 5$  and 100 V at the gate and drain electrodes, respectively. The source electrode was grounded, and the substrate did not have an electrical connection. UV light with a wavelength of 375 nm (3.31 eV) was illuminated during the stress duration. The intensity of the light on the device was 4420 lx. The light was thereafter turned off in the intermediate monitoring process, and it remained off during the recovery period. The degradation of the  $V_{TH}$  and  $I_D$  was the primary focus of our experiment, and  $V_{TH}$  was extracted using the Max-gm method. Figure 1(b) shows the transfer-characteristic curves monitored in the linear region ( $V_D = 0.1$  V), and a two-step shift in  $I_{D,off}$  was observed. In the initial stress, the  $I_{D,off}$  declined after 50 s of stress. Under an off-state bias condition, electrons were injected from the gate to the channel to form an  $I_{D,off}$ . The electrons from the gate electrode trapped at the Si<sub>3</sub>N<sub>4</sub> caused an increase in the energy band and hence restricted the gate leakage. After the stress of 200 s, an increase in the  $I_{D,off}$  was observed and  $V_{TH}$  drifted negatively during the stress.

The purple line illustrates the evolution of  $V_{TH}$  during the monitoring process in Figure 2(a). The device under the UV light exhibited a large  $\Delta V_{TH}$  value of approximately  $-3$  V. Because the UV light with a wavelength of 375 nm penetrated SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, and AlGaIn layers and arrived at the GaN layer directly, the intrinsic excitation at the GaN layer occurred once the UV light was turned on. The photon-generated electron-hole pairs were separated owing to the potential distribution in the channel. With the negative bias of the gate, holes were attracted to the gate, leading to a negative  $V_{TH}$  shift in the subsequent monitoring process. After recovery for 1000 s,  $V_{TH}$  could not return to the initial state,



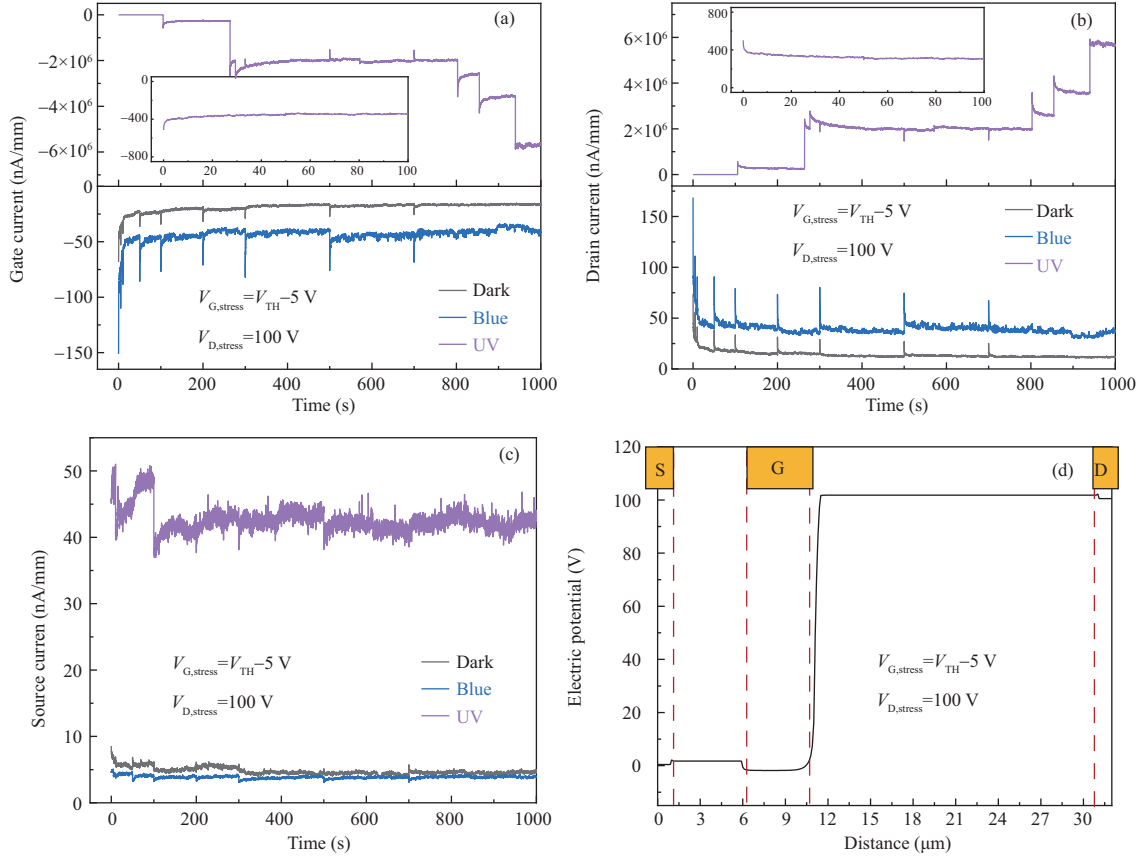
**Figure 1** (Color online) (a) The cross-sectional diagram of the MIS HEMTs; (b)  $I_D$ - $V_G$  curves measured during the off-state stress under UV light.



**Figure 2** (Color online) (a)  $\Delta V_{TH}$  and (b) the normalized on-state  $I_D$  during the stress and recovery processes.

indicating the capture of holes in traps at very deep levels. Because the negative shift of  $V_{TH}$  may also be caused by electron de-trapping, one fresh device was exposed to the blue light (475 nm, 2.71 eV) for 40 s, and the transfer characteristics were measured in the dark.  $V_{TH}$  remained unchanged after illumination (not shown). This indicated that electrons originally trapped in the gate dielectric, which affected  $V_{TH}$ , could not be de-trapped by illumination. Therefore, the negative shift of  $V_{TH}$  was due to hole generation. Experiments on the same stress biases were conducted under blue light and dark ambient conditions.  $V_{TH}$  shifted slightly to the negative side during the stress, as shown in Figure 2(a), and partially recovered after 1000 s. During the off-state stress, a small number of holes might be generated by impact ionization in the channel owing to the peak electric field of 3.1 MV/cm calculated through simulation based on Silvaco Atlas TCAD. Moreover, during the recovery process, holes trapped in shallow traps at the gate insulator layer can be de-trapped, leading to the recovery of  $V_{TH}$  drifts.

In addition, to rule out current shifts corresponding to  $V_{TH}$  drifts and focus on degradation in the access region under illumination, the on-state  $I_D$  was normalized at  $V_G = V_{TH} + 9$  V and  $V_D = 0.1$  V. The shift in the normalized  $I_D$  under different illumination is shown in Figure 2(b). During the stress duration, the normalized  $I_D$  first decreased under dark and blue light conditions. This was because the electrons from the gate were injected into  $Si_3N_4$  through the drain-side gate edge and depleted the 2DEG. Under the blue light, a series of traps at the  $Si_3N_4$ /AlGaIn interface were excited, and electrons were de-trapped, leading to a slow increase in the  $I_{D,off}$  with an increase in the stress time. In particular, the normalized  $I_D$  increased significantly under the UV light because of the electron-hole pairs generated by intrinsic excitation in the channel. During the recovery duration in the dark, the currents increased in a similar trend, owing to the defects in the access region releasing electrons. Therefore, the dominant factor for degradation in the access region was the capture-emission of electrons which was different from the degradation dominated by holes under the gate.



**Figure 3** (Color online) Comparisons of current under dark, blue and UV illumination during the stress of 1000 s on (a) gate, (b) drain, and (c) source electrodes. (d) The potential distributions in the channel under an off-state stress bias condition.

The current of the gate, drain, and source during the stress ( $I_{G,\text{stress}}$ ,  $I_{D,\text{stress}}$ , and  $I_{S,\text{stress}}$ ) are shown in Figures 3(a)–(c), respectively, which helps us to understand the degeneration process of devices under the UV light. The  $I_{D,\text{stress}}$  was almost identical to  $I_{G,\text{stress}}$  under all illuminations, which indicated that the path of the leakage current was mainly between the gate and drain during the stress. During the initial stress, as shown in the inset of Figure 3(a), the gate current under the UV light was larger than that in the dark and under the blue light. This indicates that the photon-generated holes were attracted to the gate. Attention should be taken to the positive  $I_{S,\text{stress}}$  that exhibited a large value at the beginning of the stress under the UV light. To determine the flow of carriers, the electric potentials in the channel with  $V_{\text{TH}} - 5$  and 100 V at the gate and drain electrodes, respectively, were simulated. Potential distributions under the drain and source electrodes were both higher than those of the gate electrode, appealing to the photon-generated electrons in the gate-drain and gate-source regions, respectively, and holes in the channel flowed to the gate. Because of the presence of hole-traps in  $\text{Si}_3\text{N}_4$ , holes were captured during the movement, and a negative  $V_{\text{TH}}$  shift was observed. In addition, the photon-generated holes were numerous and the damage caused by collisions was severe during the movement of holes. New defects were created in the gate insulator and permanent damage occurred.

To further verify the degradation of  $I_{D,\text{off}}$  during the stress process, the gate current was measured at varying temperatures from 300 to 400 K. Figures 4(a) and (b) show the electrical properties of the initial and degraded devices after the UV light stress, respectively. For the initial device, Poole-Frenkel (P-F) emission was the dominant conduction mechanism when the gate voltage decreased from  $-10$  to  $-15$  V. The insulator and barrier layers were regarded as equivalent barrier layers because the trends of internal electric field versus gate voltage were similar in this voltage region [26]. The dependence on both the electric field and temperature of the P-F emission current density is expressed as follows:

$$\ln(J/E) = R(T)\sqrt{E} + S(T)$$

with

$$R(T) = -\frac{q}{kT} \sqrt{\frac{q}{\pi \varepsilon_0 \varepsilon_e}},$$

$$S(T) = -\frac{q\emptyset_t}{kT} + \ln C,$$

where  $E$  denotes the electric field in the equivalent barrier layer (the detailed calculation formula is shown in [27, 28]),  $\varepsilon_e$  is the permittivity of the equivalent barrier layer,  $\emptyset_t$  is the barrier height for the electron emission from the trap states, and  $C$  is a constant. Figure 4(c) shows the plot of  $\ln(J/E)$  versus  $\sqrt{E}$  and the  $y$ -intercept is  $S(T)$ . The plot of  $S(T)$  versus  $q/kT$  should yield a straight line, as shown in the inset. The value of  $\emptyset_t$  extracted from Figure 4(c) is  $\sim 0.69$  eV.

For the degraded devices, holes could be trapped at deep levels and changed the electric field distributions. Therefore, the electric field was corrected according to the simulation.  $V_{\text{TH}}$  shifted negatively after positive charges with a concentration of  $2 \times 10^{12} \text{ cm}^{-2}$  were added to  $\text{Si}_3\text{N}_4$ , and the value of the  $V_{\text{TH}}$  shift was calibrated by referring to the  $V_{\text{TH}}$  measured after recovery. In particular, the increment of the electric field strength in  $\text{Si}_3\text{N}_4$  ( $\Delta E_{\text{inter}}$ ) was constant ( $4.83 \times 10^5 \text{ V/cm}$ ) in the off-state of the device. Therefore, the electric field used in the leakage mechanism fitting was modified to  $E' = E + \Delta E_{\text{inter}}$ . As shown in Figure 4(b), for the degraded devices, the gate leakage currents with the gate voltage ranging from  $-10$  to  $-15 \text{ V}$  were only electrical-field-dependent. The current under varying temperatures fitted well with the Fowler-Nordheim (F-N) tunneling mechanism, as shown in Figure 4(d). The F-N tunneling current density is expressed as follows:

$$\ln(J/E'^2) = A - B/E'$$

with

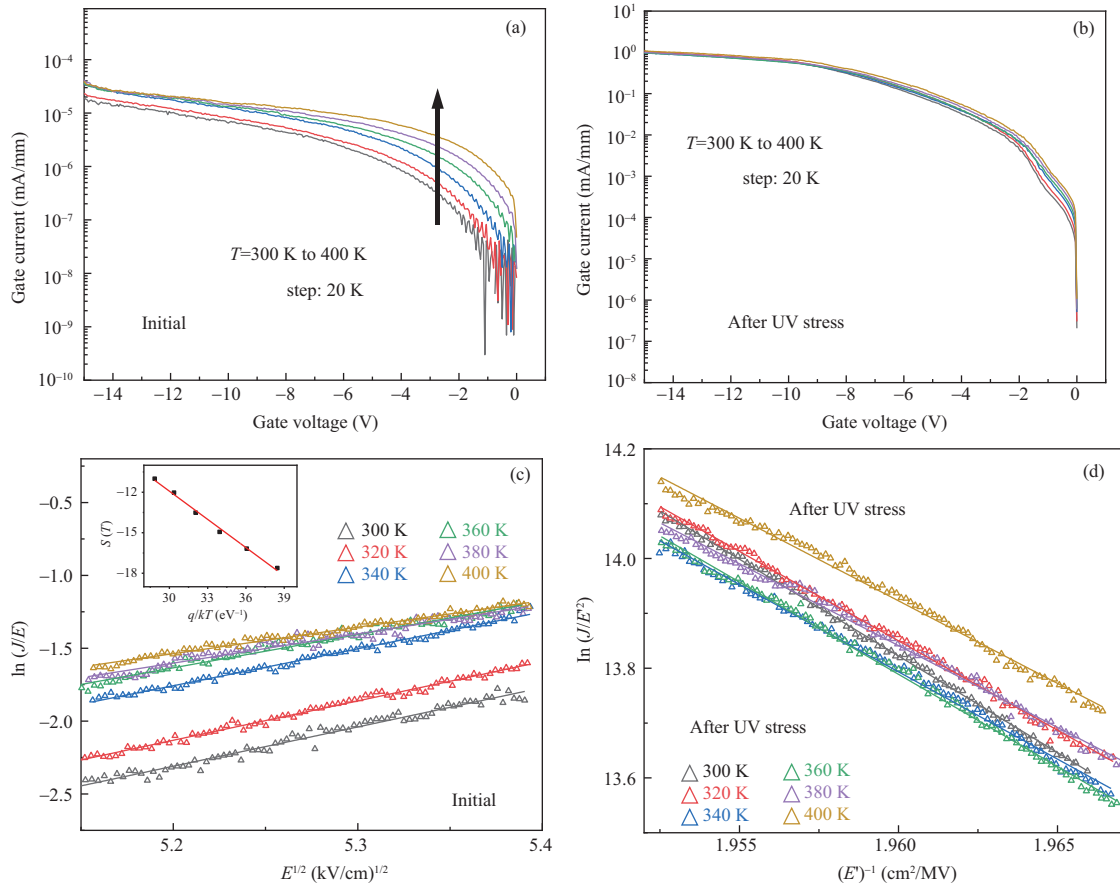
$$B = \frac{8\pi \sqrt{2m_n^*} (q\emptyset_{\text{eff}})^3}{3qh},$$

where  $A$  is a constant,  $m_n^*$  represents the conduction band effective mass, and  $\emptyset_{\text{eff}}$  denotes the effective barrier height. The plot of  $\ln(J/E'^2)$  versus  $E'$  is shown in Figure 4(d). The change in the leakage mechanism proved that the holes trapped at deep levels enhanced the electric field strength in  $\text{Si}_3\text{N}_4$ , and the triangular barrier made it easier for electrons to tunnel from the gate.

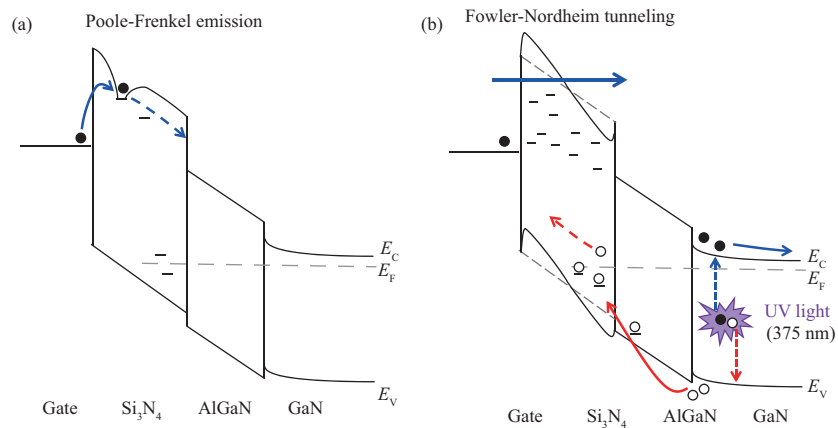
Based on the above discussion, a physical model of the degradation caused by holes in the off-state stress is proposed. Figures 5(a) and (b) show the energy band under the gate of the initial and degraded devices under the off-state stress, respectively. For the fresh devices, electrons from the gate electrode flowed into the channel through emission-capture, forming a leakage dominated by P-F emission. At the onset of the off-state stress, the electrons from the gate were trapped in  $\text{Si}_3\text{N}_4$  and rise the energy band; thus, the gate leakage was restricted by the larger barrier height. Meanwhile, under the UV light, photogenic electron-hole pairs were generated in the access region. Thereafter, they were separated by a large potential variance in the channel, and electrons flowed toward the drain and source while holes accumulated under the gate. Holes were closer to the channel than electrons and caused a negative shift in  $V_{\text{TH}}$ . Because of the reverse electric field under the gate, holes flowed toward the gate gradually and were captured by the border traps in the  $\text{Si}_3\text{N}_4$  near AlGaIn. The trapped holes increased the electric field strength in  $\text{Si}_3\text{N}_4$ . Therefore, the tunneling barrier became thinner and made it easier for electrons to tunnel from the gate, as shown in Figure 5(b). In addition, the holes with high energies collided with  $\text{Si}_3\text{N}_4$  and generated new defects. Because of the large reverse electric field at the gate edge near the drain side, the collision was more violent here.

## 4 Conclusion

In conclusion, the degradation of  $\text{Si}_3\text{N}_4/\text{GaIn}$  MIS-HEMTs in the off-state stress under illumination was mainly caused by holes. Under the UV light, holes were generated by intrinsic excitation and flowed toward the gate because of the large reverse electric field in the channel. During the movement of holes, they could be trapped in border traps in the  $\text{Si}_3\text{N}_4$ , causing a negative shift in  $V_{\text{TH}}$ . The trapped holes increased the electric field strength in  $\text{Si}_3\text{N}_4$  and made it easier for electrons to tunnel from the gate. Finally, the dominant gate leakage mechanism changed from P-F emission to F-N tunneling. In



**Figure 4** (Color online) The transfer characteristics of the (a) initial and (b) degraded devices at different temperatures from 300 to 400 K. (c) PF emission plot for the initial device. Inset: the plot of  $S(T)$  versus  $q/kT$ . (d) F-N tunneling plots for the degraded device.



**Figure 5** (Color online) The vertical band diagrams of the (a) initial and (b) degraded devices.

addition, the holes with high energies collided with  $\text{Si}_3\text{N}_4$  and generated new defects. Therefore, we should primarily focus on the UV exposure of MIS-HEMTs in practical applications.

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## References

- 1 Ikeda N, Niiyama Y, Kambayashi H, et al. GaN power transistors on Si substrates for switching applications. *Proc IEEE*, 2010, 98: 1151–1161
- 2 Millan J, Godignon P, Perpina X, et al. A survey of wide bandgap power semiconductor devices. *IEEE Trans Power Electron*, 2014, 29: 2155–2163
- 3 Chen K J, Haberlen O, Lidow A, et al. GaN-on-Si power technology: devices and applications. *IEEE Trans Electron Device*, 2017, 64: 779–795
- 4 Zhu J J, Zhu Q, Chen L X, et al. Exponential dependence of capture cross section on activation energy for interface traps in  $\text{Al}_2\text{O}_3/\text{AlN}/\text{AlGaIn}/\text{GaN}$  metal-insulator-semiconductor heterostructures. *Appl Phys Lett*, 2017, 111: 163502
- 5 Yatabe Z, Hori Y, Ma W C, et al. Characterization of electronic states at insulator/(Al)GaN interfaces for improved insulated gate and surface passivation structures of GaN-based transistors. *Jpn J Appl Phys*, 2014, 53: 100213
- 6 Tapajna M, Jurkovič M, Válik L, et al. Bulk and interface trapping in the gate dielectric of GaN based metal-oxide-semiconductor high-electron-mobility transistors. *Appl Phys Lett*, 2013, 102: 243509
- 7 Lagger P, Ostermaier C, Pobegen G, et al. Towards understanding the origin of threshold voltage instability of AlGaIn/GaN MIS-HEMTs. In: *Proceedings of International Electron Devices Meeting (IEDM)*, 2012
- 8 Lagger P, Reiner M, Pogany D, et al. Comprehensive study of the complex dynamics of forward bias-induced threshold voltage drifts in GaN based MIS-HEMTs by stress/recovery experiments. *IEEE Trans Electron Device*, 2014, 61: 1022–1030
- 9 Yang S, Tang Z K, Wong K Y, et al. High-quality interface in  $\text{Al}_2\text{O}_3/\text{GaN}/\text{GaIn}/\text{AlGaIn}/\text{GaN}$  MIS structures with in situ pre-gate plasma nitridation. *IEEE Electron Device Lett*, 2013, 34: 1497–1499
- 10 Hua M Y, Liu C, Yang S, et al. 650-V GaN-based MIS-HEMTs using LPCVD-SiN<sub>x</sub> as passivation and gate dielectric. In: *Proceedings of the 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015. 10–14
- 11 Sun H, Wang M J, Chen J G, et al. Fabrication of high-uniformity and high-reliability  $\text{Si}_3\text{N}_4/\text{AlGaIn}/\text{GaN}$  MIS-HEMTs with self-terminating dielectric etching process in a 150-mm Si foundry. *IEEE Trans Electron Device*, 2018, 65: 4814–4819
- 12 Liu Z Y, Huang S, Bao Q L, et al. Investigation of the interface between LPCVD-SiN<sub>x</sub> gate dielectric and III-nitride for AlGaIn/GaN MIS-HEMTs. *J Vacuum Sci Tech B*, 2016, 34: 041202
- 13 Cai X B, Hua M Y, Zhang Z F, et al. Atomic-scale identification of crystalline GaON nanophase for enhanced GaN MIS-FET channel. *Appl Phys Lett*, 2019, 114: 053109
- 14 Zhang Z L, Yu G H, Zhang X D, et al. Studies on high-voltage GaN-on-Si MIS-HEMTs using LPCVD  $\text{Si}_3\text{N}_4$  as gate dielectric and passivation layer. *IEEE Trans Electron Device*, 2016, 63: 731–738
- 15 Jauss S A, Hallaceli K, Mansfeld S, et al. Reliability analysis of LPCVD SiN gate dielectric for AlGaIn/GaN MIS-HEMTs. *IEEE Trans Electron Device*, 2017, 64: 2298–2305
- 16 Zhao Y W, Li L A, Que T T, et al. Experimental evaluation of interface states during time-dependent dielectric breakdown of GaN-based MIS-HEMTs with LPCVD-SiN<sub>x</sub> gate dielectric. *Chin Phys B*, 2020, 29: 067203
- 17 Que T T, Zhao Y W, Li L A, et al. Effect of overdrive voltage on PBTI trapping behavior in GaN MIS-HEMT with LPCVD SiN<sub>x</sub> gate dielectric. *Chin Phys B*, 2020, 29: 037201
- 18 Hua M Y, Wei J, Bao Q L, et al. Reverse-bias stability and reliability of hole-barrier-free E-mode LPCVD-SiN<sub>x</sub>/GaN MIS-FETs. In: *Proceedings of International Electron Devices Meeting (IEDM)*, 2017
- 19 Hua M Y, Wei J, Bao Q L, et al. Dependence of  $V_{\text{TH}}$  stability on gate-bias under reverse-bias stress in E-mode GaN MIS-FET. *IEEE Electron Device Lett*, 2018, 39: 413–416
- 20 Li B K, Tang X, Chen K J. Optical pumping of deep traps in AlGaIn/GaN-on-Si HEMTs using an on-chip Schottky-on-heterojunction light-emitting diode. *Appl Phys Lett*, 2015, 106: 093505
- 21 Zhang S K, Wang W B, Shtau I, et al. Backilluminated GaN/AlGaIn heterojunction ultraviolet photodetector with high internal gain. *Appl Phys Lett*, 2002, 81: 4862–4864
- 22 Caddemi A, Cardillo E, Salvo G, et al. Microwave effects of UV light exposure of a GaN HEMT: measurements and model extraction. *Microelectron Reliab*, 2016, 65: 310–317
- 23 Warnock S, del Alamo J A. OFF-state TDDDB in high-voltage GaN MIS-HEMTs. In: *Proceedings of IEEE International Reliability Physics Symposium (IRPS)*, 2017
- 24 Hua M Y, Wei J, Bao Q L, et al. Hole-induced threshold voltage shift under reverse-bias stress in E-Mode GaN MIS-FET. *IEEE Trans Electron Device*, 2018, 65: 3831–3838
- 25 Hua M Y, Yang S, Wei J, et al. Hole-induced degradation in E-mode GaN MIS-FETs: impact of substrate terminations. *IEEE Trans Electron Device*, 2020, 67: 217–223
- 26 Dutta G, DasGupta N, DasGupta A. Gate leakage mechanisms in AlInN/GaN and AlGaIn/GaN MIS-HEMTs and its modeling. *IEEE Trans Electron Device*, 2017, 64: 3609–3615
- 27 Turuvekere S, Karumuri N, Rahman A A, et al. Gate leakage mechanisms in AlGaIn/GaN and AlInN/GaN HEMTs: comparison and modeling. *IEEE Trans Electron Device*, 2013, 60: 3157–3165
- 28 Zhu J J, Ma X H, Hou B, et al. Investigation of gate leakage mechanism in  $\text{Al}_2\text{O}_3/\text{Al}_{0.55}\text{Ga}_{0.45}\text{N}/\text{GaN}$  metal-oxide-semiconductor high-electron-mobility transistors. *Appl Phys Lett*, 2014, 104: 153510